Module-1 BJT AC Analysis:

BJT AC Analysis: BJT AC Analysis: BJT Transistor Modeling, The re transistor model, Common emitter fixed bias, Voltage divider bias, Emitter follower configuration. Darlington connection-DC bias; The Hybrid equivalent model, Approximate Hybrid Equivalent Circuit-Fixed bias, Voltage divider, Emitter follower configuration; Complete Hybrid equivalent model, Hybrid π Model.

BJT Transistor Modeling

- A model is an equivalent circuit that represents the AC characteristics of the transistor.
- Transistor small signal amplifiers can be considered linear for most application.
- A model is the best approximate of the actual behavior of a semiconductor device under specific operating conditions, including circuit elements

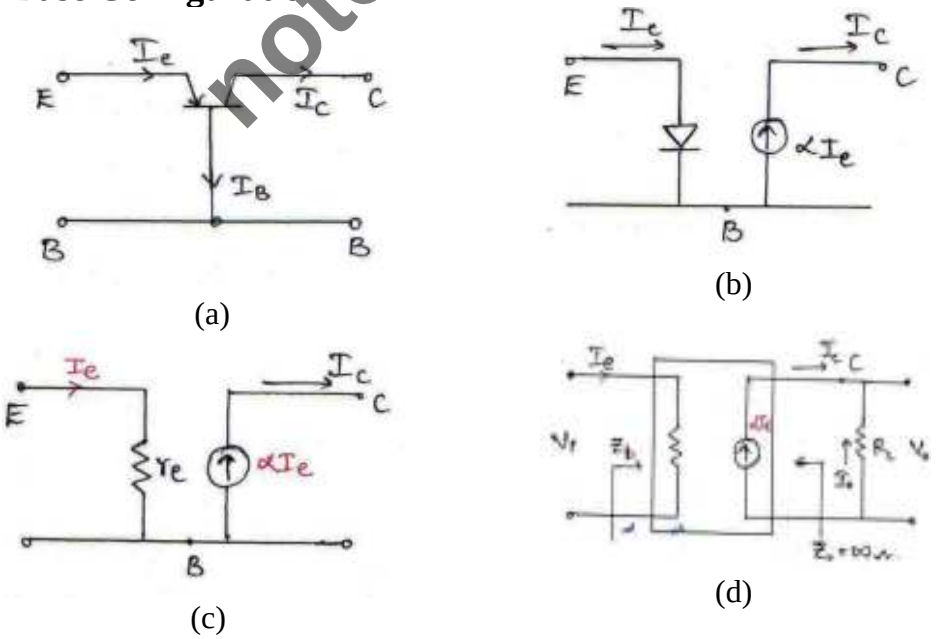
Transistor Models

- ✓ r_e- model – any region of operation, fails to account for output impedance, less accuracy
- ✓ Hybrid model – limited to a particular operating conditions, more accuracy

The r_e Transistor Model

BJTs are basically current-controlled devices; therefore the r_e models uses a diode and a current source to duplicate the behavior of the transistor. **One disadvantage to this model is its sensitivity to the DC level. This model is designed for specific circuit conditions.**

Common-Base Configuration



(a) (b) (c) (d)

Figure 1 Common Base transistor re mode

We know that from diode equation r_e is defined as follows

$$I_c = \alpha I_e$$

$$r_e = \frac{26\,\text{mV}}{I_e}$$

Applying KVL to input and out circuit of figure 1(d), we will get

input impedance: $Z_i = r_e$

Output impedance: $Z_o = \infty$

Voltage gain: $A_v = \frac{\alpha R_L}{r_e} = \frac{R_L}{r_e}$

Current gain: $A_i = -\alpha = -1$

Common-Emitter Configuration

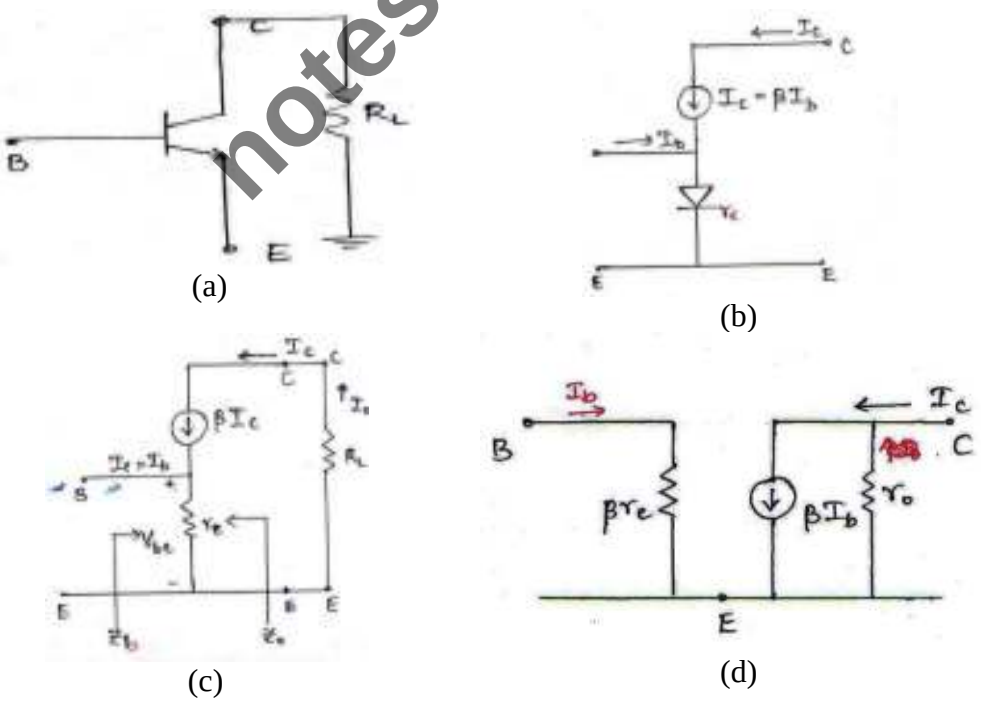


Figure 2 Common Emitter re model of npn transistor

Figure 1 (a) shows simple transistor circuit. Figure 1(b) and 1(c) shows evaluation transistor re model in CE configuration.

Applying KVL to input and out circuit of figure 2(d), we will get

input impedance: $\boldsymbol{z_i = \frac{V_i}{I_i}}$

$V_i = V_{be} = I_e r_e = \beta I_i r_e$

$Z_i = r_e$

Output impedance: $Z_o = \infty$

Voltage gain:

$V_o = -I_o R_L = -(I_c) R_L = -\beta I_b R_L$

$V_i = I_i Z_i = I_b \beta r_e$

$$A_v = \frac{V_o}{V_i} = -\frac{\beta I_b R_L}{I_b \beta r_e}$$

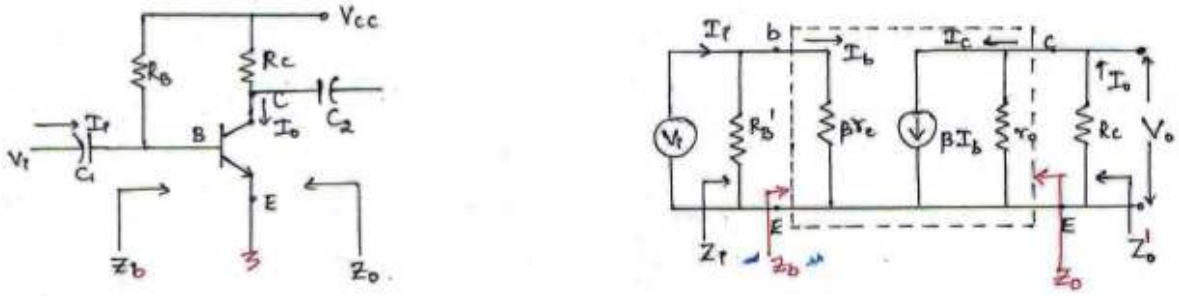
$$A_v = -\frac{R_L}{r_e}$$

Current gain,

$$A_i = \frac{I_o}{I_i} = \frac{I_c}{I_b} = \frac{\beta I_b}{I_b}$$

$A_i = \beta$

Fixed bias Common-Emitter Configuration



(a) (b)

Figure 3 Fixed bias Common-Emitter Configuration

Note in Fig. 3 (a) that the common ground of the dc supply and the transistor emitter terminal permits the relocation of R_B and R_C in parallel with the input and output sections of the transistor, respectively. In addition, note the placement of the important network parameters Z_i, Z_o, I_i, and I_o on the redrawn network. Substituting the r_e model for the common-emitter configuration of Fig. 3(a) will result in the network of Fig. 3(b).

• From the above r_e model,

Input impedance

$Z_i = [R_B \,||\, \beta r_e]$ ohms

If $R_B > 10\ \beta r_e$, then,

$[R_B \,||\, \beta r_e] \cong \beta r_e$

Then, $Z_i \cong \beta r_e$

Output impedance

Z_o is the output impedance when $V_i = 0$. When $V_i = 0$, $i_b = 0$, resulting in open circuit equivalence for the current source.

$Z_o = [R_C \,||\, r_o]$ ohms

Voltage gain

$V_o = - \beta I_b (R_C \,||\, r_o)$

• From the r_e model, $I_b = V_i / \beta r_e$

• thus,

– $V_o = - \beta (V_i / \beta r_e) (R_C \,||\, r_o)$

– $A_V = V_o / V_i = - (R_C \,||\, r_o) / r_e$

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• If $r_o > 10 R_C$,

– $A_V = - (R_C / r_e)$

• The negative sign in the gain expression indicates that there exists 180o phase shift between the input and output.

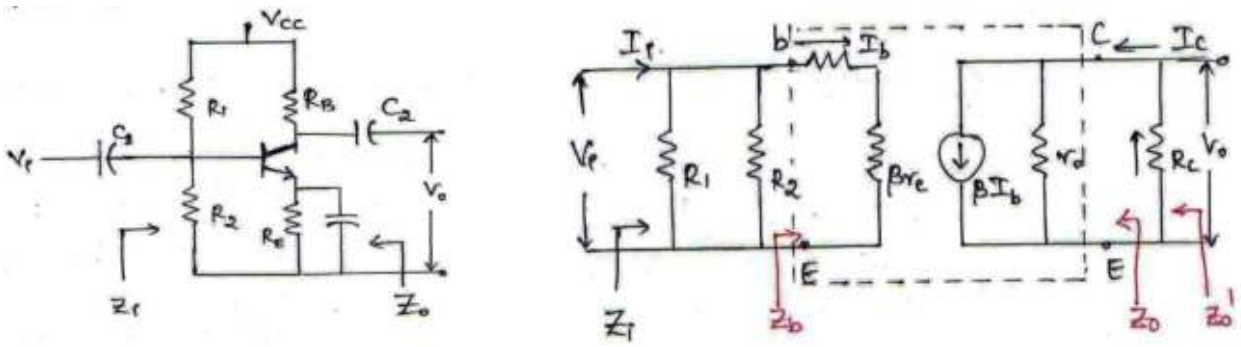
Current gain:

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}$$

$$A_i \cong \beta \Big|_{r_o \geq 10 R_C,\ R_B \geq 10 \beta r_e}$$

$$A_i = -A_v \frac{Z_i}{R_C}$$

Common-Emitter Voltage-Divider Bias



(a) (b)

Figure 4 Voltage Divider bias Common-Emitter Configuration

The r_e model is very similar to the fixed bias circuit except for R_B is $R_1 || R_2$ in the case of voltage divider bias.

Input impedance:

$$Z_b = \beta r_e$$
$$R_B = R_1 || R_2$$
$$Z_i = R_B || \beta r_e$$

Output impedance:

$$Z_o = r_o$$
$$Z_o' = R_C || r_o$$
$$Z_o{}' = R_C | r_{o \gg 10R_C}$$

Voltage gain: From the r_e model, $I_b = V_i / \beta r_e$ thus,

$$V_o = - \beta (V_i / \beta r_e) (R_C \| r_o)$$

$$A_v = \frac{V_o}{V_i} = \frac{-R_C || r_o}{r_e}$$

$$A_v = \frac{V_o}{V_i} \cong \frac{-R_C}{r_e} | r_o \geq 10R_C$$

Current gain:

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}$$

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_B}{(R_B + \beta r_e)} \quad \text{if} \quad r_o \geq 10R_C$$

$$A_i = \frac{I_o}{I_i} = \beta \quad \text{if} \quad R_B \geq 10\beta r_e$$

$$A_i = -A_v \frac{Z_i}{R_C}$$

Common-Emitter Emitter-Bias Configuration

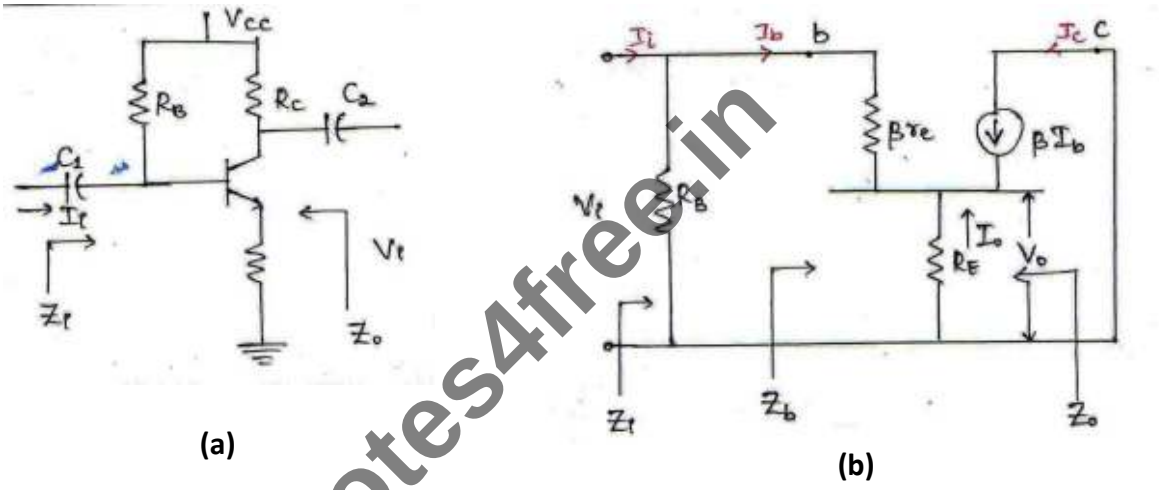


Figure 4 Fixed bias Common-Emitter Configuration with un bypassed R_E

Input impedance:

Applying KVL to the input side:

$$V_i = I_b \beta r_e + I_e R_E$$

$$V_i = I_b \beta r_e + (\beta + 1) I_b R_E$$

Input impedance looking into the network to the right of RB is

$$Z_b = V_i / I_b = \beta r_e + (\beta + 1) R_E$$

Since $\beta >> 1$, $(\beta + 1) = \beta$

$$Z_b = V_i / I_b = \beta (r_e + R_E)$$

Since R_E is often much greater than r_e,

$$Z_b = \beta R_E,$$

$$Z_i = R_B || Z_b$$

Output impedance: Z_o is determined by setting V_i to zero, $I_b = 0$ and βI_b can be replaced by open circuit equivalent. The result is,

$$Z_o = R_C$$

Voltage gain:

We know that, $V_o = - I_o R_C$

$= - \beta I_b R_C$

$= - \beta (V_i / Z_b) R_C$

$A_V = V_o / V_i = - \beta [R_C / (r_e + R_E)]$

$R_E >> r_e$, $A_V = V_o / V_i = - \beta [R_C / R_E]$

$$A_v = \frac{V_o}{V_i} = \frac{-R_C || r_o}{Z_b}$$

Substituting, $Z_b = \beta(r_e + R_E)$

$$A_v = \frac{V_o}{V_i} \cong \frac{-R_C}{r_e + R_E} | Z_b = \beta(r_e + R_E)$$

$$A_v = \frac{V_o}{V_i} \cong \frac{-R_C}{R_E} | (r_e \ll R_E)$$

Phase relation: The negative sign in the gain equation reveals a 180_o phase shift between input and output.

Current gain:

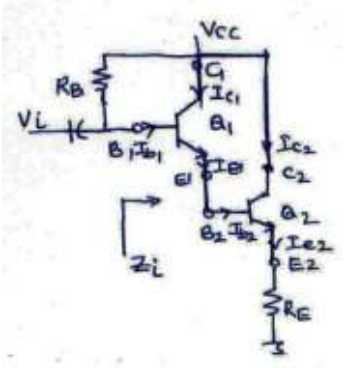
$$A_i = \frac{I_o}{I_i} = \frac{\beta R_B}{(R_B + Z_b)}$$

$$A_i = -A_v \frac{Z_i}{R_C}$$

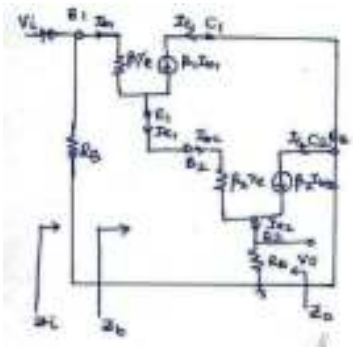
Darlington Emitter Follower

This is also known as the common-collector configuration.

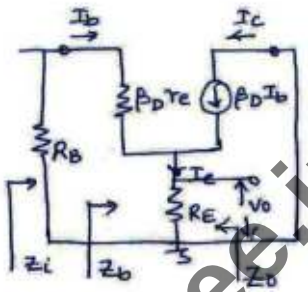
• The input is applied to the base and the output is taken from the emitter. There is no phase shift between input and output.



(a)



(b)



(c)

Figure 5 Darlington Emitter Follower

Input impedance:

$$Z_i = R_B \,||\, Z_b$$
$$Z_b = \beta_D r_e + (\beta_D + 1)R_E$$
$$Z_b = \beta_D (r_e + R_E)$$

Since R_E is often much greater than r_e,

$$Z_i = R_B || \beta r_e$$
$$Z_b = \beta_D (r_e + R_E)$$

Output impedance:

To find Zo, it is required to find output equivalent circuit of the emitter follower at its input terminal.

This can be done by writing the equation for the current Ib.

$$I_b = V_i / Z_b$$
$$I_e = (\beta_D + 1) I_b$$
$$= (\beta_D + 1)(V_i / Z_b)$$

We know that, $Z_b = \beta_D r_e + (\beta_D + 1)R_E$ substituting this in the equation for Ie we get,

$$I_e = (\beta_D + 1)(V_i / Z_b) = (\beta_D + 1)(V_i / \beta_D r_e + (\beta_D + 1)R_E)$$

$$I_e = V_i / [\beta_D r_e / (\beta_D + 1)] + R_E$$

Since $(\beta_D + 1) = \beta_D$,

$$I_e = V_i / [r_e + R_E]$$

Using the equation $I_e = V_i / [r_e + R_E]$, we can write the output equivalent circuit as,

$$Z_o = R_E || \frac{\beta_D r_e}{\beta_D + 1}$$

$$Z_o \approx R_E || r_e \qquad \text{if } \beta_D \gg 1$$

Since R_E is typically much greater than r_e, $Z_o \approx r_e$

Voltage gain:

Using voltage divider rule for the equivalent circuit,

$$V_o = V_i R_E / (R_E + r_e)$$

$$A_V = V_o / V_i = [R_E / (R_E + r_e)]$$

Since $(R_E + r_e) \cong R_E$,

$A_V \cong [R_E / (R_E] \cong 1$

Phase relationship As seen in the gain equation, output and input are in phase

Current gain:

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_B}{(R_B + Z_b)}$$

H – Parameter model :-

→ The equivalent circuit of a transistor can be dram using simple approximation by retaining its essential features.

→ These equivalent circuits will aid in analyzing transistor circuits easily and rapidly.

Two port devices & Network Parameters:-

→ A transistor can be treated as a two part network. The terminal behaviour of any two part network can be specified by the terminal voltages V_1 & V_2 at parts 1 & 2 respectively and current i_1 and i_2, entering parts 1 & 2, respectively, as shown in figure.

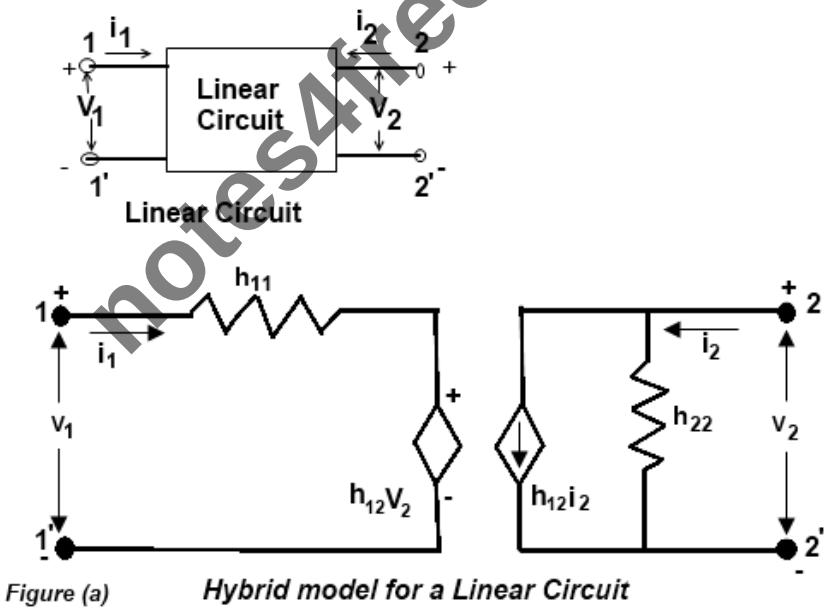


Figure 6 Two port Network

Hybrid parameters (or) h – parameters:-

If the input current i_1 and output Voltage V_2 are takes as independent variables, the input voltage V_1 and output current i_2 can be written as

$V_1 = h_{11}\, i_1 + h_{12}\, V_2$

$i_2 = h_{21} i_1 + h_{22} V_2$

The four hybrid parameters h_{11}, h_{12}, h_{21} and h_{22} are defined as follows.

$h_{11} = [V_1 / i_1]$ with $V_2 = 0$	Input Impedance with output part short circuited.
$h_{22} = [i_2 / V_2]$ with $i_1 = 0$	Output admittance with input part open circuited.
$h_{12} = [V_1 / V_2]$ with $i_1 = 0$	reverse voltage transfer ratio with input part open circuited.
$h_{21} = [i_2 / i_1]$ with $V_2 = 0$	Forward current gain with output part short circuited.

The dimensions of h – parameters are as follows:

h_{11} - Ω

h_{22} – mhos

h_{12}, h_{21} – dimension less.

as the dimensions are not alike, (ie) they are hybrid in nature, and these parameters are called as hybrid parameters.

i= 11 = input ; o = 22 = output ;

f = 21 = forward transfer ; r = 12 = Reverse transfer.

Notations used in transistor circuits:-

$h_i = h_{11}$ = Short circuit input impedance

$h_0 = h_{22}$ = Open circuit output admittance

$h_r = h_{12}$ = Open circuit reverse voltage transfer ratio

$h_f = h_{21}$= Short circuit forward current Gain.

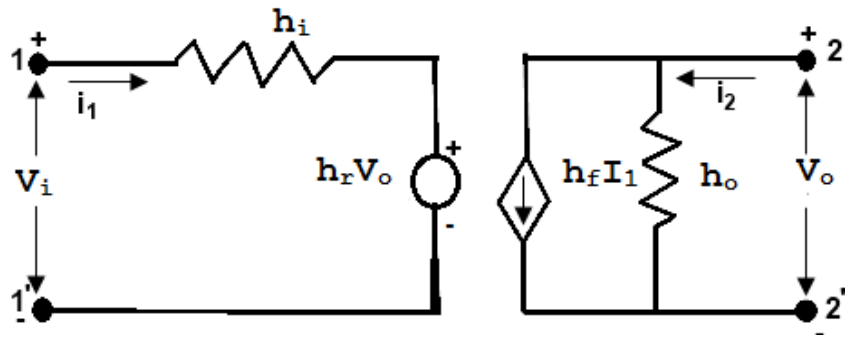
The Hybrid Model for Two-port Network:-

$V_1 = h_{11} i_1 + h_{12} V_2$

$I_2 = h_1 i_1 + h_{22} V_2$

$V_1 = h_1 i_1 + h_r V_2$

$I_2 = h_f\, i_1 + h_0\, V_2$



Transistor Hybrid model:-

Essentially, the transistor model is a three terminal two – port system.

The h – parameters, however, will change with each configuration.

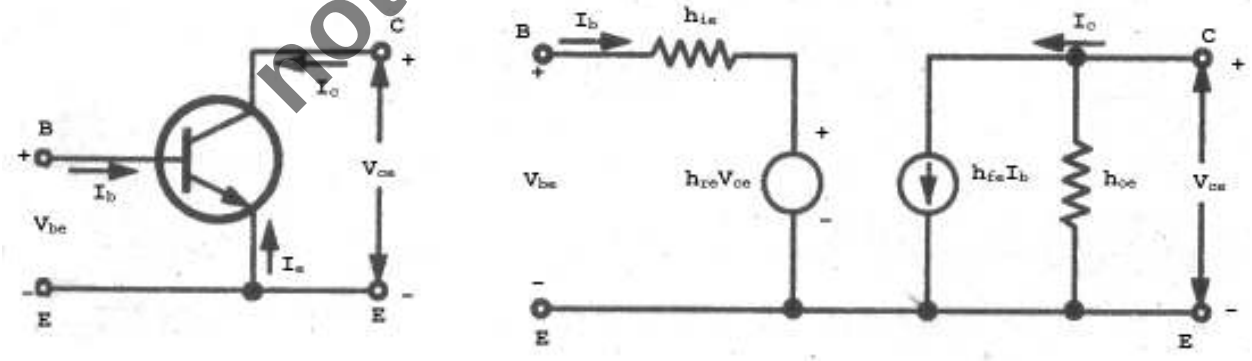
To distinguish which parameter has been used or which is available, a second subscript has been added to the h – parameter notation.

For the common – base configuration, the lowercase letter b is added, and for common emitter and common collector configurations, the letters e and c are used respectively.

Normally h_r is a relatively small quantity, its removal is approximated by h_r and $h_r V_o = 0$, resulting in a short – circuit equivalent.

The resistance determined by $1/h_o$ is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open – circuit quivalent.

CE Transistor Circuit



To Derive the Hybrid model for transistor consider the CE circuit shown in figure.The variables are $i_{B,}$ i_c, $v_{B(=V_{BE})}$ and $v_{c(=V_{CE}).}$ i_B and v_c are considered as independent variables.

Then , $v_B = f_1(i_{B,}\, v_c)$ ----------(1)

$i_C = f_2(i_{B,}\, v_c)$ ----------(2)

Making a Taylor's series expansion around the quiescent point $I_{B,}$ V_C and neglecting higher order terms, the following two equations are obtained.

$\Delta v_B = (\partial f_1/\partial i_B)V_c \,.\, \Delta i_B + (\partial f_1/\partial v_c)I_B \,.\, \Delta v_C$ ----------(3)

$\Delta i_C = (\partial f_2/\partial i_B)V_c \,.\, \Delta i_B + (\partial f_2/\partial v_c)I_B \,.\, \Delta v_C$ ----------(4)

The partial derivatives are taken keeping the collector voltage or base current constant as indicated by the subscript attached to the derivative.

Δv_B , Δv_C , Δi_C , Δi_B represent the small signal(increment) base and collector voltages and currents,they are represented by symbols v_b , v_c , i_b and i_c respectively.

Eqs (3) and (4) may be written as

$V_b = h_{ie}\, i_b + h_{re}\, V_c$

$i_c = h_{fe}\, i_b + h_{oe}\, V_c$

Where $h_{ie} = (\partial f_1/\partial i_B)V_c = (\partial v_B/\partial i_B)V_c = (\Delta v_B/\Delta i_B)V_c = (v_b/i_b)V_c$

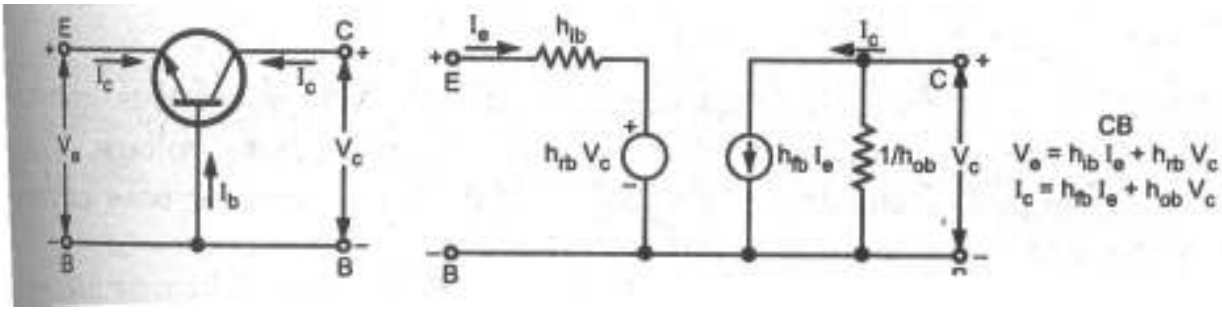
$h_{re} = (\partial f_1/\partial v_c)I_B = (\partial v_B/\partial v_c)\, I_B = (\Delta v_B/\Delta v_c)\, I_B = (v_b/v_c)\, I_B$

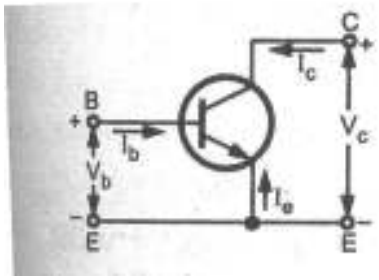
$h_{fe} = (\partial f_2/\partial i_B)V_c = (\partial i_c/\partial i_B)V_c = (\Delta i_c/\Delta i_B)V_c = (i_c/i_b)V_c$

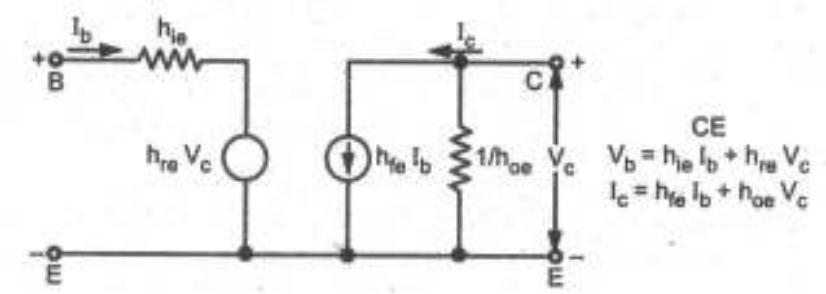
$h_{oe} = (\partial f_2/\partial v_c)I_B = (\partial i_c/\partial v_c)\, I_B = (\Delta i_c/\Delta v_c)\, I_B = (i_c/v_c)\, I_B$

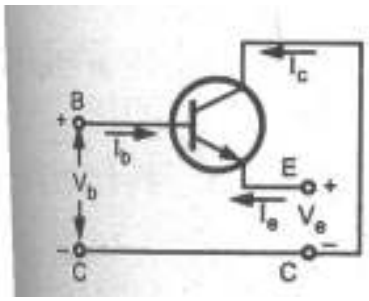
The above equations define the h-parameters of the transistor in CE configuration.The same theory can be extended to transistors in other configurations.

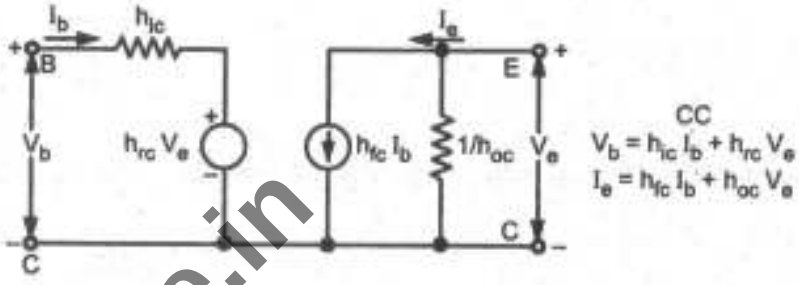
Hybrid Model and Equations for the transistor in three different configurations are are given below.







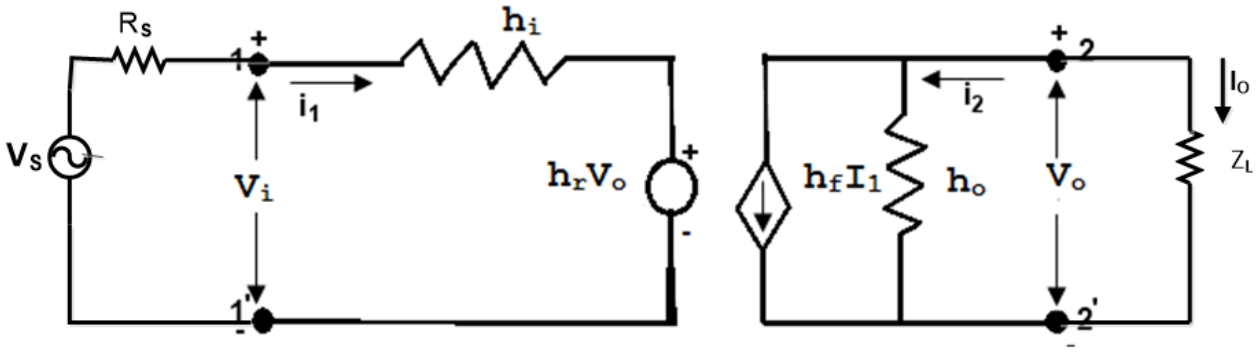




Comparision of H parameters

CB	CE	CC
$h_{ib} = \frac{v_{eb}}{i_e}$	$h_{ie} = \frac{v_{be}}{i_b}$	$h_{ic} = \frac{v_{bc}}{i_b}$
$h_{rb} = \frac{v_{eb}}{v_{cb}}$	$h_{re} = \frac{v_{be}}{v_{ce}}$	$h_{rc} = \frac{v_{bc}}{v_{ec}}$
$h_{fb} = \frac{i_c}{i_e}$	$h_{fe} = \frac{i_c}{i_b}$	$h_{fc} = \frac{i_e}{i_b}$
$h_{ob} = \frac{i_c}{v_{cb}}$	$h_{oe} = \frac{i_c}{v_{ce}}$	$h_{oc} = \frac{i_e}{v_{ec}}$

Analysis of transistor amplifier using h parameters.



For analysis of transistor amplifier we have to determine the following terms:

- Current Gain
- Voltage gain
- Input impedance
- Output impedance

Current gain:

For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_i = \frac{I_L}{I_b} = \frac{-I_c}{I_b} \qquad (I_L + I_c = 0. \quad \therefore I_L = -I_c)$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$V_o = I_L Z_L = -I_c Z_L$$

$$\therefore I_c = h_{fe}\ I_b + h_{oe}\ (-I_c\ Z_L)$$

$$\text{or } \frac{I_c}{I_b} = \frac{h_{fe}}{1 + h_{oe} Z_L}$$

$$\therefore A_i = -\frac{h_{fe}}{1 + h_{oe} Z_L}$$

Input Impedence:

The impedence looking into the amplifier input terminals (1,1') is the input impedence Z_i

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_I Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \qquad (\text{since } Y_L = \frac{1}{Z_L})$$

Voltage gain:

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_c}{V_b} = - \frac{I_C Z_L}{V_b}$$

$$\therefore A_v = \frac{I_B A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

Output Admittance: It is defined

$$Y_0 = \left.\frac{I_c}{V_c}\right|_{V_s} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe}\frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $\quad R_s . I_b + h_{ie} . I_b + h_{re} V_c = 0.$

$$\frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{re}\, h_{fe}}{R_s + h_{ie}}$$

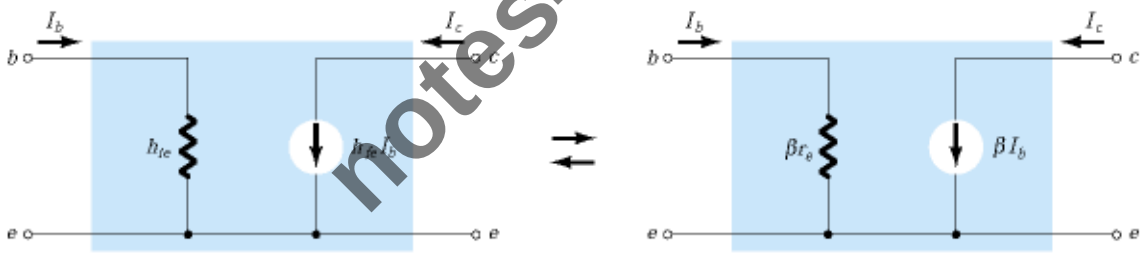
Voltage amplification taking into account source impedance (R_S) is given by

$$A_{VS} = \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_S} \qquad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i\right)$$

$$= A_V \cdot \frac{Z_i}{Z_i + R_s}$$

$$= \frac{A_i\, Z_L}{Z_i + R_s}$$

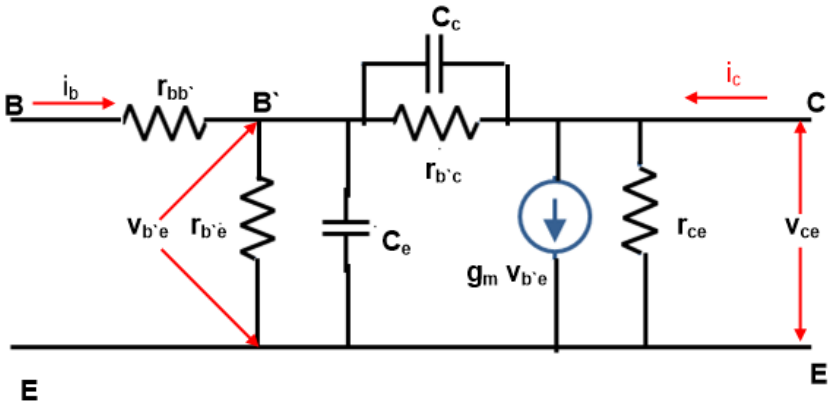
Simplified Hybrid model is identical to the re model is as shown in fig. refer re model analysis



Hybrid versus re model: (a) common-emitter configuration

Hybrid · π model

- The hybrid-pi or Giacoletto model of common emitter transistor model is given below. The resistance components in this circuit can be obtained from the low frequency hparameters.
- For high frequency analysis transistor is replaced by high frequency hybrid-pi model and voltage gain, current gain and input impedance are determined.



This is more accurate model for high frequency effects. The capacitors that appear are stray parasitic capacitors between the various junctions of the device. These capacitances come into picture only at high frequencies.

- C_{bc} or C_u is usually few pico farads to few tens of pico farads.
- r_{bb} includes the base contact, base bulk and base spreading resistances.
- r_{be} (r_π), r_{bc}, r_{ce} are the resistances between the indicated terminals.
- r_{be} (r_π) is simply βr_e introduced for the CE r_e model.
- r_{bc} is a large resistance that provides feedback between the output and the input.
- $r_\pi = \beta r_e$
- $g_m = 1/r_e$
- $r_o = 1/h_{oe}$
- $h_{re} = r_\pi / (r_\pi + r_{bc})$

The **transconductance, gm**, is related to the dynamic (differential) resistance, re, of the forward-biased emitter-base junction:

$$g_m = \partial Ic/\partial Vb' e$$
$$= \alpha \partial Ie/\partial Vb'e$$
$$\approx \alpha/re$$
$$\approx Ic/Vth$$

Vth = kBT/q

The resistance rbb' is the base spreading resistance.

The resistance rb'c and the capacitance Cb'c (Cc) represent the dynamic (differential) resistance and the capacitance of the reverse-biased collector-base junction.

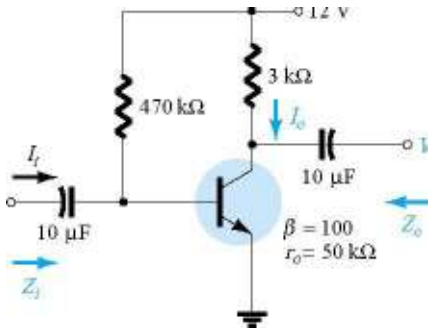
Using transconductance:

$$i_c \approx g_m v_{b'e}$$

(ignoring the current through r_{ce})

Example 1

(a) Determine r_e. (b) Find Z_i (c) Calculate Z_o (d) Determine A_v (e) Find A_i (f) Repeat parts (c) through (e) including $r_o = 50\ k\Omega$ in all calculations and compare results. (From Text Book - Boylestad)



Solution

(a) DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\ V - 0.7\ V}{470\ k\Omega} = 24.04\ \mu A$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu A) = 2.428\ mA$$

$$r_e = \frac{26\ mV}{I_E} = \frac{26\ mV}{2.428\ mA} = \mathbf{10.71\ \Omega}$$

(b) $\beta r_e = (100)(10.71\ \Omega) = 1.071\ k\Omega$

$$Z_i = R_B \| \beta r_e = 470\ k\Omega \| 1.071\ k\Omega = \mathbf{1.069\ k\Omega}$$

(c) $Z_o = R_C = \mathbf{3\ k\Omega}$

(d) $$A_v = -\frac{R_C}{r_e} = -\frac{3\ k\Omega}{10.71\ \Omega} = \mathbf{-280.11}$$

(e) Since $R_B \geq 10\beta r_e (470\ k\Omega > 10.71\ k\Omega)$

$$A_i \cong \beta = \mathbf{100}$$

(f) $Z_o = r_o \| R_C = 50\ k\Omega \| 3\ k\Omega = \mathbf{2.83\ k\Omega}$ vs. $3\ k\Omega$

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\ k\Omega}{10.71\ \Omega} = \mathbf{-264.24}\ \text{vs.}\ -280.11$$

$$A_i = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)} = \frac{(100)(470\ k\Omega)(50\ k\Omega)}{(50\ k\Omega + 3\ k\Omega)(470\ k\Omega + 1.071\ k\Omega)}$$

$$= \mathbf{94.13}\ \text{vs.}\ 100$$

As a check:

$$A_i = -A_v \frac{Z_i}{R_C} = \frac{-(-264.24)(1.069\ k\Omega)}{3\ k\Omega} = \mathbf{94.16}$$

which differs slightly only due to the accuracy carried through the calculations.

Example 2

For the network of Figure, determine:

(a) r_e

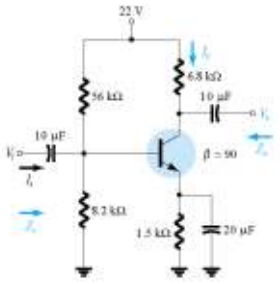
(b) Z_i

(c) Z_o ($r_o = \infty\ \Omega$).

(d) A_v ($r_o = \infty\ \Omega$).

(e) A_i ($r_o = \infty\ \Omega$).

(f) The parameters of parts (b) through (e) if $r_o = 1/h_{oe} = 50\ \text{k}\Omega$ and compare results.



Solution

(a) DC: Testing $\beta R_E > 10R_2$

$$(90)(1.5\ \text{k}\Omega) > 10(8.2\ \text{k}\Omega)$$

$$135\ \text{k}\Omega > 82\ \text{k}\Omega\ (\textit{satisfied})$$

Using the approximate approach,

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2\ \text{k}\Omega)(22\ \text{V})}{56\ \text{k}\Omega + 8.2\ \text{k}\Omega} = 2.81\ \text{V}$$

$$V_E = V_B - V_{BE} = 2.81\ \text{V} - 0.7\ \text{V} = 2.11\ \text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11\ \text{V}}{1.5\ \text{k}\Omega} = 1.41\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.41\ \text{mA}} = \mathbf{18.44\ \Omega}$$

(b) $R' = R_1 \| R_2 = (56\ \text{k}\Omega) \| (8.2\ \text{k}\Omega) = 7.15\ \text{k}\Omega$

$Z_i = R' \| \beta r_e = 7.15\ \text{k}\Omega \| (90)(18.44\ \Omega) = 7.15\ \text{k}\Omega \| 1.66\ \text{k}\Omega$

$= \mathbf{1.35\ k\Omega}$

(c) $Z_o = R_C = \mathbf{6.8\ k\Omega}$

(d) $A_v = -\frac{R_C}{r_e} = -\frac{6.8\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$

(e) The condition $R' \geq 10\beta r_e$ ($7.15\ \text{k}\Omega \geq 10(1.66\ \text{k}\Omega) = 16.6\ \text{k}\Omega$ is *not* satisfied. Therefore,

$$A_i \cong \frac{\beta R'}{R' + \beta r_e} = \frac{(90)(7.15\ \text{k}\Omega)}{7.15\ \text{k}\Omega + 1.66\ \text{k}\Omega} = \mathbf{73.04}$$

(f) $Z_i = \mathbf{1.35\ k\Omega}$

$Z_o = R_C \| r_o = 6.8\ \text{k}\Omega \| 50\ \text{k}\Omega = \mathbf{5.98\ k\Omega}$ vs. $6.8\ \text{k}\Omega$

$A_v = \frac{R_C \| r_o}{r_e} = \frac{5.98\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-324.3}$ vs. -368.76

The condition

$$r_o \geq 10R_C\ (50\ \text{k}\Omega \geq 10(6.8\ \text{k}\Omega) = 68\ \text{k}\Omega)$$

is *not* satisfied. Therefore,

$$A_i = \frac{\beta R' r_o}{(r_o + R_C)(R' + \beta r_e)} = \frac{(90)(7.15\ \text{k}\Omega)(50\ \text{k}\Omega)}{(50\ \text{k}\Omega + 6.8\ \text{k}\Omega)(7.15\ \text{k}\Omega + 1.66\ \text{k}\Omega)}$$

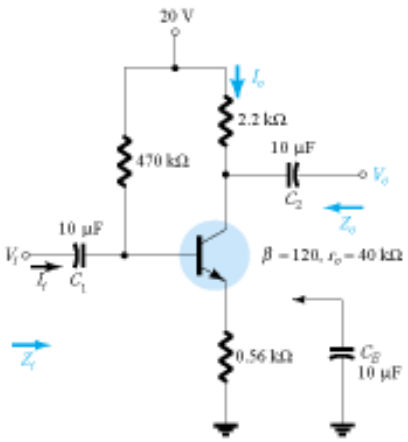
$= \mathbf{64.3}$ vs. 73.04

There was a measurable difference in the results for Z_o, A_v, and A_i because condition $r_o \geq 10R_C$ was *not* satisfied.

Example 3

For the network of Fig. , without C_E (unbypassed), determine:

(a) r_e
(b) Z_i
(c) Z_o
(d) A_v
(e) A_i



Solution

(a) DC: $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega + (121)0.56\text{ k}\Omega} = 35.89\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(46.5\ \mu\text{A}) = 4.34\text{ mA}$$

and $$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.34\text{ mA}} = \mathbf{5.99\ \Omega}$$

(b) Testing the condition $r_o \geq 10(R_C + R_E)$:

$$40\text{ k}\Omega \geq 10(2.2\text{ k}\Omega + 0.56\text{ k}\Omega)$$

$$40\text{ k}\Omega \geq 10(2.76\text{ k}\Omega) = 27.6\text{ k}\Omega\ (\textit{satisfied})$$

Therefore,

$$Z_b \cong \beta(r_e + R_E) = 120(5.99\ \Omega + 560\ \Omega)$$
$$= 67.92\text{ k}\Omega$$

and $$Z_i = R_B \| Z_b = 470\text{ k}\Omega \| 67.92\text{ k}\Omega$$
$$= \mathbf{59.34\ k\Omega}$$

(c) $Z_o = R_C = \mathbf{2.2\ k\Omega}$

(d) $r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\text{ k}\Omega)}{67.92\text{ k}\Omega}$$
$$= \mathbf{-3.89}$$

compared to -3.93 using Eq. (8.27): $A_v \cong -R_C/R_E$

(e) $$A_i = -A_v \frac{Z_i}{R_C} = -(-3.89)\left(\frac{59.34\text{ k}\Omega}{2.2\text{ k}\Omega}\right)$$
$$= \mathbf{104.92}$$

compared to 104.85 using Eq. (8.28): $A_i \cong \beta R_B/(R_B + Z_b)$.

Example 4

Repeat the analysis of Example 3 with C_E in place.

Solution

(a) The dc analysis is the same, and $r_e = 5.99\ \Omega$.

(b) R_E is "shorted out" by C_E for the ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\ \text{k}\Omega \| (120)(5.99\ \Omega)$$
$$= 470\ \text{k}\Omega \| 718.8\ \Omega \cong \mathbf{717.70\ \Omega}$$

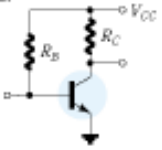
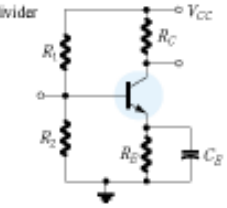
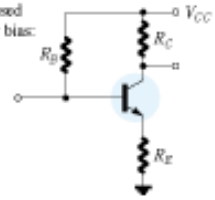
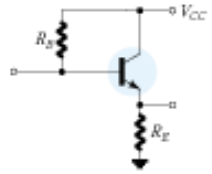
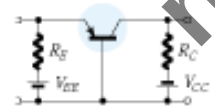
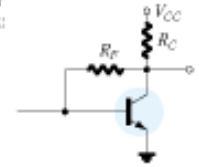
(c) $Z_o = R_C = \mathbf{2.2\ k\Omega}$

(d) $$A_v = -\frac{R_C}{r_e}$$
$$= -\frac{2.2\ \text{k}\Omega}{5.99\ \Omega} = \mathbf{-367.28}$$ (a significant increase)

(e) $$A_i = \frac{\beta R_B}{R_B + Z_b} = \frac{(120)(470\ \text{k}\Omega)}{470\ \text{k}\Omega + 718.8\ \Omega}$$
$$= \mathbf{119.82}$$

Summary of Transistor small signal analysis

TABLE 8.1 Relative Levels for the Important Parameters of the CE, CB, and CC Transistor Amplifiers

Configuration	Z_i	Z_o	A_v	A_i
Fixed-bias: 	Medium (1 kΩ) $= R_B \| \beta r_e$ $= \beta r_e$ $(R_B \geq 10\beta r_e)$	Medium (2 kΩ) $= R_C \| r_o$ $= R_C$ $(r_o \geq 10R_C)$	High (−200) $= -\frac{(R_C \| r_o)}{r_e}$ $\cong -\frac{R_C}{r_e}$ $(r_e \geq 10R_C)$	High (100) $= \frac{\beta R_B r_o}{(r_e + R_C)(R_B + \beta r_e)}$ $\cong \beta$ $(r_e \geq 10R_C,$ $R_B \geq 10\beta r_e)$
Voltage-divider bias: 	Medium (1 kΩ) $= R_1 \| R_2 \| \beta r_e$	Medium (2 kΩ) $= R_C \| r_o$ $\cong R_C$ $(r_o \geq 10R_C)$	High (−200) $= -\frac{R_C \| r_o}{r_e}$ $\cong -\frac{R_C}{r_e}$ $(r_e \geq 10R_C)$	High (50) $= \frac{\beta(R_1 \| R_2) r_o}{(r_o + R_C)(R_1 \| R_2 + \beta r_e)}$ $= \frac{\beta(R_1 \| R_2)}{R_1 \| R_2 + \beta r_e}$ $(r_e \geq 10R_C)$
Unbypassed emitter bias: 	High (100 kΩ) $= R_B \| Z_b$ $Z_b = \beta(r_e + R_E)$ $\cong R_B \| \beta R_E$ $(R_E \gg r_e)$	Medium (2 kΩ) $= R_C$ (any level of r_o)	Low (−5) $= -\frac{R_C}{r_e + R_E}$ $\cong -\frac{R_C}{R_E}$ $(R_E \gg r_e)$	High (50) $\cong -\frac{\beta R_B}{R_B + Z_b}$
Emitter-follower: 	High (100 kΩ) $= R_B \| Z_b$ $Z_b \cong \beta(r_e + R_E)$ $\cong R_B \| \beta R_E$ $(R_E \gg r_e)$	Low (20 Ω) $= R_E \| r_e$ $\cong r_e$ $(R_E \gg r_e)$	Low ($\cong 1$) $= \frac{R_E}{R_E + r_e}$ $\cong 1$	High (−50) $\cong -\frac{\beta R_B}{R_B + Z_b}$
Common-base: 	Low (20 Ω) $= R_E \| r_e$ $\cong r_e$ $(R_E \gg r_e)$	Medium (2 kΩ) $= R_C$	High (200) $\cong \frac{R_C}{r_e}$	Low (−1) $\cong -1$
Collector feedback: 	Medium (1 kΩ) $= \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_E}}$ $(r_o \geq 10R_C)$	Medium (2 kΩ) $\cong R_C \| R_F$ $(r_o \geq 10R_C)$	High (−200) $= -\frac{R_C}{r_e}$ $(r_e \geq 10R_C)$ $R_F \gg R_C)$	High (50) $= -\frac{\beta R_F}{R_F + \beta R_C}$ $\cong -\frac{R_F}{R_C}$

FORMAT-1B

MODULE-2: Field Effect Transistors (FET)

Definition:

FET is a three terminal electronic device used for variety of applications that match with BJT. In FET, an electric field is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between controlling and controlled quantities.In a Field effect device current is controlled by the action of an electron field, rather than carrier injection.

The main difference between BJT and FET is BJT is a current controlled device while FET is a voltage controlled device. This is shown in fig 1.

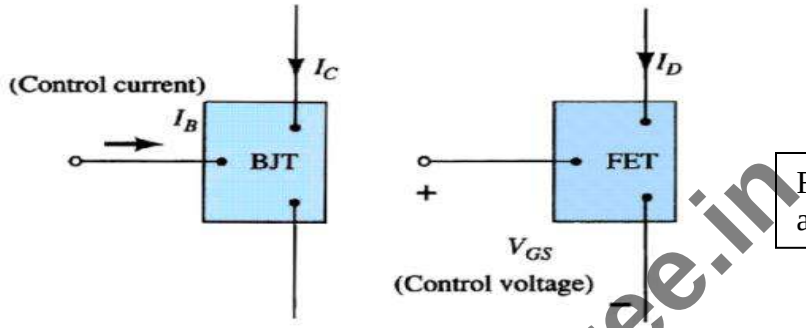


Fig 1: Comparison between BJT and FET

TYPES OF FETS:

1. Junction Field Effect Transistors(JFETs)
2. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

JUNCTION FIELD EFFECT TRANSISTORS(JFETS):

JFET is a unipolar device as conduction in the device is dependent on either electrons or holes. Accordingly there are two types of JFET; namely: n-Channel JFET and p-Channel JFET.

Features of FET:

- FET is a voltage controlled device.
- FET is a unipolar device.
- FET has high input impedance
- AC voltage gain of JFET is low
- FET has higher temperature stability.
- FET are small in size and hence are useful in ICs.

CONSTRUCTION AND CHARACTERISTICS OF N-CHANNEL JFET:

The basic construction of the n-channel JFET is as shown in fig 2. The major part of the structure is the n-type material which forms the channel between embedded layers of p-

type material. The top of the n-type channel is connected through an ohmic contact to a terminal referred to as the drain(D), where as the lower end of the material is connected through an ohmic contact referred to as source(S). The 2 p-type materials are connected together to the gate (G) terminal. In the absence of any applied potentials , JFET has 2 p-n junctions under no bias condition. As a result, depletion region is formed at each junction.

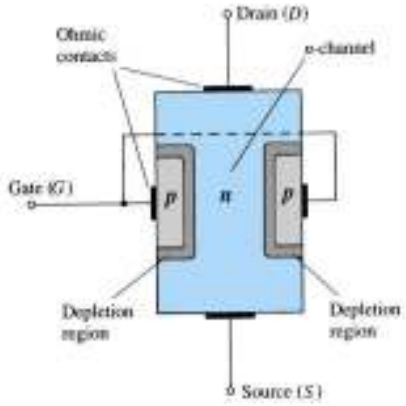
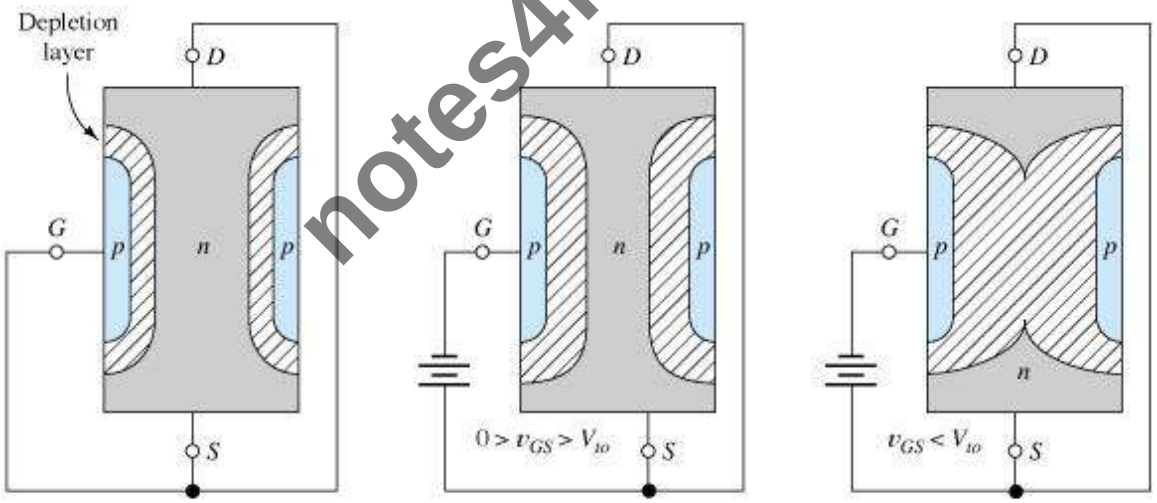


Fig 2 Construction of n-channel JFET

OPERATION:

Fig 3 shows the working of n-channel JFET for different gate-source voltage (V_{GS}) and drain to source voltage (V_{DS}) = 0V.



(a) Bias is zero and depletion layer is thin; low-resistance channel exists between the drain and the source

(b) Moderate gate-to-channel reverse bias results in narrower channel

(c) Bias greater than pinch-off voltage; no conductive path from drain to source

Fig 3: Operation of n-channel JFET

Case i: V_{GS} = 0 and V_{DS} = 0

- Under zero bias condition depletion region around the p-n junction is thin and thus exhibits low channel resistance.

Case ii: V_{GS} = 0 and V_{DS} = + small voltage.

The gate and source are at the same potential and the instant the voltage VDS is applied the electrons in the n-channel are drawn towards the drain terminal establishing drain current (ID).

Due to reverse biasing of the p-n junction for the length of the channel results in gate current = 0.

As VDS is increased further, the drain current increases. When VDS = VP, the depletion region widens causing reduction in the channel width. The reduced path of conduction causes the resistance to increase and the current saturates. When VDS is further increased, the two deletion regions touch resulting in pinch-off condition. The drain characteristics (plot of ID vs VDS for VGS = constant is as shown in fig 4.

Case iii: V_{GS} = -ve voltage and V_{DS} = + small voltage.

The effect of applied reverse bias on gate and source widens the depletion regions around the p-n junctions but at the lower levels of VDS. The resulting saturation level for ID is reduced and will continue to decrease as VGS is made more and more negative. The drain characteristics is as shown in fig 5 for different values of VGS. When VGS = -VP, pinch-off condition occurs resulting in ID = 0. VP is called pinch-off voltage.

The region to the left of pinch off locus is called ohmic region and the region to the right of pinch-off locus is saturation region. This region of JFET is employed for linear amplifiers. In ohmic region JFET can be employed as a variable resistor. The resistance is controlled by VGS. As VGS becomes more and more negative , the slope of the characteristics becomes more and more horizontal indicating increasing resistance level.

The resistance is given by the equation 1.

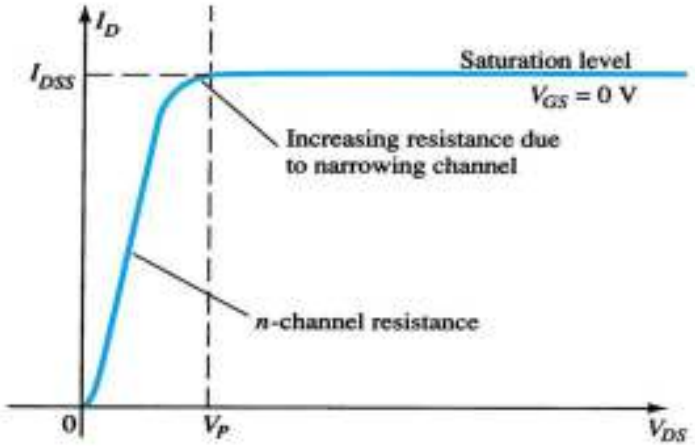


Fig 4 : Drain characteristics of n-channel JFET for VGS = 0V.

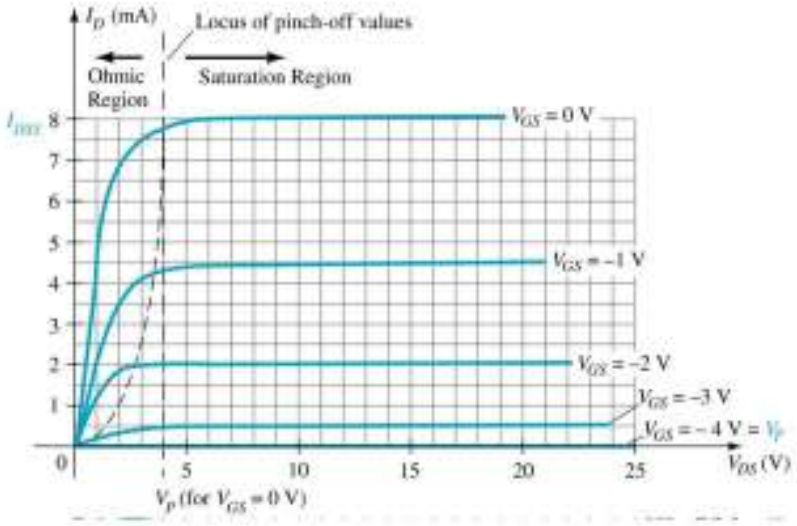


Fig 5 :Drain characteristics of JFET for different V_{GS} values.

TRANSFER CHARACTERISTICS OF N-CHANNEL JFET:

Transfer characteristics are a plot of I_D as a function of V_{GS} with V_{DS} as constant. Shockley Equation as in equation 1 is used to plot transfer characteristics.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \text{---------- Eqn (1)}$$

I_D depends on V_{GS} in a non-linear manner. As a result, FET's are often referred to square law devices. Using the drain characteristics on the right of Y-axis, we can draw a horizontal line from the saturation region of the curve denoted as V_{GS} = 0V to the I_D axis. The resulting current level for both the graphs is I_{DSS}.
When V_{GS} =V_P, the drain current is 0mA, defining another point on transfer curve. Transfer curve is a direct transfer from input to output variables. Transfer characteristics are a parabolic curve as shown in fig 6.

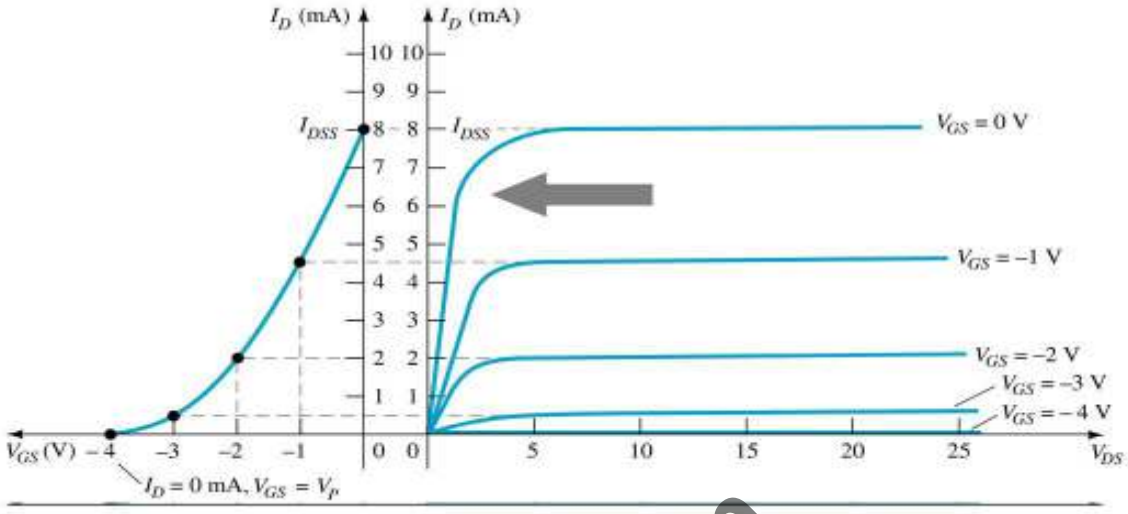


Fig 6: Transfer characteristics from drain characteristics

TRANSFER CHARACTERISTICS: SHORT-HAND METHOD

Transfer characteristics can also be obtained by applying following conditions to schokley's equation (1).

Condition1: VGS = 0

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Therefore $I_D = I_{DSS}$.

Condition 2:$V_{GS} = V_P$

Therefore from equation 1 $I_D = 0$mA.

Condition 3: $V_{GS} = V_P/2$

Therefore from equation 1,$ID = IDSS(1 - \frac{1}{2})^2$

$I_D = I_{DSS}/4$

Condition 4: $I_D = I_{DSS}/2$

From eq(1) ,$VGS = VP(1 - \sqrt{ID/IDSS})$

$$VGS = VP(1 - \sqrt{0.5})$$
$$VGS = 0.3VP$$

Points are marked for these conditions of VGS and ID and the co-ordinates are joined using smooth curve.

CONSTRUCTION AND CHARACTERISTICS OF P-CHANNEL JFET:

The basic construction of the p-channel JFET is as shown in fig 2. The major part of the structure is the p-type material which forms the channel between embedded layers of p-type material. The top of the p-type channel is connected through an ohmic contact to a terminal referred to as the drain(D), where as the lower end of the material is connected through an ohmic contact referred to as source(S). The 2 n-type materials are connected together to the gate (G) terminal. In the absence of any applied potentials , JFET has 2 p-n junctions under no bias condition. As a result, depletion region is formed at each junction.

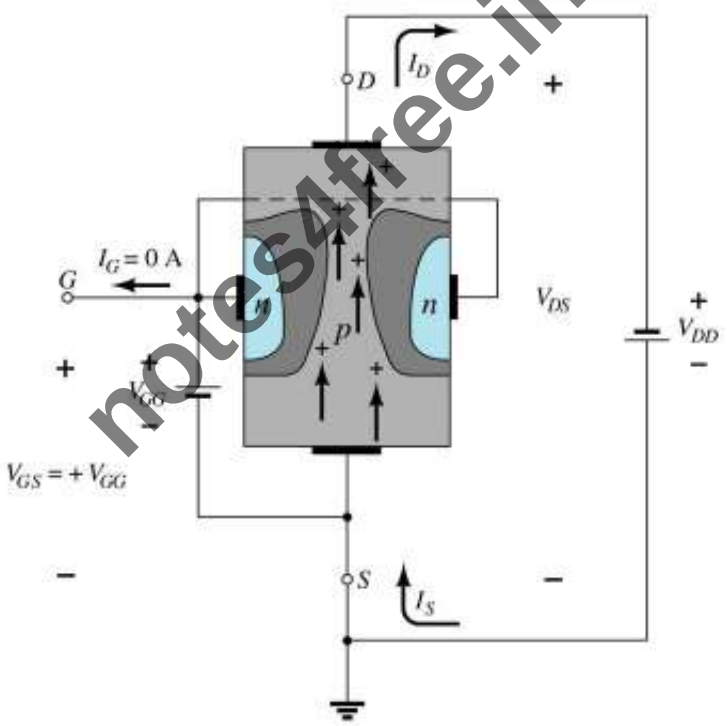


Fig 7 Construction of n- channel JFET

OPERATION OF P-CHANNEL JFET:

Case i: V_{GS} = 0 and V_{DS} = 0

- Under zero bias condition depletion region around the p-n junction is thin and thus exhibits low channel resistance.

Case ii: V_{GS} = 0 and V_{DS} = -ve small voltage.

The gate and source are at the same potential and the instant the voltage VDS is applied the holes in the p-channel are drawn towards the drain terminal establishing drain current (ID).

Due to reverse biasing of the p-n junction for the length of the channel results in gate current = 0.

As VDS is increased further, the drain current increases. When VDS = -VP, the depletion region widens causing reduction in the channel width. The reduced path of conduction causes the resistance to increase and the current saturates. When VDS is further increased, the two deletion regions touch resulting in pinch-off condition. The drain characteristics (plot of ID vs VDS for VGS = constant is as shown in fig 8).

Case iii: V_{GS} = +ve voltage and V_{DS} = -ve small voltage.

The effect of applied reverse bias on gate and source widens the depletion regions around the p-n junctions but at the lower levels of VDS. The resulting saturation level for ID is reduced and will continue to decrease as VGS is made more and more positive. The drain characteristics are as shown in fig 8 for different values of VGS. When VGS = -VP, pinch-off condition occurs resulting in ID = 0. VP is called pinch-off voltage.

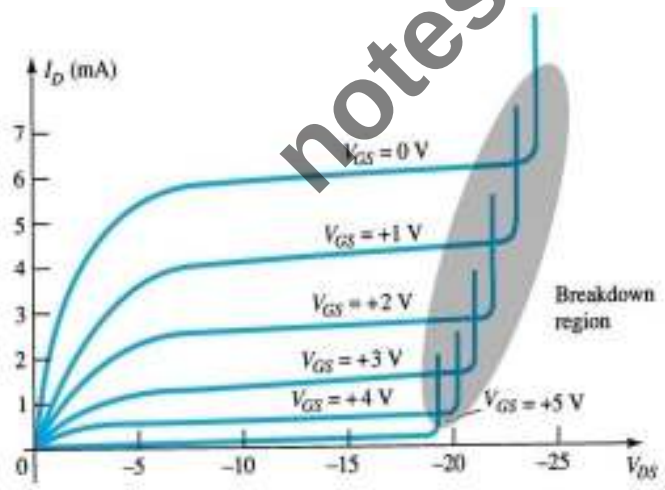


Fig 8: Drain Characteristics of p-channel JFET

Symbols of JFET:
Fig 9(a) and 9 (b) shows the symbols of n-channel and p- channel FET respectively.

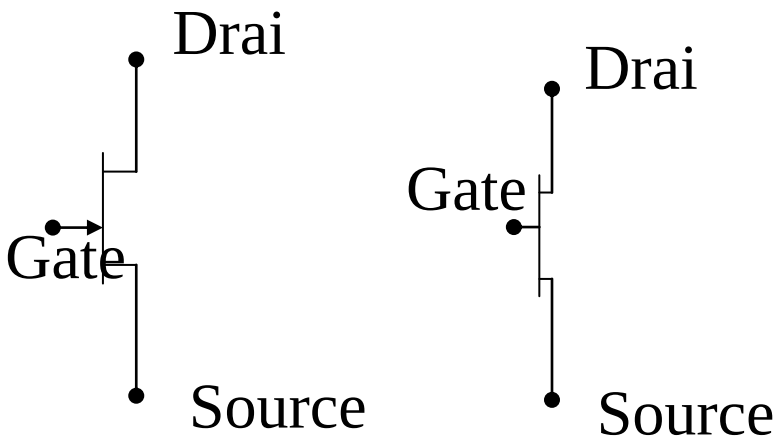


Fig 9: JFET Symbols.
9(a) n-Channel JFET 9(b)p-channel JFET

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs):

MOSFET is a type of Field Effect Transistor in which majority charge carriers flow in the channel. The width of the channel is controlled by an electrode called gate. Channel width determines how well the device conducts.

MOSFETS are useful in high-speed switching circuits and in Integrated Circuits.

There are two types of MOSFET's:

(i) Depletion type MOSFET
(ii) Enhancement type MOSFET

DEPLETION TYPE MOSFET:

Depletion-type MOSFETs are further classified as

(i) N-channel D-type MOSFET
(ii) P-Channel D-type MOSFET

N-CHANNEL DEPLETION TYPE MOSFET:

The basic construction of the n-channel depletion type MOSFET is as shown in fig (10). A slab of p-type material is formed from a Si base and is referred to as the substrate. The source and drain terminals are connected through metallic contacts to n-doped regions linked by a n-channel. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin SiO_2 layer. The presence of SiO_2 layer accounts for very high input impedance of the device. The input impedance of MOSFET is higher than JFET.

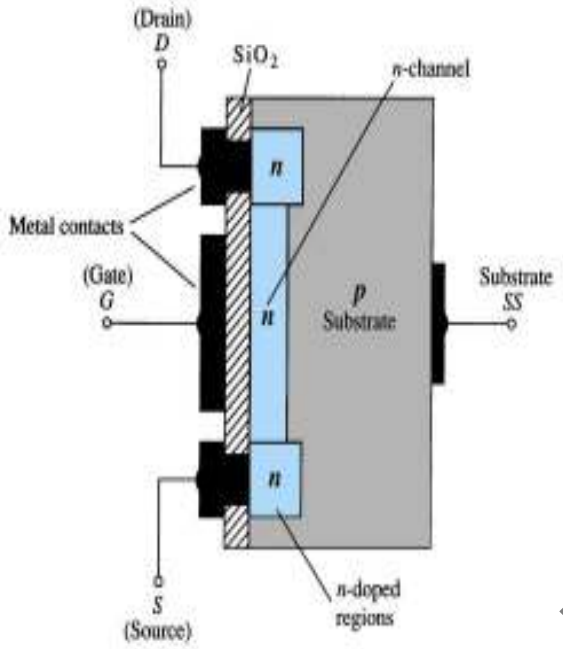


Fig 10: Construction n-Channel Depletion type MOSFET.

A small n layer is implanted in the region below SiO_2 to create n-channel. The insulating layer between gate and the channel has resulted in another name for the device : Insulated-gate FET or IGFET.

OPERATION OF N-CHANNEL DEPLETION MODE MOSFET:

Case i: V_{GS} = 0 and V_{DS} = +ve voltage

Since drain is positive with respect to source, the free electrons are attracted from source to drain to constitute drain current I_D. The drain characteristics and transfer characteristics of depletion mode MOSFET is as shown in fig 11.

Case ii: V_{GS} = -ve Voltage and V_{DS} = +ve small voltage

The negative potential at the gate will cause the electrons to move towards p-type substrate as charges repel while holes from p-type substrate are attracted toward gate. Depending on the magnitude of negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, higher is the rate of recombination. The resulting level of I_D is reduced with the increasing levels og negative bias for VGS as in fig11.

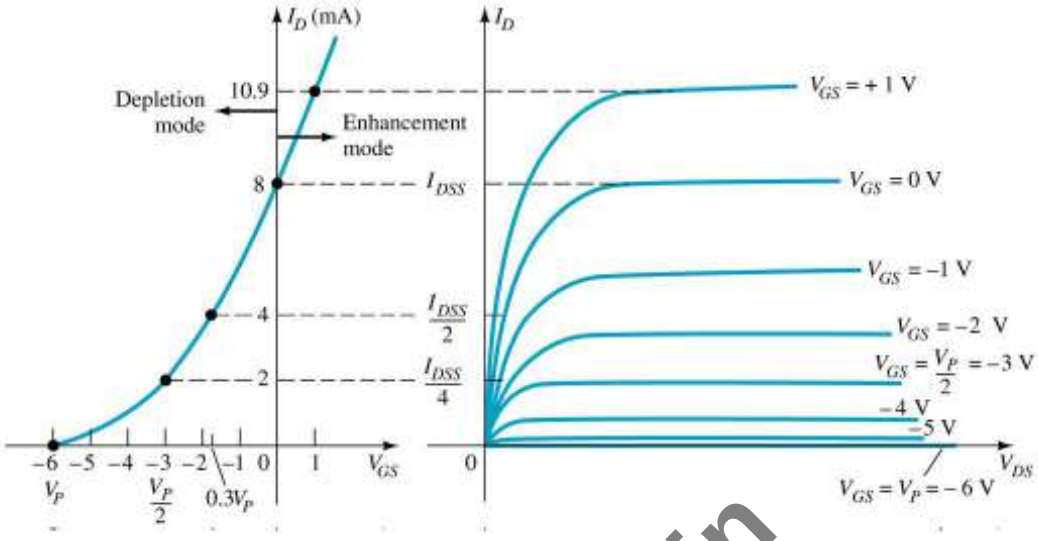


Fig11(a) Transfer Characteristics Fig 11(b) Drain Characteristics.

Case iii: V_{GS} = +ve Voltage and V_{DS} = +ve small voltage

For positive values of V_{GS}, the +ve gate will draw additional electrons from p-type substrate as minority charge carriers are attracted towards gate. New carriers are generated due to collisions and I_D will increase at a rapid rate. Thus, application of $+V_{GS}$ has enhanced the level of free carriers in the channel compared to V_{GS} = 0V. The region of +ve gate voltage on the drain or transfer characteristics is referred as enhancement region. The region between the cut-off and the saturation level of I_{DSS} is refereed as the depletion region.

Transfer characteristics are a plot of I_D as a function of V_{GS} with V_{DS} as constant.
Shockley Equation as in equation 2 is used to plot transfer characteristics.

---------- Eqn (2) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Also, Short hand method can be used to plot transfer characteristics curve.

Condition1: V_{GS} = 0, Hence from eq(2),

$I_D = I_{DSS}$.

Condition 2:$V_{GS} = V_P$

Therefore from equation 2 I_D = 0mA.

Condition 3: $V_{GS} = V_P/2$

Therefore from equation 2,$ID = IDSS(1 - \frac{1}{2})^2$

$I_D = I_{DSS}/4$

Condition 4: $I_D = I_{DSS}/2$

From eq(1) ,$VGS = VP(1 - \sqrt{ID/IDSS})$

$$VGS = VP(1 - \sqrt{0.5})$$
$$VGS = 0.3VP$$
$$VGS = 0.3VP$$

Points are marked for these conditions of VGS and ID and the co-ordinates are joined using smooth curve.

P-CHANNEL DEPLETION TYPE MOSFET:

The basic construction of the p-channel depletion type MOSFET is as shown in fig (12a). A slab of n-type material is formed from a Si base and is referred to as the substrate. The source and drain terminals are connected through metallic contacts to p-doped regions linked by a p-channel. The gate is also connected to a metal contact surface but remains insulated from the p-channel by a very thin SiO_2 layer. The presence of SiO_2 layer accounts for very high input impedance of the device. The input impedance of MOSFET is higher than JFET.

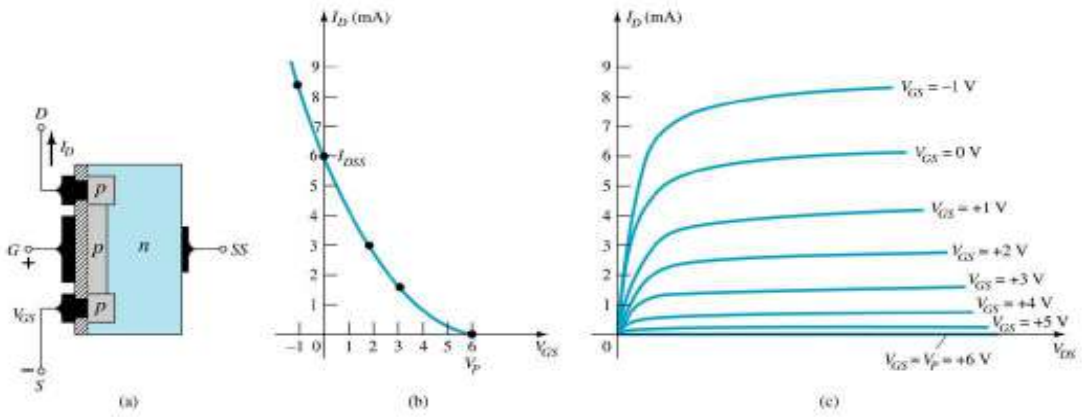


Fig 12: (a) Construction (b) Transfer Characteristics (c) Drain characteristics

OPERATION OF P-CHANNEL DEPLETION MODE MOSFET:

Case i: V_{GS} = 0 and V_{DS} = -ve voltage

Since drain isnegative with respect to source, the holes are attracted from source to drain to constitute drain current I_D. The drain characteristics and transfer characteristics of depletion mode MOSFET is as shown in fig 12(c) and (b) respectively.

Case ii: V_{GS} = +ve Voltage and V_{DS} = -ve small voltage

The positive potential at the gate will cause the holes to move towards n-type substrate as charges repel while electrons from n-type substrate are attracted toward gate. Depending on the magnitude of positive bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of holes in the p-channel available for conduction. The more positive the bias, higher is the rate of recombination. The resulting level of I_D is reduced with the increasing levels or positive bias for V_{GS} as in fig12(c).

Case iii: V_{GS} = -ve Voltage and V_{DS} = -ve small voltage

For positive values of V_{GS}, the -ve gate will draw additional holes from n-type substrate as minority charge carriers are attracted towards gate. New carriers are generated due to

collisions and I_D will increase at a rapid rate. Thus, application of $-V_{GS}$ has enhanced the level of free carriers in the channel compared to $V_{GS} = 0V$.

Transfer characteristics are a plot of I_D as a function of V_{GS} with V_{DS} as constant. Shockley Equation as in equation 2 is used to plot transfer characteristics.

---------- Eqn (3) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Also, Short hand method can be used to plot transfer characteristics curve.

Condition1: $V_{GS} = 0$, Hence from eq(3),

$I_D = I_{DSS}$.

Condition 2:$V_{GS} = V_P$

Therefore from equation 2 $I_D = 0mA$.

Condition 3: $V_{GS} = V_P/2$

Therefore from equation 2,$ID = IDSS(1 - \frac{1}{2})^2$

$I_D = I_{DSS}/4$

Condition 4: $I_D = I_{DSS}/2$

From eq(1) ,$VGS = VP(1 - \sqrt{ID/IDSS})$

$$VGS = VP(1 - \sqrt{0.5})$$
$$VGS = 0.3VP$$
$$VGS = 0.3VP$$

Points are marked for these conditions of V_{GS} and I_D and the co-ordinates are joined using smooth curve.

SYMBOLS OF DEPLETION TYPE MOSFET

Fig 13 shows the symbols of n-channel and p-channel Depletion mode MOSFET.

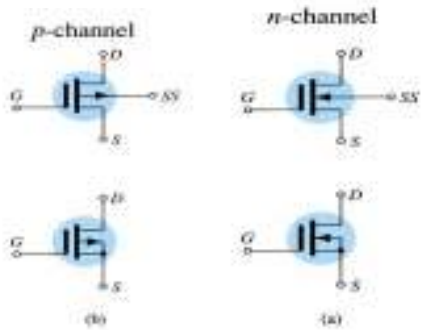


Fig 13 (a) n-channel depletion type MOSFET (b) p-channel depletion type MOSFET

N-CHANNEL ENHANCEMENT-MODE MOSFET (E-MOSFET):

The construction of n-channel enhancement mode MOSFET is as shown in fig 14. The starting material is a p-type substrate into which highly doped n-regions are diffused to form source and drain regions. A layer of SiO_2 is grown allover the p-type substrate and is etched to create window for n-diffusion. The source and drain terminals are taken out through metallic contacts to n-doped regions as shown in fig 14. Metal is deposited on SiO2 to create Gate. The presence of SiO2 between gate and p-substrate provides electrical isolation between the two regions. No channel exists between source and drain in E-MOSFET.

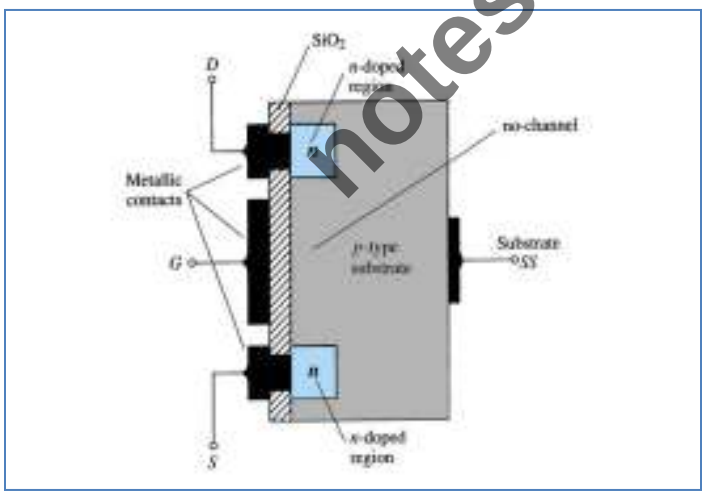


Fig 14: Construction of n-channel E-MOSFET

OPERATION OF N-CHANNEL E-MOSFET:

Case i: V_{GS} = 0 and V_{DS} = +ve voltage

The application of drain to source voltage while gate and source are shorted will cause no ID to flow as no channel exists for this condition.

Case ii: V_{GS} = +ve Voltage and V_{DS} = +ve small voltage

When gate is made positive with respect to source, electrons are attracted towards the gate but holes are repelled back into p-type substrate. Since the region under the gate is p-type substrate, the positive voltage on gate causes holes which are majority charge carriers in p-type substrate to repel and move towards substrate. A positive V_{GS} and positive V_{DS} causes the two pn junctions to be reverse biased and depletion region is formed. Now the device is said to be in depletion mode. The positive V_{GS} also causes electrons to be attracted towards the gate. Now, device is said to be in accumulation mode. Since the region below the gate was p-substrate and accumulation of electrons has caused the type to change to n-type. Thus the device is said to be in inversion mode as shown in fig 15. A positive V_{GS} has caused a thin layer of negative chargesto be formed in the substrate under the gate. Thus, channel is said to be created. The value of V_{GS} which causes channel to be formed under the gate is called threshold voltage(V_T). A small I_D flows. When V_{GS} is increased above V_T, conductivity of the channel is enhanced and thus pulling more electrons into the channel. When $V_{GS}<V_T$, there is no channel. Since channel is formed by the application of $+V_{GS}$, the type of MOSFET is Enhancement type. As V_{GS} is increased further, higher level of I_D flows as shown in fig 16. A positive V_{GS} cause potential drop across the channel. For large V_{DS} this voltage may not be sufficient to invert the channel near the drain end there by causing drain current to saturate. The channel is said to be pinched off. I_D flows due to diffusion.

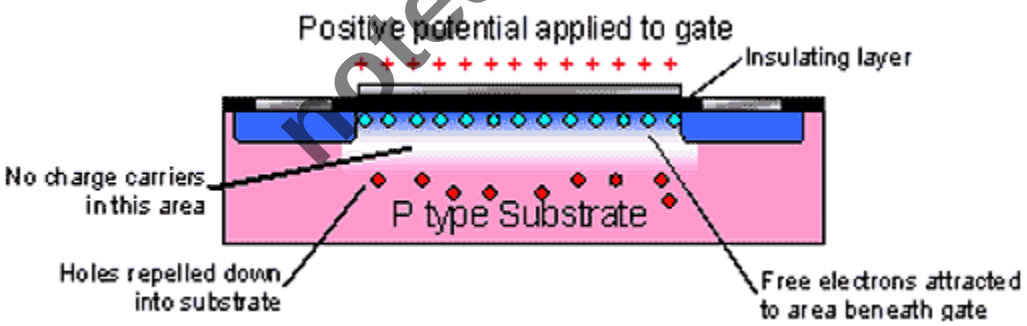


Fig 15: Formation of Inversion layer

TRANSFER CHARACTERISTICS OF N-CHANNELE-MOSFET:

The transfer characteristics of n-channel E-MOSFET is as shown in fig 16. For VGS >VT, the relationship between drain current and VGS is nonlinear and is given by eqn 4.

$$ID = K(VGS - VT)^2 \qquad \text{----------Eq 4}$$

Where K is a constant and is a function of the construction of the device as given by Eqn 5.

$$K = \frac{ID(ON)}{(VGS(ON) - VT)^2} \qquad \text{----------Eq 5}$$

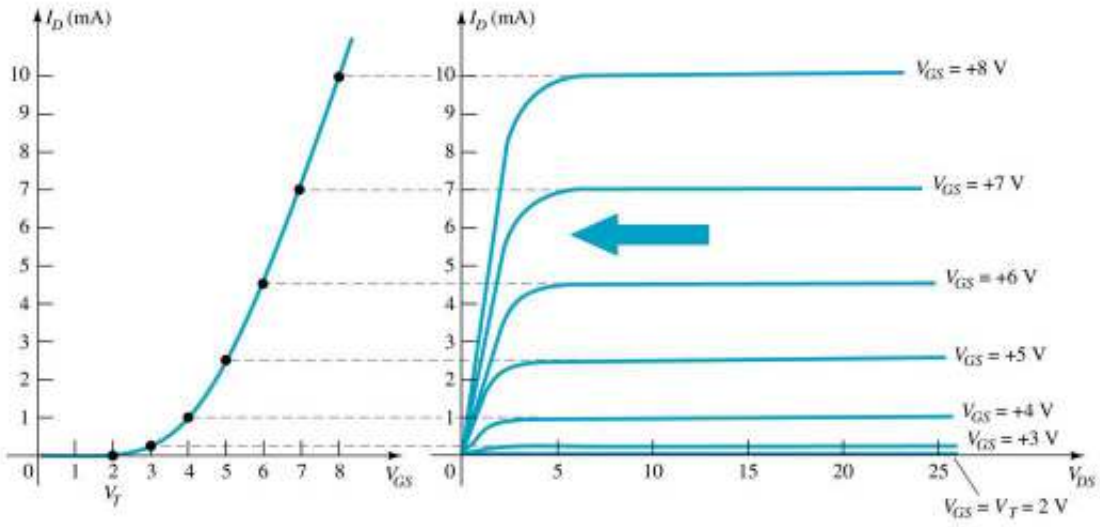


Fig16: Transfer Characteristics Drain Characteristics

Thus I_D increases steadily when $V_{GS} > V_T$ and I_D is zero when $V_{GS} < V_T$.

p-CHANNELENHANCEMENT-MODE MOSFET (E-MOSFET):

The construction of p-channel E-MOSFET is opposite to that of n-channel E_MOSFET. Substrate is of n-type and source, drain are of p-type as in fig17(a). The voltage polarities and current directions are reversed in p-channel E-MOSFET. The drain and transfer characteristics of p-channel E-MOSFET are as shown in Fig 17 (c) and (b) respectively.

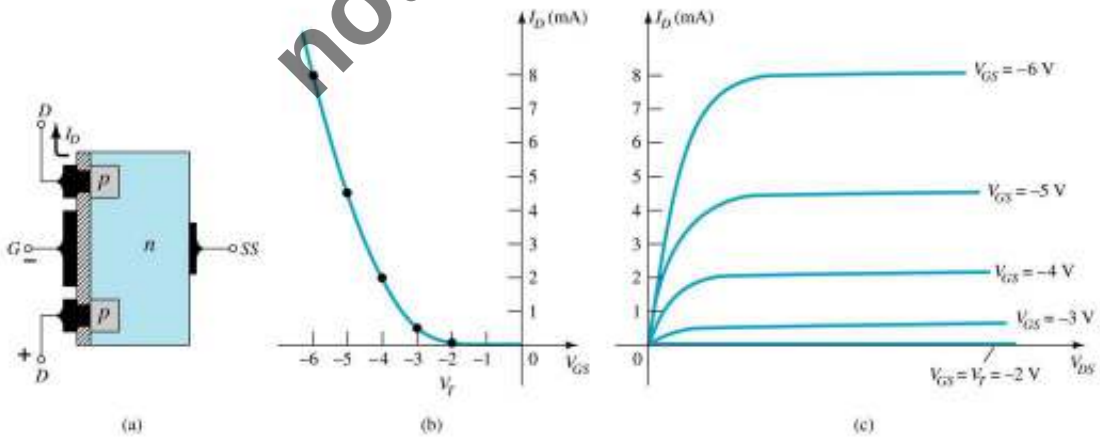


Fig 17: (a) Construction (b) Transfer Characteristics (c) Drain Characteristics

OPERATION OF P-CHANNEL E-MOSFET:

Case i: V_{GS} = 0 and V_{DS} = -ve voltage

The application of drain to source voltage while gate and source are shorted will cause no ID to flow as no channel exists for this condition.

Case ii: V_{GS} = -ve Voltage and V_{DS} = -ve small voltage

When gate is made negative with respect to source, holes are attracted towards the gate but electrons are repelled back into n-type substrate. Since the region under the gate is n-type substrate, the negative voltage on gate causes electrons which are majority charge carriers in n-type substrate to repel and move towards substrate. A negative V_{GS} and negative V_{DS} causes the two pn junctions to be reverse biased and depletion region is formed. Now the device is said to be in depletion mode. The negative V_{GS} also causes holes to be attracted towards the gate. Now, device is said to be in accumulation mode. Since the region below the gate was n-substrate and accumulation of holes has caused the type to change to p-type. Thus the device is said to be in inversion mode .A negative V_{GS} has caused a thin layer of positive charges to be formed in the substrate under the gate. Thus, channel is said to be created. The value of V_{GS} which causes channel to be formed under the gate is called threshold voltage(V_T). A small I_D flows. When V_{GS} is decreasedbelow V_T, conductivity of the channel is enhanced and thus pulling more electrons into the channel. When $V_{GS}>V_T$, there is no channel. Since channel is formed by the application of $-V_{GS}$, the type of MOSFET is Enhancement type. The drain characteristics are as shown in fig 17 (c).

TRANSFER CHARACTERISTICS OF P-CHANNEL E-MOSFET:

The V_{GS} is negative and I_D flows in opposite direction. The transfer characteristics of p-channel E-MOSFET is as shown in fig 17(b). I_D increases steadily with V_{GS}.

E-MOSFET SYMBOLS:

Fig 18 (a) and 18(b) shows the symbols of n-channel and p-channel E-MOSFET.

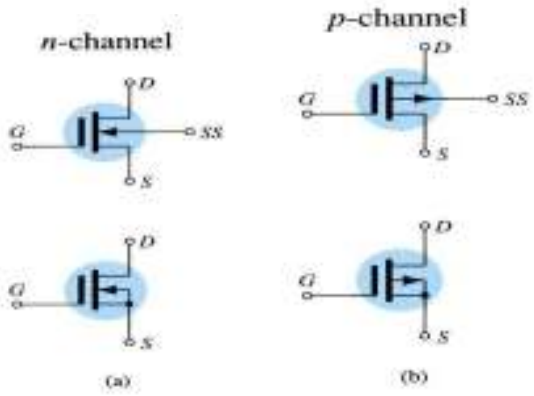


Fig 18: E-MOSFET Symbols

FET CONFIGURATION:

The three types of FET configuration are:

(i) Common Source (CS) Configuration
(ii) Common Drain (CD) Configuration
(iii)Common Gate (CG) Configuration

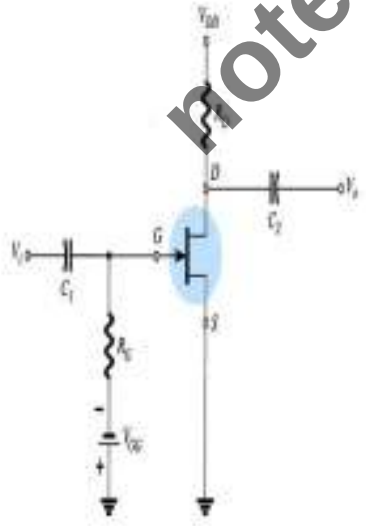
FET BIASING:
Biasing is done to establish proper levels of DC voltages and currents for desired region of operation. It establishes Q-point.
TYPES OF BIASING:

(i) Fixed Bias
(ii) Self Bias
(iii)Voltage divider Bias

Voltage divider bias most widely used biasing technique in amplifiers.

FET AS AN AMPLIFIER:

Fig.19 Shows Common Source Circuit. The Voltage V_{GG} provides the necessary reverse-bias between gate and source of JFET. The signal to be amplified is V_S. The transfer Characteristics of JFET is as shown in Fig. 20. A DC load line is drawn on the characteristics. The point of intersection of DC load line on Transfer characteristics for specific V_{GS} is called Q point. Let Q point be situated at the middle of DC load line.



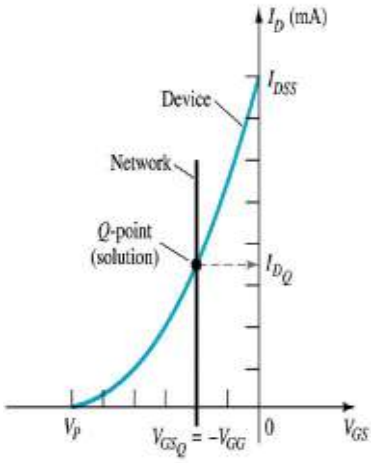


Fig 19: CS Amplifier with Fixed Bias

Fig 20: Locate Q-Point

The instantaneous V_{gs} is
$V_{gs}=V_S-V_{GG}$ ----- (6)
Both I_D and V_{DS} can be considered as sinusoid superimposed on the DC values.

Then V_{GS}=-V_{GG}+V_{gs} ----- (7)

I_D=i_d+I_{DQ}

V_{OUT} =V_{DS} =V_{DSQ}+V_{ds} ----- (8)

Since output signal is greater than input signal, amplification has occurred. The magnitude of Voltage gain is the ratio of output voltage to input voltage.

$|A_V|=\frac{V_O}{V_S}$

The selection of Q point at the middle gives undistorted output. If the operating point is located either closer to ohmic region or near pinch-off voltage, the output waveform will be clipped during +Ve or –Ve half cycles. In Common Source circuit, output is 180^0 out of phase with input.

To locate Q point, the following procedure is used

- Plot transfer characteristics
- Draw a vertical line(load line) from VGS = -VGG.
- Intersection of load line with transfer characteristics will give Q point.

Fig 20 shows the position of Q point using the above procedure.

JFET parameters

Transconductance: The change in the Drain Current due to change in Gate to Source voltage is defined as Transconductance 'g_m'.

$g_m=\frac{\Delta I_d}{\Delta V_{GS}}$

We know that, $I_D= I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$ ----- (9)

And $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$

Differentiate Eq. (9) w.r.t V_{GS}

$\frac{\Delta I_D}{\Delta V_{GS}} = I_{DSS} \times 2 \left(1-\frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right)$

$g_m = -\frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$ ----- (10)

Also from Eq. (9) $1-\frac{V_{GS}}{V_P}=\sqrt{\frac{I_D}{I_{DSS}}}$ ----- (11)

Therefore substitute Eq. (11) in Eq. (10),

we get, $g_m = -\frac{2I_{DSS}}{V_P}\sqrt{\frac{I_D}{I_{DSS}}} = -\frac{2}{V_P}\sqrt{\frac{I_D I_{DSS}^2}{I_{DSS}}}$

therefore $g_m = -\frac{2}{V_P}\sqrt{I_D I_{DSS}}$ ----- (12)

when V_{GS}=0, $g_m = g_{mo}$

therefore from Eq. (10), $g_{mo}= -\frac{2I_{DSS}}{V_P}$ ----- (13)

Substitute Eq. (13) in Eq. (10)

we get, $g_m = g_{mo}\left(1-\frac{V_{GS}}{V_P}\right)$

Drain Resistance, r_d: The ratio of change in Drain to Source voltage to change in Drain current is called Drain resistance, r_d with constant V_{GS}.

$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS=constant}}$

r_d determines the output impedance Z_O of the JFET amplifier.

JFET small signal model:

Fig. (21) shows low frequency small signal model for n-channel JFET. The relationship between I_D and V_{GS} is

$\Delta I_D = g_m \Delta V_{gs}$

and hence a current Source is connected from Drain to Source. The input impedance of JFET is high and hence I_G=0. Thus in the small signal model input impedance is representated by open circuit. The output impedance is representated by r_d from Drain to Source.

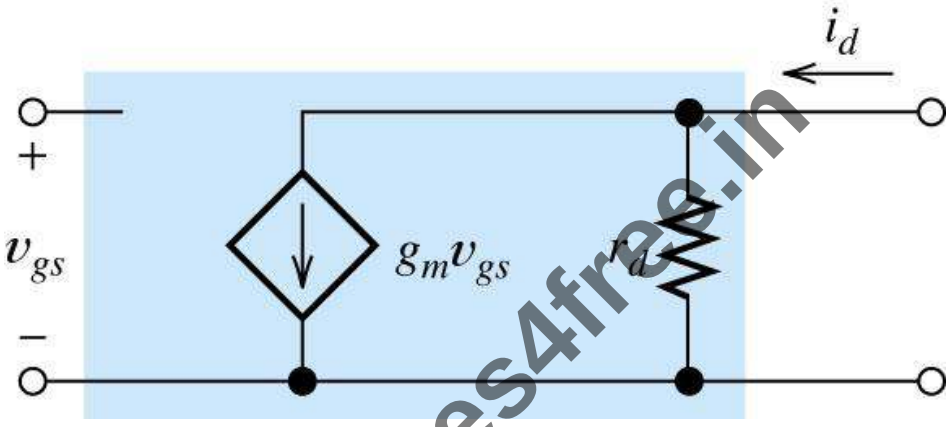


Fig. (21) n-JFET small signal model

Approximate model

Since r_d >> external Drain resistance R_D, r_d can be replaced by open circuit as shown in Fig. (22).

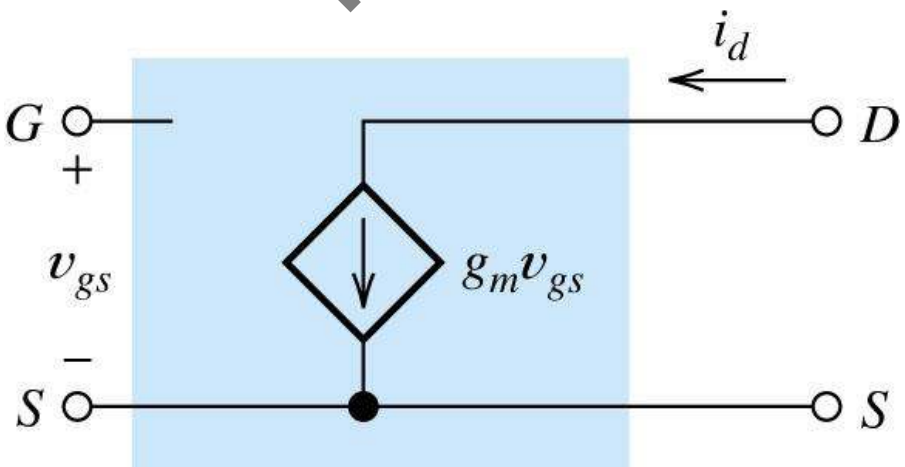


Fig. (22) Approximate small signal model of n-JFET.

COMMON SOURCE (CS) AMPLIFIER WITH FIXED BIASING:

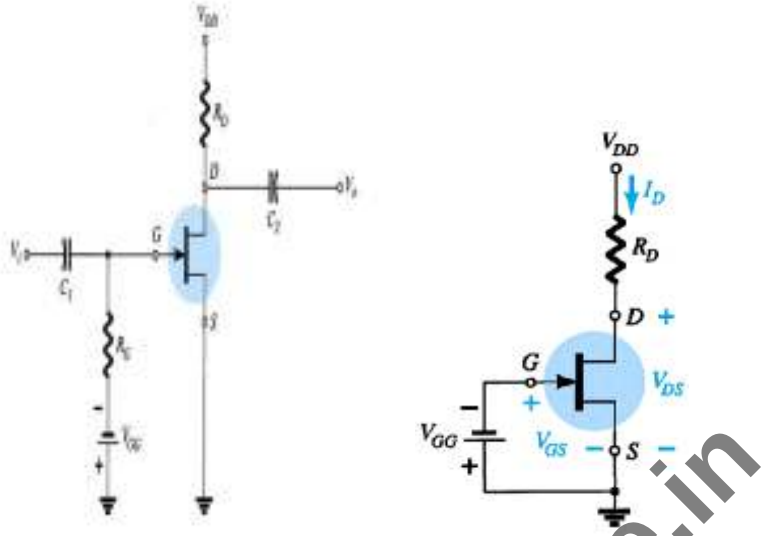


Fig 23: CS Amplifier with Fixed BiasFig 24: DC equivalent Circuit

Fig 23 shows CS amplifier with fixed bias.RG is used to limit current in case VGG is connected with wrong polarity
This would forward bias the gate-source junction causing high currents, which would destroy the transistor
DC Analysis:

Open circuit C_1& C_2 and current through RG i.e. IG=0. Therefore RG is represented by short circuits as shown in Fig. (24)
Apply KVL to the input circuit of Fig. (24)
V_{GG}-V_{GS}=0
V_{GS}=-V_{GG} ----- (14)
Since V_{GG} is constant, V_{GS} is fixed and hence the name fixed bias.
Apply KVL to output circuit
V_{DD}-$I_D R_D$-V_{DS}=0
V_{DSQ}=V_{DD}-$I_D R_D$ ----- (15)
And I_D for fixed bias is I_{DQ}= $I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$
Therefore Q point is $[V_{DS}, I_{DQ}]$

Small signal analysis:

(i) To obtain AC equivalent circuit, short circuit C_1, C_2 and reduce DC voltages to zero.

(ii) Replace JFET by its small signal model to obtain AC equivalent circuit Fig. (25).

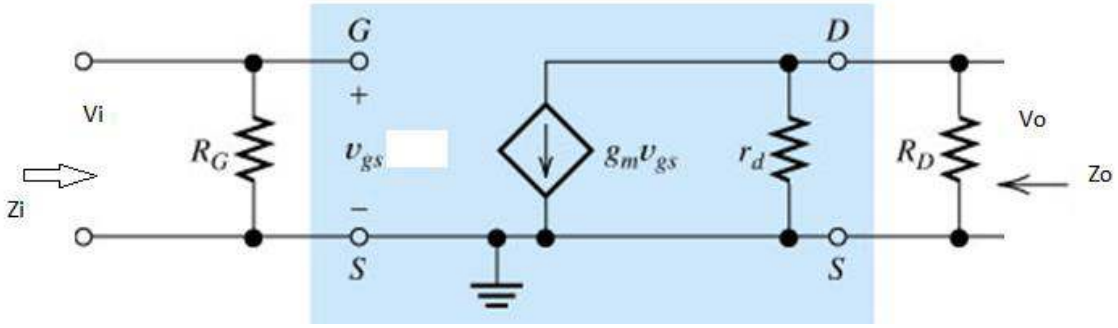


Fig 25: ac equivalent circuit

Z_i: From the circuit, Fig. (25)

$Z_i=R_G$

Zo:

Reduce $V_i=0$, $V_{gs}=0$ therefore $g_mV_{gs}=0$.

$Z_o=R_D \| r_d$

If $r_d >> R_D$, Then $Z_o=R_D$

Voltage gain, A_V:

$A_V = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

From Fig. (25) $V_o = - g_mV_{gs} (r_d \| R_D)$ and $V_i=V_{gs}$

$A_V = - g_mV_{gs} (r_d \| R_D)$

If $r_d >> R_D$, $A_V = - g_m R_D$

The negative sign indicates there is a phase shift of 180^0 between input and output voltages.

COMMON SOURCE (CS) AMPLIFIER WITH SELF BIAS:

Fig 26 shows Common Source amplifier with self bias. Voltage across RS determines gate to source voltage. Dc equivalent circuit is obtained by open circuiting all capacitors as shown in fig 27.

Apply KVL to Fig27,

$-V_{GS}-V_S=0$

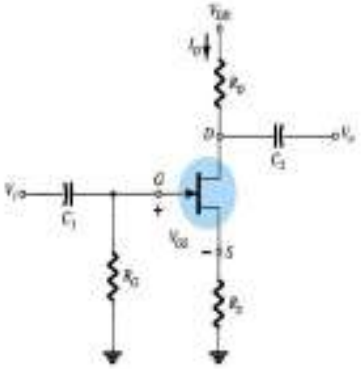
$V_S = -V_{GS}$.

Also, $V_S = I_D R_S$

Therefore, $V_{GS} = -I_DR_S$

Apply KVL to output circuit of fig27,

$V_{DS} = V_{DD} – I_DR_S-I_DR_D$



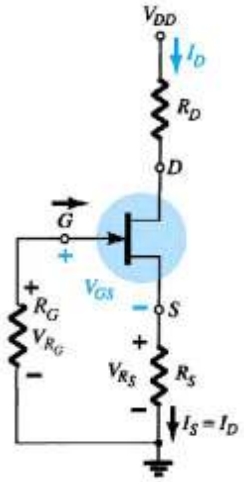


Fig 26. CS amplifier with Self Bias Fig 27 DC equivalent Circuit

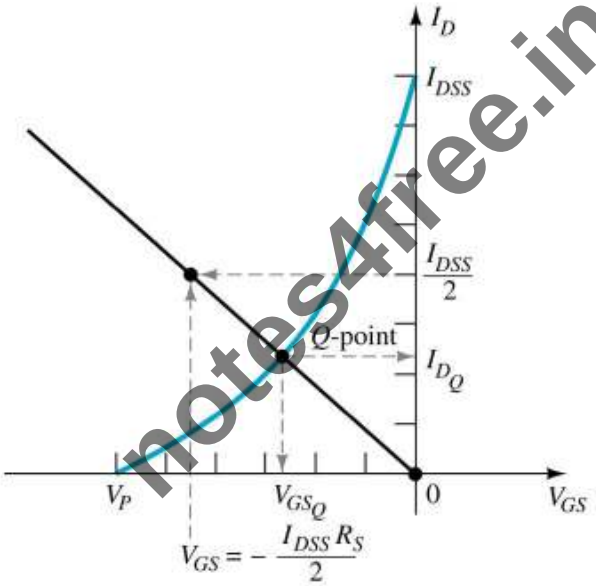


Fig 28 : Q point

Fig 8 shows the location of Q point obtained by following procedure.

- Plot transfer characteristics
- Plot one point of load line at V_{GS} =0, I_D = 0.
- Second point can be obtained by choosing I_D and finding V_{GS}.
- $I_D = I_{DSS}/2$, then

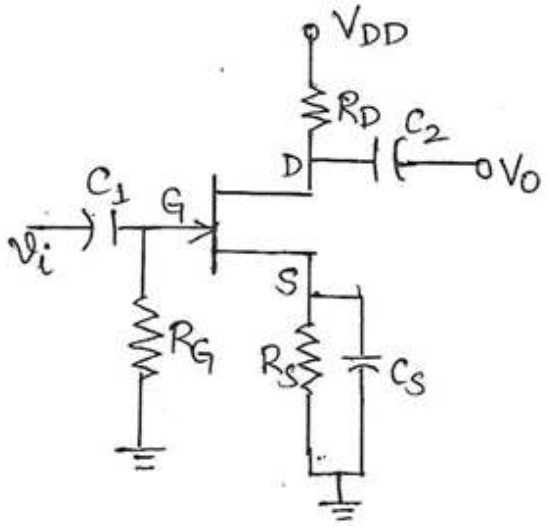
$V_{GS} = -I_D R_S = -I_{DSS}R_S/2$

Join two points to draw DC load line

- Intersection of load line with transfer characteristics will give Q point.

CS amplifier with Self Bias(Bypassed Rs) –ac analysis

Fig 29 shows CS amplifier with Self bias and RS is bypassed by CS. Fig 30 shows ac equivalent Circuit obtained by short circuiting C1,C2,CS.



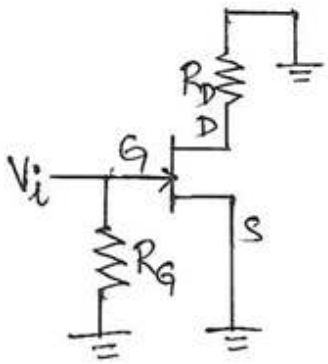


Fig 29: CS amplifier with Self Bias

Fig 30: ac Equivalent Circuit.

Replacing JFET by its equivalent small signal model results in circuit shown in Fig 31.

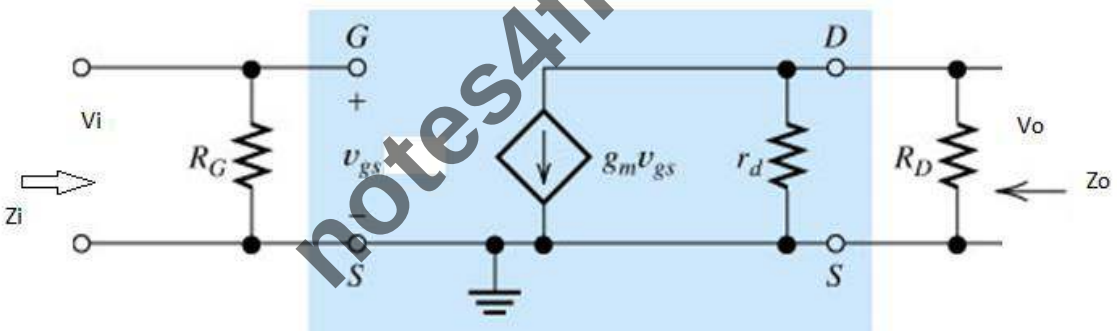


Fig 31: AC equivalent model of CS amplifier with Self bias

Z_i: From the circuit, Fig. (31)

$Z_i = R_G$

Zo:

Reduce $V_i=0$, $V_{gs}=0$ therefore $g_m V_{gs}=0$.

$Z_o = R_D \| r_d$

If $r_d >> R_D$, Then $Z_o = R_D$

Voltage gain, A_V:

$A_V = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

From Fig. (31) $V_o = - g_m V_{gs} (r_d \| R_D)$ and $V_i = V_{gs}$

$A_V = - g_m V_{gs} (r_d \| R_D)$

If $r_d >> R_D$, $A_V = - g_m R_D$

The negative sign indicates there is a phase shift of 180^0 between input and output voltages.

CS amplifier with Self Bias(UnBypassedRs) –ac analysis

Fig 32 shows CS amplifier with self bias but RS is unbypassed. To obtain ac equivalent circuit, c1 and c2 are short circuited as shown in Fig33. Replacing JFET by its equivalent small signal model, we get the circuit shown in fig 34.

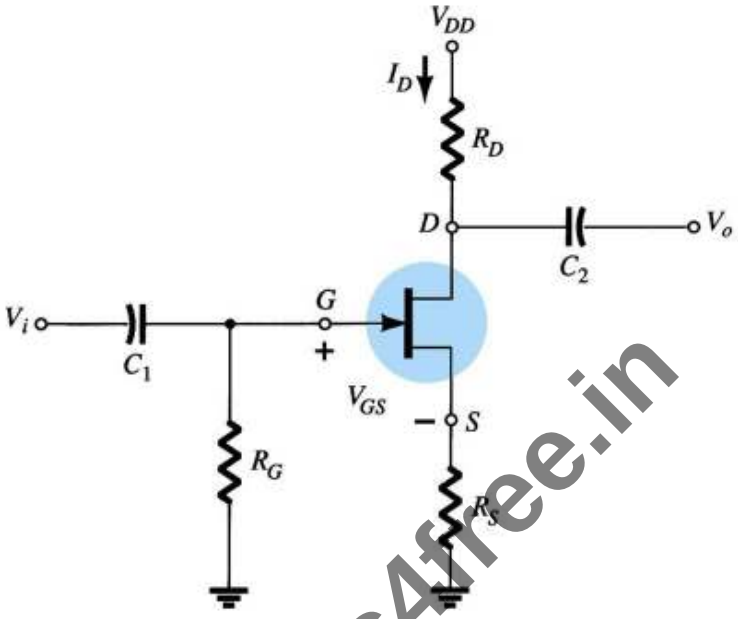


Fig 32: CS amplifier with self bias

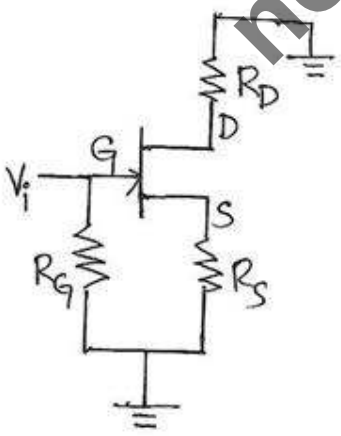


Fig 33: ac Equivalent Circuit

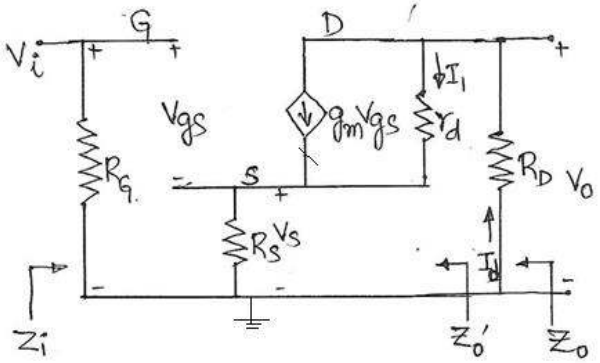


Fig 34: ac Equivalent model

Zi: From Fig 34,
$Z_i = R_G$.

Zo': Output impedance excluding RD.

$Z_o' = V_o/I_d$

Apply KVL to the output circuit of Fig 34,

$V_o = I_1 r_d + I_d R_S$

But, $I_1 = I_d - g_m V_{gs}$.

Therefore, $V_o = (I_d - g_m V_{gs}) + I_d R_S$----------(16)

Apply KVL to the input circuit of Fig 34,

$V_i - V_{gs} - I_d R_S = 0$

$V_{gs} = -I_d R_S + V_i$

For output impedance, $V_i = 0$.

Therefeore, $V_{gs} = -I_d R_S$----------(17)

Substituting Eq (17) in (16)

$V_0 = I_d(r_d + g_m R_S r_d + R_S)$

Therefore, $Z_o' = V_o/I_d = r_d + g_m R_S r_d + R_S$

But, $\mu = g_m r_d$

Therefore, $Z_o' = r_d + R_S(\mu + 1)$----------(18)

Thus, output impedance with unbypassed RS is increased.

Zo: Output impedance considering RD

$Zo = Z_0' || R_D$

Voltage Gain ,AV:

From Fig 34, $V_o = -I_d R_D$----------(19)

Apply KVL to the outer part of Fig 34,

$(I_d - g_m V_{gs}) r_d + I_d R_D + I_d R_S = 0$;----------(20)

Also $V_{gs} = V_i - I_d R_S$----------(21)

Eq (21) in Eq (20)

$I_d = (g_m V_i r_d)/(r_d + g_m R_S r_d + R_s + R_D)$----------(22)

Eq (22) in Eq (19)

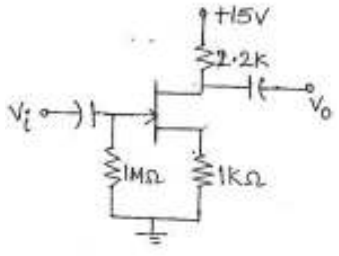
$V_o = (-g_m V_i r_d R_D)/(r_d + g_m R_S r_d + R_S + R_D)$

$A_V = V_o/V_i = -g_m r_d R_D / r_d + g_m R_S r_d + R_S + R_D$

If $r_d >> R_S + R_D$,

$A_V = -g_m R_D/(1 + g_m R_S)$

Example: For the CS amplifier shown, operating point is defined by V_{GSQ} = -2.5V, V_P = -6V and I_{DQ} = 2.5mA with I_{DSS} = 8mA.Calculate g_m, r_d ,Z_i,Z_o and A_V. Take Yos = 20µS



(i) $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$

$g_{mo} = -\frac{2I_{DSS}}{V_P} = \frac{2\times8\times10^{-3}}{6} = 2.67\text{mS}$

$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = \left(1 - \frac{(-2.5V)}{(-6v)}\right) = 1.58\text{mS}$

(ii) $r_d = \frac{1}{Y_{OS}} = \frac{1}{20\times10^{-6}} = 50\text{K}\Omega$

(iii) $Z_i = R_G = 1\text{M}\Omega$

(iv) $Zo = Z_0' || R_D = r_d + R_S(\mu+) || RD = 2163.41\Omega$

(v)

$A_V = \frac{V_o}{V_i} = -g_m r_d R_D / r_d + g_m R_S r_d + R_S + R_D = -1.315.$

CS amplifier with Voltage Divider Bias(Bypassed Rs):

Fig 35 Shows voltage divider bias circuit.

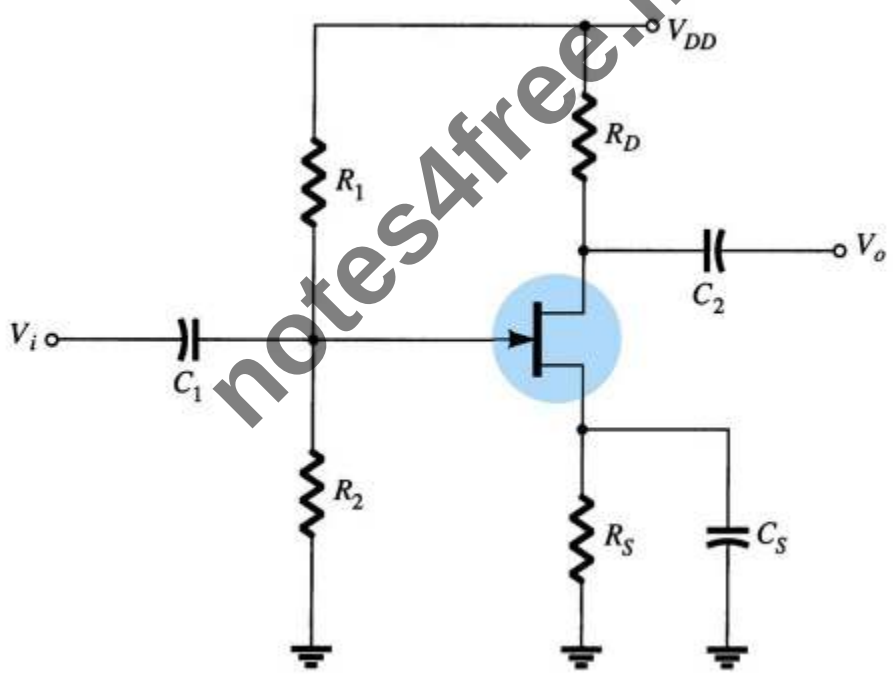


Fig 35: Voltage Divider Bias

DC analysis: Open circuit C1, C2, CS and the resultant circuit is as shown in Fig 36.

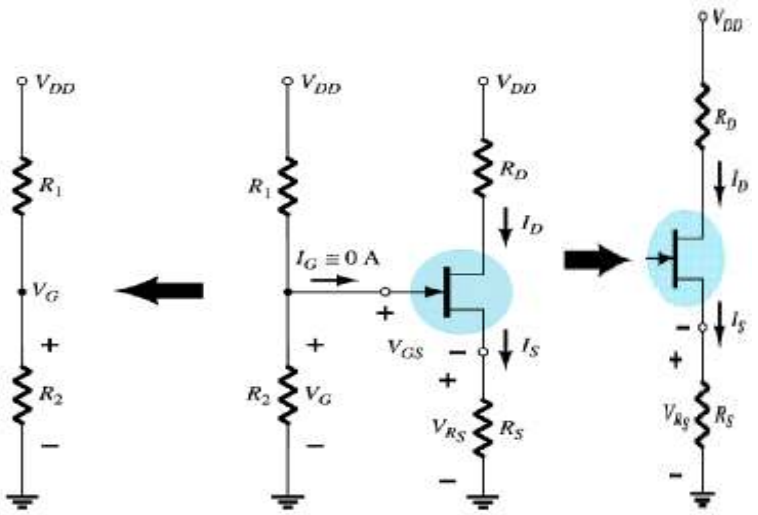


Fig 36: DC Equivalent Circuit.

From Fig 36,

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$-V_G + V_{GS} + I_D R_S = 0$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Fig 37 shows the procedure to fix Q point in voltage divider bias.

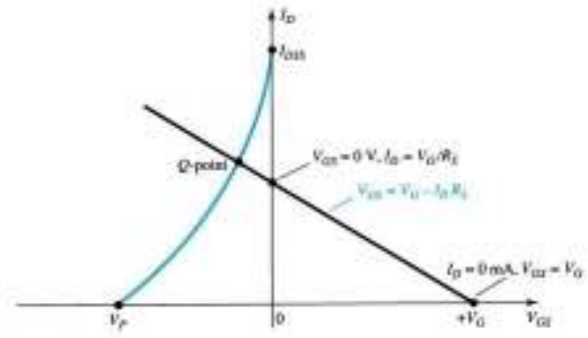


Fig 37: Fixing Q Point.

AC Analysis: AC Equivalent Circuit is obtained by Shorting C1, C2 and CS as shown in Fig 38. Replacing JFET by its small signal model, we get the circuit shown in Fig 39.

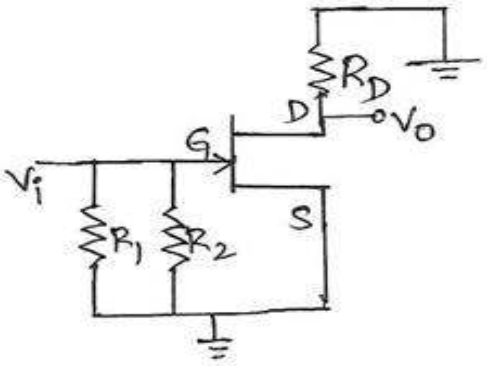


Fig 38: AC Equivalent Circuit

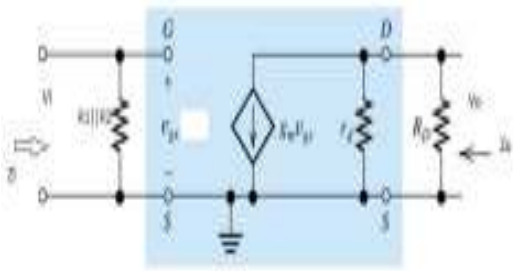


Fig 39: AC Equivalent model

Z_i: From the circuit, Fig. (39)

$Z_i = R_1 \| R_2$

Zo:

Reduce $V_i=0$, $V_{gs}=0$ therefore $g_m V_{gs}=0$.

$Z_o = R_D \| r_d$

If $r_d >> R_D$, Then $Z_o = R_D$

Voltage gain, A_V:

$A_V = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

From Fig. (39) $V_o = - g_m V_{gs} (r_d \| R_D)$ and $V_i = V_{gs}$

$A_V = - g_m V_{gs} (r_d \| R_D)$

If $r_d >> R_D$, $A_V = - g_m R_D$

The negative sign indicates there is a phase shift of 180^0 between input and output voltages.

CS amplifier with Voltage Divider Bias (UnBypassed Rs): ac Analysis

Fig 40 Shows CS voltage divider bias with un-bypassed RS. AC Analysis is obtained by short circuiting C1,C2 and the resultant circuit is shown in Fig 41. Replacing JFET by its equivalent small signal model, we get circuit shown in Fig 42.

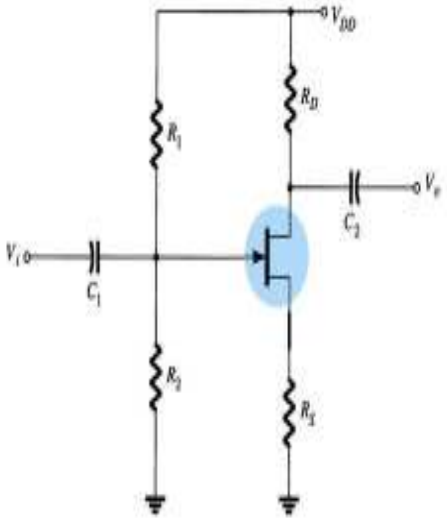


Fig 40: CS amplifier with Voltage Diver Bias

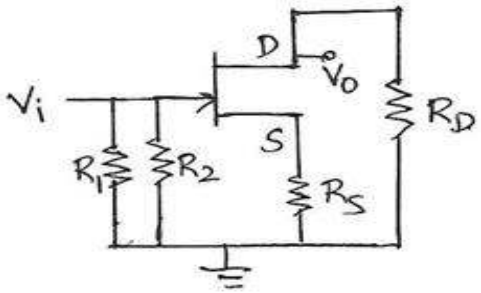


Fig 41: Ac Equivalent Circuit

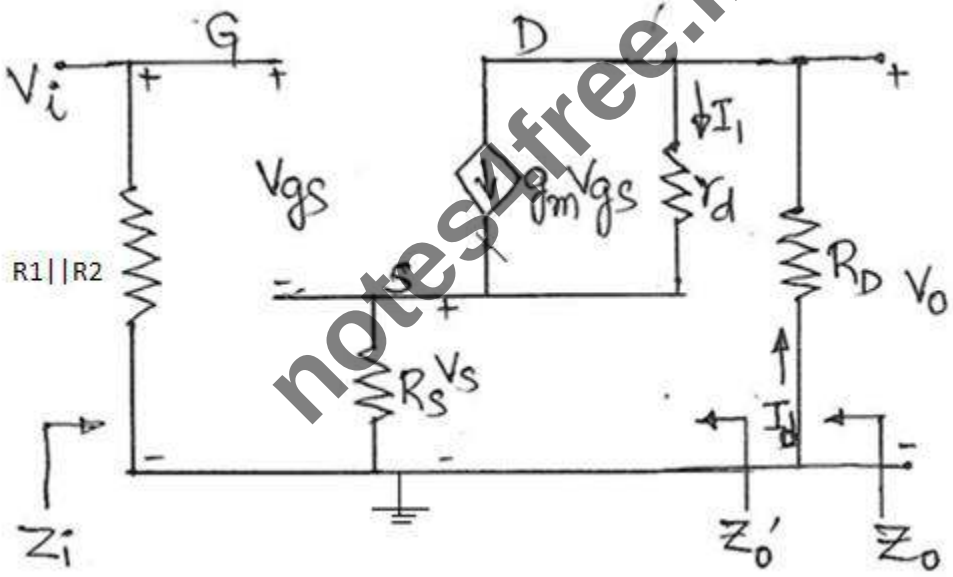


Fig 42: AC equivalent Model

Zi: From Fig 42,

$Z_i = R_1||R_2$.

Zo': Output impedance excluding RD.

$Z_o' = V_o/I_d$

Apply KVL to the output circuit of Fig 42,

$V_o = I_1 r_d + I_d R_S$

But, $I_1 = I_d - g_m V_{gs}$.

Therefore, $V_o = (I_d - g_m V_{gs}) + I_d R_S$----------(23)

Apply KVL to the input circuit of Fig 42,

$V_i - V_{gs} - I_d R_S = 0$

$V_{gs} = -I_dR_S + V_i$
For output impedance, $V_i = 0$.
Therefeore, $V_{gs} = -I_dR_S$----------(24)
Substituting Eq (24) in (23)
$V_0 = I_d(r_d+g_mR_Sr_d+R_S)$
Therefore, $Z_o' = V_o/I_d = r_d + g_mR_Sr_d + R_S$
But, $\mu = g_mr_d$
Therefore, $Z_o' = r_d+ R_S(\mu+1)$----------(25)
Thus, output impedance with unbypassed RS is increased.
Zo: Output impedance considering RD
$Zo = Z_0'||R_D$
Voltage Gain ,AV:
From Fig 42, $V_o = -I_dR_D$----------(26)
Apply KVL to the outer part of Fig 42,
$(I_d-g_mV_{gs})r_d + I_dR_D + I_dR_S = 0$;----------(27)
Also $V_{gs} = V_i - I_dR_S$----------(28)
Eq (27) in Eq (26)
$I_d = (g_mV_ir_d)/(r_d + g_mR_Sr_d + R_s + R_D)$----------(29)
Eq (22) in Eq (19)
$V_o= (-g_mV_ir_dR_D)/(r_d + g_mR_Sr_d + R_S + R_D)$
$A_V = V_o/V_i = -g_mr_dR_D/r_d + g_mR_Sr_d + R_S + R_D$
If $r_d >> R_S+R_D$,
$A_V = -g_mR_D/(1+g_mR_S)$

Common Drain (CD)/ Source Follower Configuration:

Fig. (43) shows Common Drain configuration. The input is applied between Gate and Source and output between Source and Ground (i.e. Drain is grounded during AC analysis)

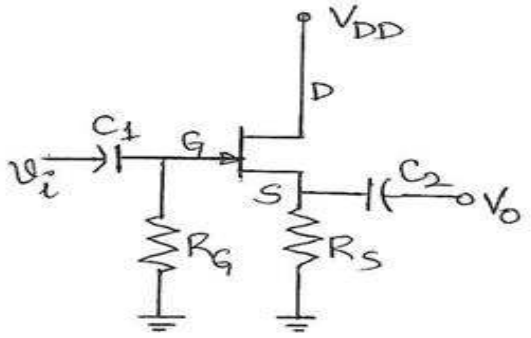


Fig 43: Source Follower Circuit

From the circuit in Fig 43,
$V_G + V_{GS} - V_S = 0$
Therefore $V_G + V_{GS} = V_S$
When a signal is applied to JFET gate via C_1, V_G varies with the signal. As V_{GS} is constant and $V_S = V_G + V_{GS}$ varies with V_i. As the output voltage at the Source (V_S)

follows changes in the signal voltage applied to the gate, this circuit is also called Source follower.

The AC equivalent circuit and low frequency equivalent model for Source follower is as shown in Fig. (44) and Fig. (45) respectively.

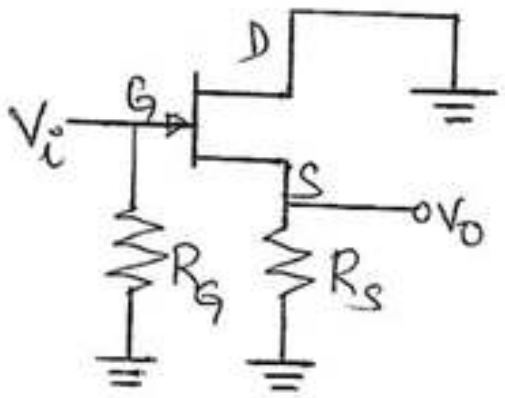


Fig. (44) AC Equivalent Circuit

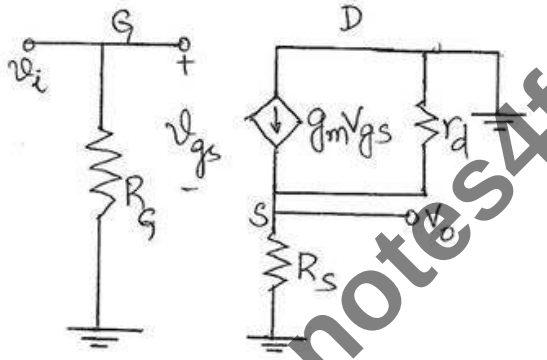


Fig. (45) AC Equivalent Model

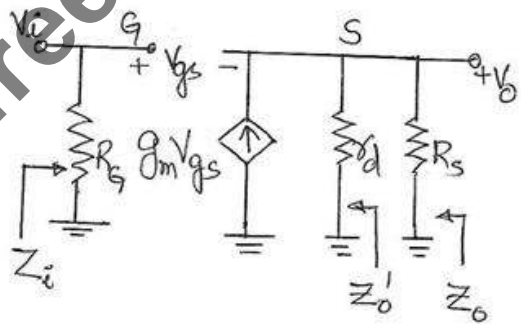


Fig (46) AC Equivalent Model

V_i-V_{gs}-V_o=0

V_o=V_i-V_{gs}

V_o + V_{gs}-V_i=0

V_{gs}=V_i-V_o

V_i=0, V_{gs}=-V_o

Z_i:

From the input circuit,

Z_i= R_G

Output Z:Z_o

Fig. (45) can also be written as Fig. (46)

$\acute{Z}_O = \frac{V_o}{I_d}$

Apply KVL to the output loop of Fig 46,

V_i-V_{gs}-V_o=0

For Z_o, V_i=0, V_o=V_{gs}

But from Fig. (46), I_d=$g_m V_{gs}$

Therefore $g_m V_o = I_d$

$\acute{Z}_O = \frac{V_o}{I_d} = \frac{1}{g_m}$

Therefore $Z_o = \acute{Z}_O \| R_S$

$Z_o = \frac{1}{g_m} \| R_S$

Voltage Gain, A_V

$A_V = \frac{V_o}{V_i}$

From Fig. (46),

$V_o = I_d (r_d \| R_S)$

And $I_d = g_m V_{gs}$

Therefore $V_o = g_m V_{gs} (r_d \| R_S)$

From input circuit

$V_i = -V_{gs} + V_o$

Therefore $V_i = - g_m V_{gs} (r_d \| R_S) - V_{gs}$

Therefore $A_V = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_S)}{-V_{gs}[g_m(r_d \| R_S)+1]}$

$A_V = \frac{g_m(r_d \| R_S)}{1+[g_m(r_d \| R_S)]}$

If $rd >> RS$; $r_d \| R_S \approx R_S$

$A_V = \frac{g_m R_S}{1+g_m R_S}$

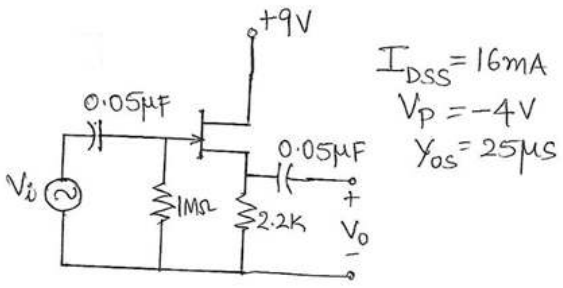
If $g_m R_S >> 1$, $A_V \approx 1$ but it is always less than one.

There is no phase shift between input and output voltages.

Source Follower exhibits following Characteristics;

- High input Impedance.
- Low Output Impedance
- Voltage gain is less than 1.
- No phase shift between input and output.

Example: A DC analysis of Source Follower network shown in Fig. below results in V_{GSQ}= -2.86V and I_{DQ}=4.56mA. Determine (i) g_m (ii) r_d (iii) Z_i (iv) Z_o with and without r_d (v) A_V with and without r_d. Take I_{DSS}=16mA, V_P=-4V, Y_{OS}=25µS.



(i) $g_{mo} = \frac{2I_{DSS}}{V_P} = \frac{2\times16\times10^{-3}}{4} = 8\text{mS}$

$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_P}\right) = 8 \times 10^{-3}\left(1 - \frac{(-2.86)}{(-4)}\right)$

$g_m = 2.28 \times 10^{-3}$ S.

(ii) $r_d = \frac{1}{Y_{OS}} = \frac{1}{25\times10^{-6}} = 40\text{K}\Omega$

(iii) $Z_i = R_G = 1\text{M}\Omega$

(iv) With r_d

$Z_o = r_d \| R_S \| \frac{1}{g_m} = 40\text{K} \| 2.2\text{K} \| \frac{1}{2.28\times10^{-3}}$

$= 362.52\Omega$

Without r_d

$Z_o = R_S \| \frac{1}{g_m} = 2.2 \times 10^3 \| \frac{1}{2.28\times10^{-3}}$

$= 365.69\Omega$

(v) A_V With r_d

$A_V = \frac{g_m(r_d \| R_S)}{1+[g_m(r_d \| R_S)]} = 0.826.$

A_V Without r_d

$A_V = \frac{g_m R_S}{1+g_m R_S} = \frac{2.28\times10^{-3}\times2.2\times10^3}{1+2.28\times10^{-3}\times2.2\times10^3} = 0.833$

Common Gate (CG) Configuration:

Fig. (47) shows CG configuration, the input is applied between Source and Gate and output is taken between Drain and Gate.

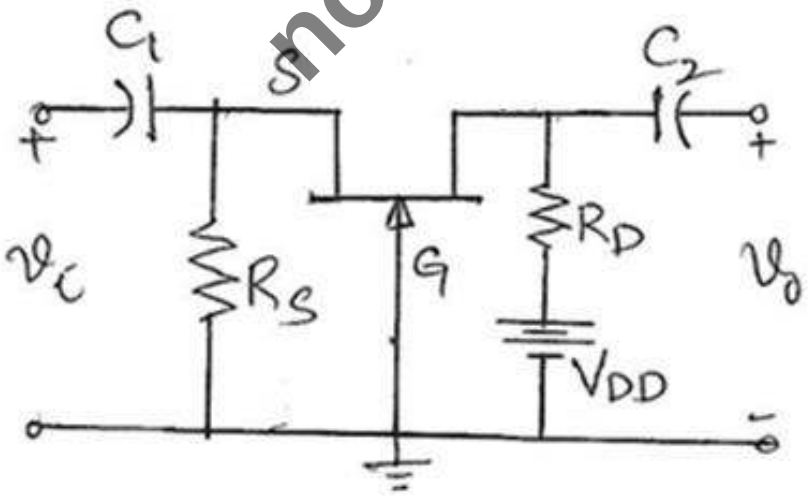


Fig. (47) Common Gate Configuration

In CG configuration, Gate voltage is constant. An increase in V_i in positive direction increases the –Ve Gate to Source bias voltages. Due to this Drain current reduces, reducing the drop I_DR_D. Since $V_D = V_{DD} - I_DR_D$, the reduction in I_D results in an

increase in output V_g V_D. Similarly when input V_g reduces, opposite action takes place which reduces the output voltage. Thus there is no phase shift between input and output in a Common Gate amplifier. AC equivalent model of CG amplifier is as shown in Fig. (48).

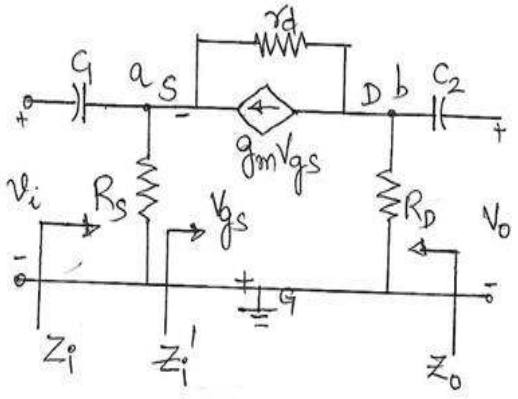


Fig. (48) AC Equivalent Model

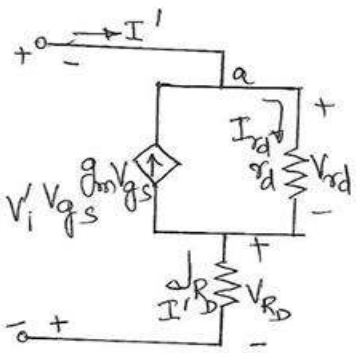


Fig (49) AC Equivalent Model Redrawn

$\acute{Z}_\iota = \frac{V_i}{I}$

Current through r_d (Fig 49)

$I_{rd} = I + g_m V_{gS}$

Therefore $I = I_{rd} - g_m V_{gS}$ ----- (30)

From the circuit,

$I_{rd} = \frac{V_i - IR_D}{r_d}$ ----- (31)

Substitute Eq. (31) in Eq. (30)

$I = \frac{V_i - IR_D}{r_d} - g_m V_{gS}$ ----- (32)

But $V_i = -V_{gS}$ (from Fig. (49))

Therefore $I = \frac{V_i - IR_D}{r_d} + g_m V_i$

$I = \frac{V_i}{r_d} - \frac{IR_D}{r_d} + g_m V_i$

$I\left[1 + \frac{R_D}{r_d}\right] = V_i\left[\frac{1}{r_d} + g_m\right]$

$\frac{V_i}{I} = \frac{1+\frac{R_D}{r_d}}{\frac{1}{r_d}+g_m} = \frac{r_d+R_D}{g_m r_d+1} = \acute{Z}_\iota$

$Z_i = \acute{Z}_\iota \| R_S = R_S \| \frac{r_d+R_D}{1+g_m r_d}$

If $r_d >> R_D$ and $g_m r_d >> 1$,

$Z_i = R_S \| \frac{r_d}{g_m r_d} = R_S \| \frac{1}{g_m}$

Input impedance of CG amplifier is less than CS and CD amplifier.

Z_o : when V_i=0 i.e. when input is short circuited, the equivalent circuit is

$Z_o = r_d \| R_D$

If $r_d >> R_D$, $Z_O \approx R_D$

$A_V = \frac{V_o}{V_i}$

V_O=-$I_D R_D$ and V_i=-V_{gs}
Apply KVL to Fig. (b) outer loop
V_i+ (I_d-$g_m V_{gs}$)r_d+ $I_D R_D$=0
But V_{gs} =- V_i
Therefore Vi + $I_d R_d$ +$g_m V_i r_d$ + $I_D R_D$=0
Vi [1+$g_m r_d$] + I_d [r_d+R_D] =0
-I_d [r_d+R_D] = Vi [1+$g_m r_d$]

$V_i = \frac{-I_d(r_d+R_D)}{1+g_m r_d}$

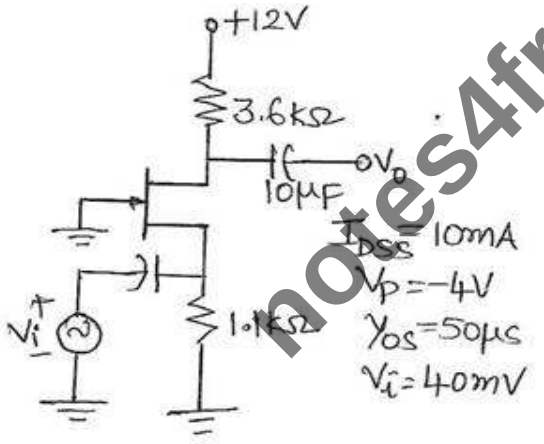
$A_V = \frac{V_o}{V_i} = \frac{R_D(1+g_m r_d)}{r_d+R_D}$

If $r_d >> R_D$, $g_m r_d >> 1$

$A_V = \frac{R_D(g_m r_d)}{r_d} = R_D\, g_m$

Thus there is no phase shift between input and output in CG amplifier.

Example: For the network shown ,if V_{GSQ} = -2.2V and I_{DQ} = 2.03mA. Determine g_m,r_d. Calculate Z_i with and without r_d, Z_o with and without r_d. Determine v_o with and without r_d.



(i) $g_{mo} = \frac{2I_{DSS}}{V_P} = \frac{2\times10\times10^{-3}}{4} = 5\text{mS}$

$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_P}\right) = 5\times10^{-3}\left(1 - \frac{(-2.2)}{(-4)}\right)$

$g_m = 2.25\times10^{-3}$ S.

(ii) $r_d = \frac{1}{Y_{OS}} = \frac{1}{50\times10^{-6}} = 20\text{K}\Omega$

(iii) $\frac{r_d+R_D}{g_m r_d+1} = \acute{Z}_l = 0.31\text{K}\Omega$

(iv) $Z_i = \acute{Z}_l \| R_S = R_S \| \frac{r_d+R_D}{1+g_m r_d} = 0.35\text{K}\Omega$

(v) $Z_O \approx R_D = 3.6\text{K}\Omega$

(vi) $Z_o = r_d \| R_D = 3.05\text{K}\Omega$

(vii) $A_V = R_D\, g_m = 8.1$

(viii) $A_V = \frac{V_o}{V_i} = \frac{R_D(1+ g_m r_d)}{r_d + R_D} = 7.02$

(ix) $vo\ without\ rd = 324mV$

$$vo = 280.8mV$$

Module 3: TRANSISTOR and FET FREQUENCY RESPONSE

The frequency response of an amplifier is the plot of the magnitude of voltage gain as a function of frequency. In transistor amplifier the low frequency response is governed by coupling and bypass capacitors. The high frequency response is affected by the transistor parasitic capacitances and stray wiring capacitances. The mid frequency response is unaffected by these capacitances.

General frequency considerations:

The response of a single stage or multistage amplifier depends on the frequency of the applied signal. The coupling and bypass capacitors affect the low frequency response since the reactance of these capacitors decreases with increase in frequency. The internal capacitances of the active devices and the stray wiring capacitances will limit the high frequency response of the system. An increase in the number of stages of a cascaded system will also limit the low and high frequency responses.

Frequency response of RC Coupled amplifier:

Fig. (1) shows the frequency response of RC coupled amplifier. The horizontal scale is a logarithmic scale to permit a plot extending from low to high frequency regions. The frequency range is divided into 3 regions.

(i) Low frequency region.
(ii) Mid frequency region.
(iii) High frequency region.

The drop in the gain at low frequencies is due to the coupling capacitors (C_C,C_S) and bypass capacitors (C_E). At high frequencies the drop in gain is due to the internal device capacitances and the stray wiring capacitances. In the mid frequency range the gain is almost independent of the frequency. This is due to the fact that at mid frequencies the coupling and bypass capacitors act as short circuits and the device and stray wiring capacitances act as open circuits due to their low capacitance. The mid band gain is denoted as Av_{mid}.

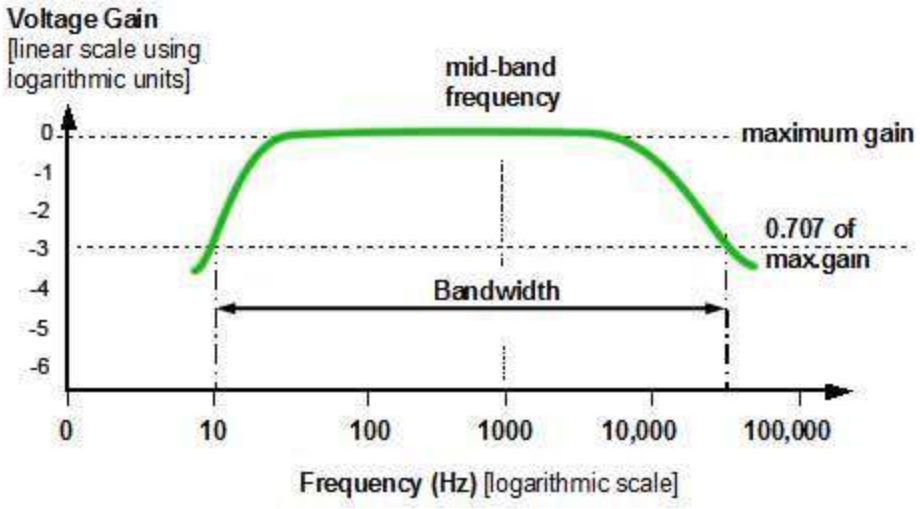


Fig. (1) Frequency response of RC coupled amplifier.

Frequency response of transformer coupled amplifier:

Fig.(2) shows frequency response of transformer coupled amplifier. The magnetizing inductive reactance of the transformer winding is $X_L=2\pi fl$. At low frequencies the gain drops due to small value of X_L. At f=0 (DC) there is no change in flux in the core. As a result the secondary induced voltage or output voltage is zero and hence the gain. At high frequencies the gain drops due to stray capacitance between the turns of primary and secondary windings.

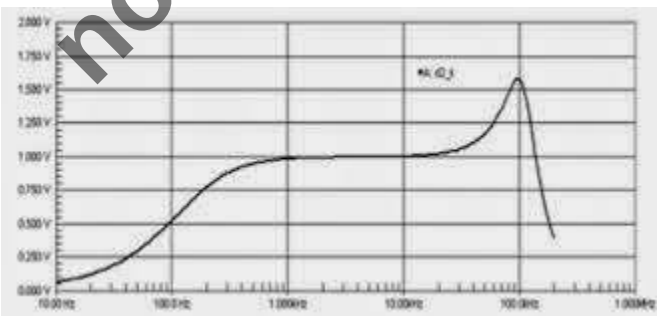


Fig. (2) Frequency response of transformer coupled amplifier.

Frequency response of direct coupled amplifier:

Fig. (3) shows frequency response of direct coupled amplifier. Since there are no coupling or bypass capacitors, there is no drop in gain at low frequencies. It has a flat response to the upper cut-off frequency. Gain drops at high frequencies due to device internal capacitances and the stray wiring capacitances.

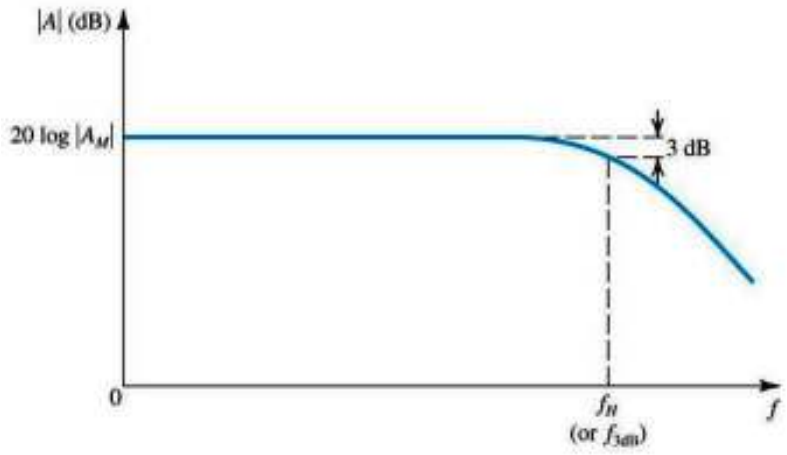


Fig. (3) Frequency response of direct coupled amplifier.

Half power frequencies and bandwidth:

The frequencies f_1 and f_2 at which the gain is 0.707 Av_{mid} are called cut-off frequencies or corner frequencies or break frequencies. f_1 is called the lower cut-off frequency and f_2 is called the upper cut-off frequency.

Bandwidth or pass band of the amplifier is

$BW = f_2 - f_1$ ----- (1)

The output voltage in the mid band is $|V_O| = |Av_{mid}|\,|V_i|$

Output power in the mid band is

$$P_{O(mid)} = \frac{|V_O|^2}{R_O}$$

$$= \frac{|Av_{mid}|^2 |V_i|^2}{R_O} \text{ ----- (2)}$$

The output voltage at cut-off frequencies is

$$|V_O| = |0.707 Av_{mid}|\,|V_i|$$

The output power at cut-off frequencies is

$$P_{O\,(cut\text{-}off)} = \frac{|0.707 Av_{mid}|^2 |V_i|^2}{R_O}$$

$= \frac{0.5\ |\mathrm{Av}_{mid}|^2 |V_i|^2}{R_O}$

$= 0.5\ P_{O\ (mid)}$ ----- (3)

Thus, the output power at cut-off frequencies is half the mid band power output. f_1 is called the lower half power frequency and f_2 is called the upper half power frequency.

Normalized gain V/s Frequency plot:

The normalized gain is obtained by dividing the gain Av at each frequency by the mid band gain Av_{mid}.

Therefore normalized gain = $\frac{A_V}{Av_{mid}}$ ----- (4)

Fig. (4) shows the normalized gain V/s frequency plot for an RC coupled amplifier.

The normalized mid band gain is $\frac{Av_{mid}}{Av_{mid}}$ =1

The normalized gain at cut-off frequencies is $\frac{0.707 Av_{mid}}{Av_{mid}}$ =0.707

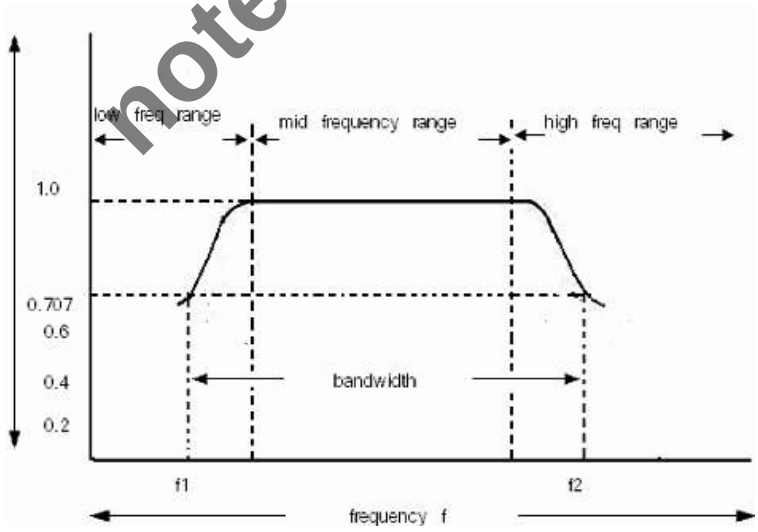


Fig. (4) Normalized gain V/s frequency plot

Normalized decibel gain is $\left.\frac{A_V}{Av_{mid}}\right|_{\mathrm{dB}} = 20 \log_{10}\left[\frac{A_V}{Av_{mid}}\right]$ -----(5)

Normalized decibel voltage gain in mid band is

$20 \log_{10}\left[\frac{A_V}{Av_{mid}}\right]$ =0

Normalized decibel voltage gain at cut-off frequencies is

$20 \log_{10}\left[\frac{0.707A_V}{Av_{mid}}\right]$ =-3dB

Since normalized decibel voltage gain at cut-off frequencies is 3dB less than the normalized decibel mid band voltage gain. f_1 and f_2 are also called 3dB frequencies.

f_1 →lower 3dB frequency

f_2→upper 3dB frequency

Fig. (5) shows the plot of normalized dB voltage gain V/s frequency for an RC coupled amplifier.

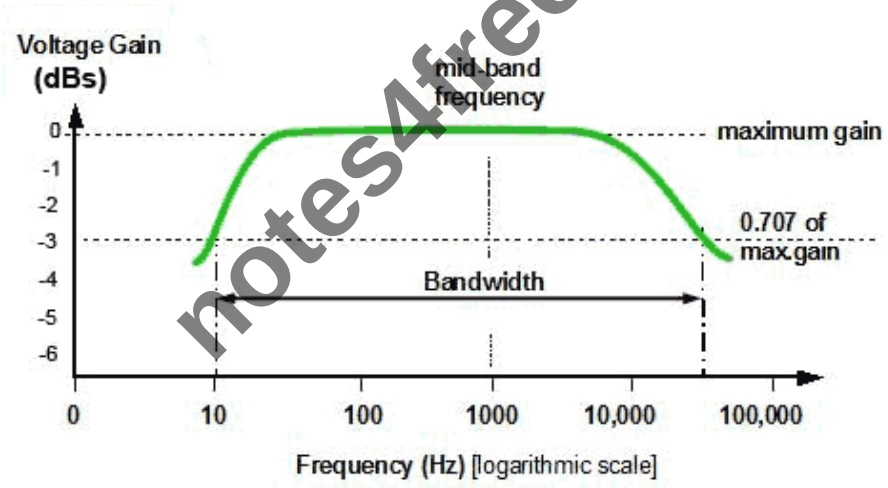


Fig. (5) Plot of normalized decibel voltage gain V/s frequency.

Phase angle plot:

A single stage RC coupled amplifier introduces a 180^0 phase shift between input and output signals in the mid band region. At low frequencies the output voltage V_O lags V_i by an additional angle θ_1. Therefore, the total phase phase shift between V_O and V_i is more than 180^0. At high frequencies, V_O leads V_i by an additional angle θ_2. As a result, the total phase shift drops below 180^0. Fig. (6) shows the phase plot for a single stage RC coupled amplifier.

Fig. (6) Phase plot of single stage RC coupled amplifier.

Low frequency analysis:

In the low frequency region of a single stage BJT amplifier, the amplifier gain increases with frequency. Hence it can be modelled as a high pass RC circuit as shown in Fig. (7).

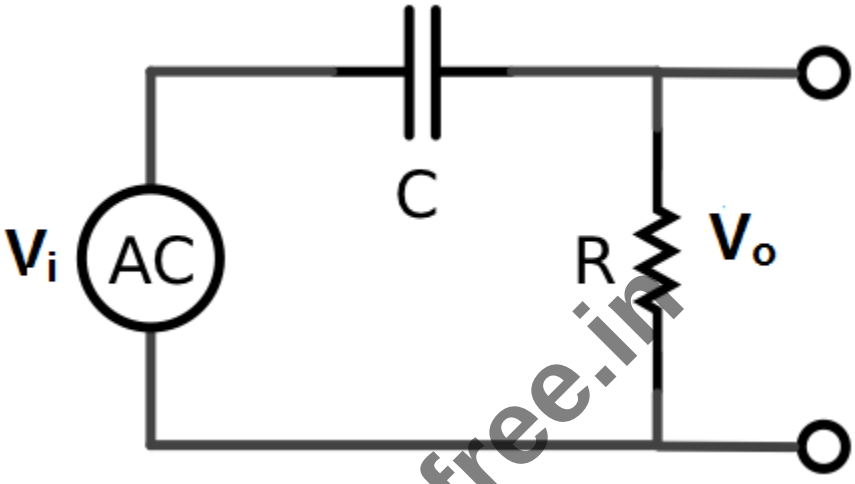


Fig. (7) Amplifier modelled as high pass RC circuit.

The capacitor C represents the combined effect of coupling and bypass capacitors and the resistance R represents the combined effect of resistive elements of the amplifier network.

The capacitive reactance is

$X_C = \frac{1}{2\pi fc}$ ----- (6)

At f=0, $X_C = \infty\Omega$. i.e. at low frequencies, the capacitor acts as a open circuit as shown in Fig. (8)

From Fig. (8), V_O=0.

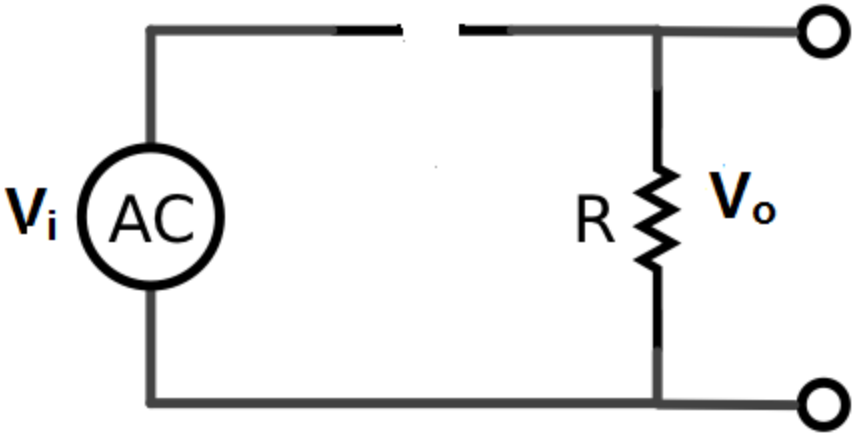


Fig. (8) at f=0

At high frequencies, $X_C \approx 0\Omega$ i.e. at high frequencies, capacitor acts as a short circuit as shown in Fig. (9).

From Fig. (9), $V_O \approx V_L$

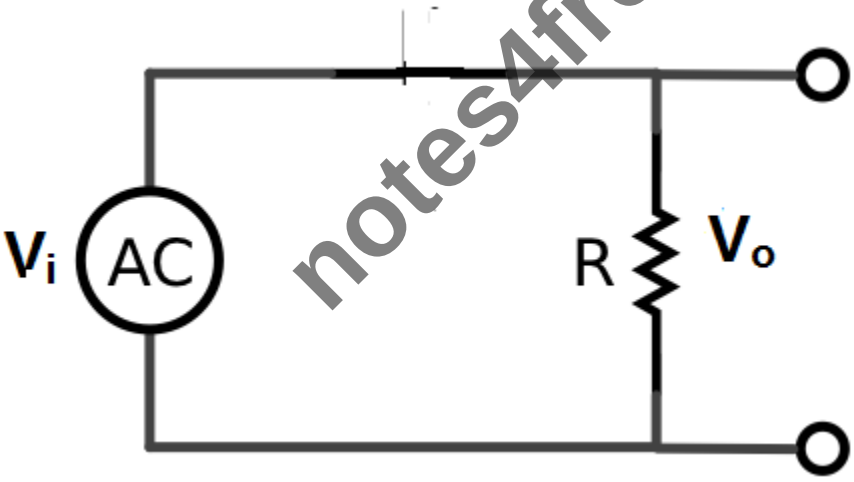


Fig. (9) at high frequencies

Hence as the input signal frequency increases from zero to mid band value, the output voltage rises from zero to V_i and hence the gain from zero to 1.

Mathematical analysis:

Apply Voltage division rule to circuit in Fig. (7),

$V_O = \frac{V_i R}{R - jX_C}$

Voltage gain is given by

$A_V = \frac{V_o}{V_i} = \frac{R}{R - jX_C} = \frac{R}{R[1 - j\frac{X_C}{R}]}$

$A_V = \frac{1}{1 - j[\frac{X_C}{R}]}$ ------ (7)

The magnitude of voltage gain is

$|A_V| = \frac{1}{\sqrt{1 + [\frac{X_C}{R}]^2}}$ ----- (8)

(i) At f=0, $X_C = \frac{1}{2\pi fc} = \infty\Omega$ therefore $|A_V| = 0$

(ii) At high frequencies, $f \rightarrow \infty$, therefore $X_C \rightarrow 0$. Hence $|A_V| \rightarrow 1 = |A_V|_{mid}$

$|A_V|_{mid\ (dB)} = 20 \log_{10}(1) = 0dB$

(iii) When $X_C = R$ ----- (9)

$|A_V| = \frac{1}{\sqrt{2}} \rightarrow \frac{V_o}{V_i} = \frac{1}{\sqrt{2}}$ or $V_O = 0.707V_i$

The corresponding decibel gain is

$20 \log_{10} \frac{1}{\sqrt{2}} = -3dB$

From Eq. (9), $\frac{1}{2\pi fc} = R$

$f = \frac{1}{2\pi Rc}$

The frequency given by the above Eq. is the lower cut-off frequency or lower 3dB cut-off frequency denoted by f_1.

Therefore $f_1 = \frac{1}{2\pi Rc}$ ----- (10)

$\frac{X_C}{R} = \frac{1}{2\pi fcR} = [\frac{1}{2\pi Rc}] \times \frac{1}{f} = \frac{f_1}{f}$

Using in Eq. (7) and (8)

$A_V = \frac{1}{1-j[\frac{f_1}{f}]}$ ------ (11)

$|A_V| = \frac{1}{\sqrt{1+[\frac{f_1}{f}]^2}}$ ----- (12)

From Eq. (11), phase angle of A_V is

$\theta_1 = \tan^{-1}\left[\frac{f_1}{f}\right]$ ----- (13)

Since θ_1 is +Ve, V_O leads V_i by an angle θ_1

In magnitude and phase form, Eq. (11) can be written as

$A_V = |A_V| \Delta \theta_1$

$= \frac{1}{\sqrt{1+[\frac{f_1}{f}]^2}} \Delta \tan^{-1}\left[\frac{f_1}{f}\right]$ ----- (14)

Fig. (10) shows the plot of $|A_V|$ V/s frequency.

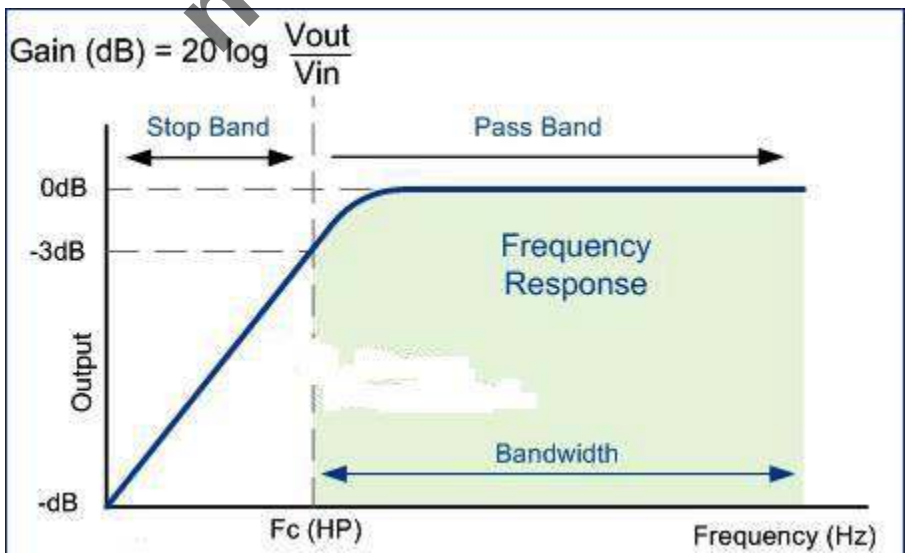


Fig. (10) Low frequency response of high pass RC circuit.

Bode plot of low frequency response:

From Eq. (12), we have

$$|A_V| = \frac{1}{\sqrt{1+[\frac{f_1}{f}]^2}}$$

Voltage gain in dB is

$$|A_V|_{dB} = 20 \log_{10} \left[\frac{1}{\sqrt{1+[\frac{f_1}{f}]^2}}\right]$$

$$|A_V|_{dB} = -20 \log_{10} \sqrt{1 + [\frac{f_1}{f}]^2} \text{ ----- (15)}$$

To construct the plot of $|A_V|_{dB}$ V/s frequency using straight line segments, we consider the following frequency ranges.

(a) For frequencies f << f_1 or $\frac{f_1}{f}$ >> 1

Eq. (15) can be approximated as

$$|A_V|_{dB} = -20 \log_{10} \sqrt{[\frac{f_1}{f}]^2}$$

$$|A_V|_{dB} = -20 \log_{10} [\frac{f_1}{f}] \text{ ----- (16)}$$

$|A_V|_{dB}$ is calculated at different values of $\frac{f_1}{f}$ and tabulated in table (1).

f	$\frac{f_1}{f}$	$\|A_V\|_{dB} = -20 \log_{10} [\frac{f_1}{f}]$
$\frac{f_1}{10}$	10	-20dB
$\frac{f_1}{4}$	4	-12dB

$\frac{f_1}{2}$	2	-6dB
f_1	1	0dB

Table (1): $|A_V|_{dB}$ at different frequencies.

Following conclusions can be drawn from table (1).

(i) A change in frequency by a factor of 2 is equal to one octave. When the frequency changes from $\frac{f_1}{4}$ to $\frac{f_1}{2}$ or $\frac{f_1}{2}$ to f_1(one octave), the gain increases by 6dB.

(ii) A change in frequency by a factor of ten is equal to one decade. When the frequency changes from $\frac{f_1}{10}$ to f_1(one decade), the gain increases by 20dB.

(iii) If a plot of $|A_V|_{dB}$ against log scale in the frequency range $\frac{f_1}{10} < f < f_1$ is plotted, a straight line with slope 6dB/octave or 20dB/decade is obtained as shown in Fig. (11).

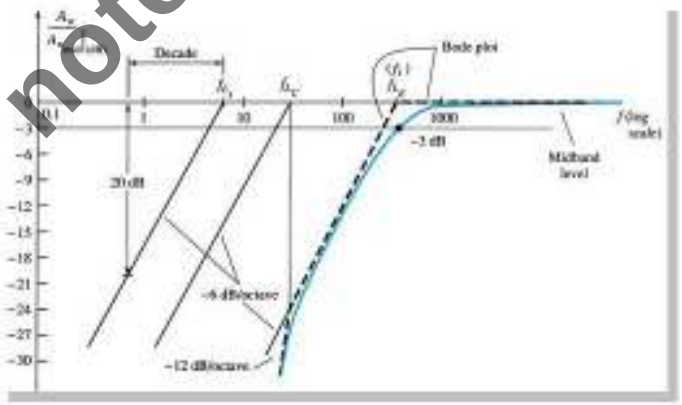


Fig. 11: Bode plot for low frequency region.

(b) For frequencies, f >> f_1 or $\frac{f_1}{f}$ <<1

Eq. (15) can be approximated by

$|A_V|_{dB} \approx$ - 20 $\log_{10}$ 1=0dB.

The plot of $|A_V|_{dB}$ against log scale for the frequency range f >>f_1, is a straight line on the frequency axis as shown in Fig. (11). The slope of this line is zero, since the gain is constant at 0dB. The plot in Fig. (11) is made of 2 straight line segments called asymptotes with a break point at f_1. Hence f_1 is called break frequency or corner frequency. This peicewise linear plot is also called bode magnitude plot or simply bode plot.

From bode plot, at f= f_1 , $|A_V|_{dB}$ =0.

From bode plot, at f= f_1 , $|A_V|_{dB}$ =-3.

Thus, at f= f_1 , the gain read from bode plot differs from the actual gain by 3dB.

Phase Plot:

At low frequencies, V_O leads V_i by an angle θ_1 given by

$$\theta_1 = \tan^{-1}\left[\frac{f_1}{f}\right] \text{ ----- (17)}$$

The value of θ_1 is calculated at different values of $\frac{f_1}{f}$ as shown in table (2).

Table (2): Phase angle between V_O and V_i

f	$\frac{f_1}{f}$	$\theta_1 = \tan^{-1}\left[\frac{f_1}{f}\right]$	Total phase shift θ=180 + θ_1
0	∞	90^0	270^0
$\frac{f_1}{100}$	100	89.4^0	269.4^0
f_1	1	45^0	225^0
$100f_1$	0.01	0.572^0	180.572^0
∞	0	0^0	180^0

The total phase shift θ_1 between V_O and V_i is the sum of the phase shift of RC network and inherent phase shift (180^0) introduced by the amplifier.

From table (2),

(i) The phase shift θ_1 due to RC network decreases from 90^0 to 0^0. The plot of θ_1 V/s frequency is shown in Fig. (12).

(ii) The total phase θ, decreases from 270^0 to 180^0.

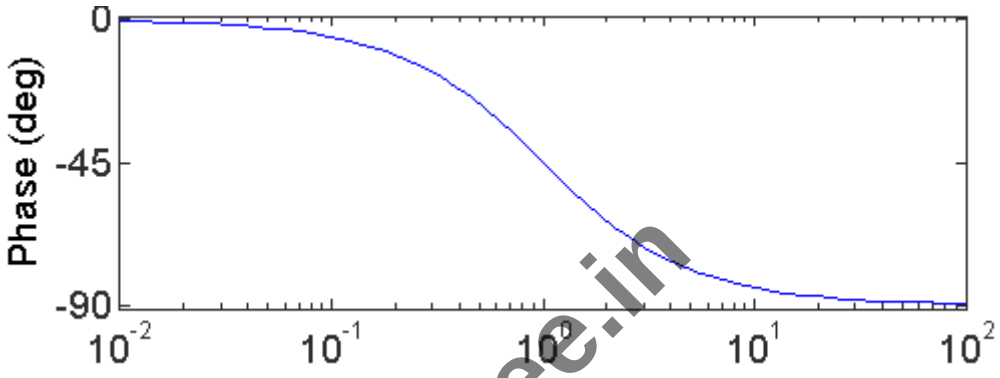


Fig. (12) Phase response of RC network.

Low frequency Response of BJT amplifier:

Fig. (13) shows the circuit of single stage BJT amplifier. The coupling capacitors C_S and C_C and bypass capacitor C_E determines the low frequency response.

Effect of C_S on low frequency response:

The input coupling capacitor C_S couples the source signal to BJT. First, we will neglect the effects of C_C and C_E i.e. they are treated as short circuits.

The AC equivalent circuit is obtained by reducing VCC to zero and C_C and C_E by their short circuit equivalent as shown in Fig. (14).

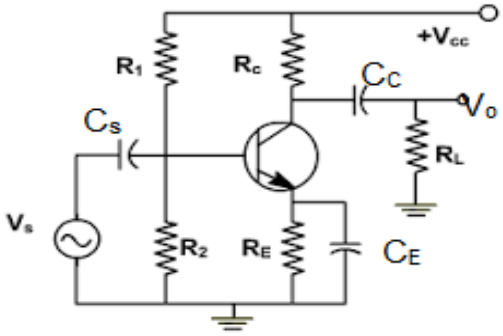


Fig. (13) Single stage BJT amplifier

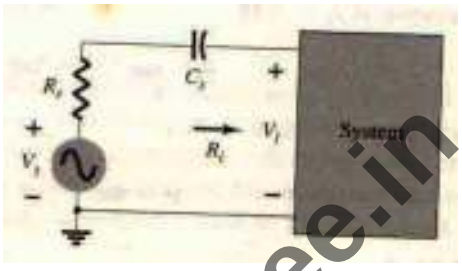


Fig. (14) AC equivalent circuit

The resistance of the transistor between base-emitter is h_{ie}. The input AC equivalent circuit is shown in Fig. (15).

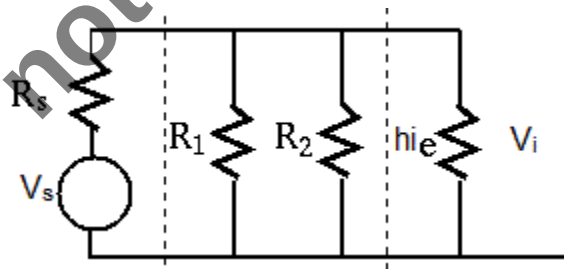


Fig. (15) Input AC equivalent

Let $R_i = R_1 \parallel R_2 \parallel h_{ie}$ ----- (18)

Where $h_{ie} = \beta r_e$ ----- (19)

Using voltage division rule in the circuit of Fig. (15) the voltage applied to the amplifier is

$$V_i = \frac{V_S R_i}{(R_{S+} R_i) - f X c_S} \text{ ----- (20)}$$

Where $Xc_S = \frac{1}{2\pi f C_S}$ ----- (21)

$$V_i = \frac{V_S\left[\frac{R_i}{R_S+R_i}\right]}{1-j\left[\frac{Xc_S}{R_i+R_S}\right]}$$

$$V_i = \frac{|V_S|\left[\frac{R_i}{R_S+R_i}\right]}{\sqrt{1+j\left[\frac{Xc_S}{R_i+R_S}\right]^2}} \text{-----(22)}$$

In the mid frequency band, f is large. As a result, $Xc_S \rightarrow 0$.

Therefore from Eq. (22),

$|V_i|_{mid} = \frac{|V_S|R_i}{(R_{S+}R_i)}$ ----- (23)

Therefore Eq. (22) becomes,

$$|V_i| = \frac{|Vi|mid}{\sqrt{1+\left[\frac{Xc_S}{R_i+R_S}\right]^2}} \text{ ----- (24)}$$

The lower 3dB cut-off occurs when $|V_i| = \frac{|Vi|mid}{\sqrt{2}} = 0.707\ |V_i|_{mid}$

Therefore Eq. (24) becomes,

$$0.707\ |V_i|_{mid} = \frac{|Vi|mid}{\sqrt{1+\left[\frac{Xc_S}{R_i+R_S}\right]^2}}$$

This condition is satisfie, if $\frac{Xc_S}{R_i+R_S} = 1$ or $Xc_S = R_i + R_S$

$\frac{1}{2\pi f C_S} = R_i + R_S$

Therefore f= $\frac{1}{2\pi(R_S+R_i)C_S}$ ----- (25)

Eq. (25) gives the lower 3dB cut-off frequency due to C_S.

Therefore $f_{Ls}= \frac{1}{2\pi(R_S+R_i)C_S}$ ----- (26)

Effect of output coupling capacitor C_C on low frequency response :

The output coupling capacitor C_C couples the output of the BJT to the load. The equivalent circuit on the output side by neglecting the effect of C_S and C_E by treating them as short circuits is as shown in Fig. (16).

Fig. (16) (a) AC equivalent circuit of output side (b) Simplified AC equivalent circuit

Let $R_O=r_O \| R_C$ ----- (27)

V_C= output voltage of BJT

V_O=load voltage

Using voltage division rule in circuit of Fig. (16) (a), the load voltage is,

$V_O= \frac{V_C R_L}{(R_{O+}R_L)-jXc_C}$ -----(28)

Where $Xc_C = \frac{1}{2\pi f C_C}$ ----- (29)

$$V_O = \frac{V_C\left[\frac{R_L}{R_O+R_L}\right]}{1-j\left[\frac{Xc_C}{R_O+R_L}\right]}$$

$$|V_O| = \frac{|V_C|\left[\frac{R_L}{R_O+R_L}\right]}{\sqrt{1+j\left[\frac{Xc_C}{R_O+R_L}\right]^2}}$$ ----- (30)

In the mid frequency band, Xc_C ➔ 0

Therefore $|V_O|_{mid} = \frac{|V_C|R_L}{(R_O+R_L)}$ ----- (31)

Substitute Eq. (31) in (30)

$$|V_O| = \frac{|Vo|mid}{\sqrt{1+\left[\frac{Xc_C}{R_O+R_L}\right]^2}} \text{ ----- (32)}$$

The lower 3dB cut-off occurs when $|V_O| = \frac{|Vo|mid}{\sqrt{2}} = 0.707\ |V_O|_{mid}$

This is possible iff,

$\frac{Xc_C}{R_O+R_L} = 1$ or $Xc_C = R_O + R_L$

Therefore $f = \frac{1}{2\pi(R_O+R_L)C_C}$ ----- (33)

Eq. (33) gives the lower 3dB cut-off frequency due to C_C.

Therefore $f_{Lc} = \frac{1}{2\pi(R_O+R_L)C_C}$ ----- (34)

Effect of Emitter bypass capacitor C_E on low frequency response :

The equivalent circuit (13) considering the effect of C_E is as shown in Fig. (17). Hence the effect of C_S and C_C are neglected.

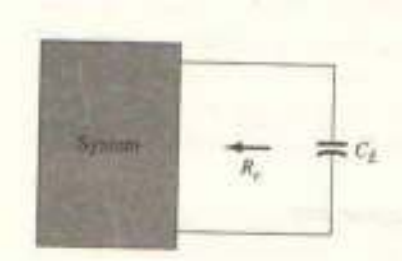


Fig. (17) AC equivalent circuit

Replacing the transistor by its low frequency small signal hybrid model the AC equivalent circuit is as shown in Fig. (18).

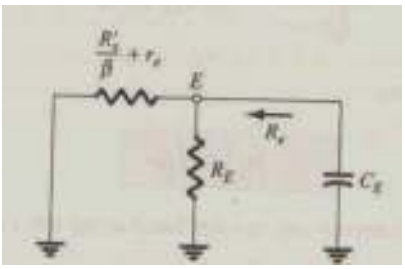


Fig. (18) AC equivalent circuit using hybrid model

R_e is the AC equivalent resistance seen by C_e. To find Re, V_S is reduced to 0 as shown in Fig. (18).

Let $\acute{Z}_\iota = R_S \| R_1 \| R_2$ ----- (35)

The AC equivalent circuit is redrawn as shown in Fig. (20)

Fig. (18) AC equivalent circuit to find R_e

$\acute{R}_S = \beta r_e$ is in base circuit. When it is transformed to emitter circuit, it is divided by β. Therefore $I_E \approx I_C = \beta I_B$.

The resulting circuit is shown in Fig. (21).

$R_e = R_E \| \frac{\acute{R}_S}{\beta} + r_e$ ----- (36)

From Fig. (18), the lower cut-off frequency due to C_E is

$f_{L_E} = \frac{1}{2\pi R_e C_E}$ ----- (37)

Effect of C_E on voltage gain:

The mid band voltage gain of amplifier of Fig. (13) without C_E is given by,

$A_{V_{mid}} = -\frac{R_O || R_L}{r_e + R_E}$ ----- (38)

Where $R_O = R_C || r_O$

If C_E is connected in parallel with R_E, then voltage gain becomes a function of frequency. The voltage gain at any frequency is

$$A_V = -\frac{R_O||R_L}{r_e+R_E||X_{C_E}} \text{ ----- (39)}$$

Where $X_{C_E} = \frac{1}{2\pi f C_E}$ ----- (40)

As the frequency increases:

(i) X_{C_E} decreases.
(ii) $R_E || X_{C_E}$ decreases.
(iii) A_V increases in magnitude.

As the frequency approaches the mid band value

(i) X_{C_E} approaches zero.
(ii) $R_E || X_{C_E}$ approaches zero. (i.e. R_E is shorted out)
(iii) A_V approaches maximum value or mid band value.

$$A_{V_{mid}} = -\frac{R_O||R_L}{r_e} \text{ ----- (41)}$$

Overall lower cutoff frequency:

The low frequency response of the amplifier is influenced by the capacitors C_S, C_C and C_E. The lower cut-off frequencies due to C_S, C_C and C_E are f_{L_S}, f_{L_C} and f_{L_E} respectively. If these cut-off frequencies are relatively apart (i.e. one is greater than the other by 4 times or more) the higher of the 3 is approximately the lower cut-off frequency for the amplifier stage.

Ex: $f_{L_S} = 6Hz$, $f_{L_C} = 25Hz$ and $f_{L_E} = 320Hz$

Then the lower cut-off frequency of amplifier is $f_{L_E} = 320Hz$ Because, $f_{L_E} > 4f_{L_S}$

$f_{L_E} > 4f_{L_C}$.

Miller Effect Capacitance:

Fig. (19) shows an inverting amplifier with a capacitance C_f between the input and output nodes. WKT, A_V is –Ve for inverting amplifier since V_O and V_i are

180^0 out of phase. Using Millers theorem we can find the loading effect of C_f on the input and output circuits of the amplifier.

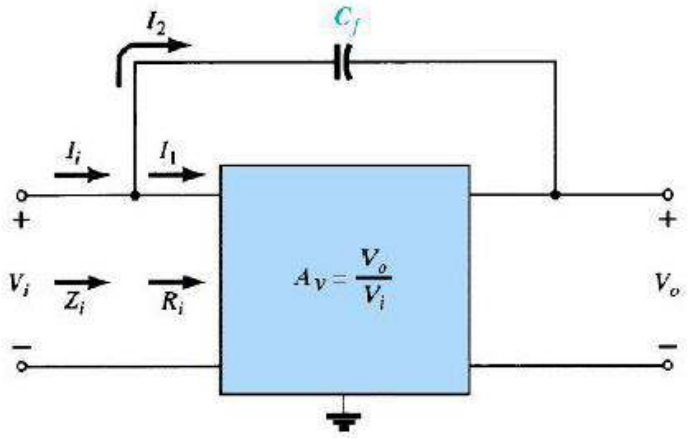


Fig. (19) Inverting amplifier with capacitance between input and output nodes.

To find Miller-Input Capacitance (C_{mi}) :

From Fig. (19),

$R_i = \frac{V_i}{I_1}$ ➔ $I_1 = \frac{V_i}{R_i}$

$Z_i = \frac{V_i}{I_i}$ ➔ $I_i = \frac{V_i}{Z_i}$

Apply KCL at input node A,

$I_i = I_1 + I_2$ ----- (42)

From Fig. (23),

$I_2 = \frac{V_i - V_o}{X_{C_f}}$

But $V_0 = A_V V_i$

Therefore $I_2 = \frac{V_i - A_V V_i}{X_{C_f}} = \frac{V_i[1 - A_V]}{X_{C_f}}$

Substitute for I_i , I_1 and I_2 in Eq. (42), we get

$$\frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{V_i[1-A_V]}{X_{C_f}}$$

Eliminating V_i throught,

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{[1-A_V]}{X_{C_f}} = \frac{1}{R_i} + \frac{1}{\frac{X_{C_f}}{1-A_V}}$$

Let $X_{C_{mi}} = \frac{X_{C_f}}{1-A_V}$ ----- (43)

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_{mi}}} \text{ ----- (44)}$$

But $X_{C_f} = \frac{1}{2\pi f C_f}$

$$X_{C_{mi}} = \frac{1}{[1-A_V]2\pi f C_f} \text{ ----- (45)}$$

Where $C_{mi} = [1 - A_V]C_f$ = miller input capacitance ----- (46)

From Eq. (44), Z_f can be interpreted as the impedance resulting from the parallel combination of R_i and C_{mi} as shown in Fig. (24).

To find Miller output capacitance (C_{mo}) :

From Fig. (19),

$R_O = \frac{V_o}{V_i}$ ➔ $I_1 = \frac{V_o}{R_O}$

$Z_O = \frac{V_o}{I_O}$ ➔ $I_O = \frac{V_o}{Z_O}$

Apply KCL at node B,

$I_0 = I_1 + I_2$ ----- (47)

From Fig. (19)

$I_2 = \frac{V_O - V_i}{X_{C_f}}$

But $V_0 = A_V + V_i$ or $V_i = \frac{V_o}{A_V}$

Therefore $I_2 = \frac{V_O - \frac{V_o}{A_V}}{X_{C_f}} = \frac{V_O\left[1 - \frac{1}{A_V}\right]}{X_{C_f}}$

Usually, R_O is large therefore $\frac{V_o}{R_0}$ can be neglected

Eq. (47), $\frac{V_o}{Z_0} = \frac{V_o}{R_0} + \frac{V_O\left[1 - \frac{1}{A_V}\right]}{X_{C_f}}$

$I_0 \approx \frac{V_O\left[1 - \frac{1}{A_V}\right]}{X_{C_f}}$

$Z_0 = \frac{V_0}{I_0} = \frac{X_{C_f}}{1 - \frac{1}{A_V}} = \frac{1}{\left[1 - \frac{1}{A_V}\right] 2\pi f C_f}$

$Z_0 = \frac{1}{2\pi f C_{m_o}}$ ----- (48)

Where, $C_{m_o} = \left[1 - \frac{1}{A_V}\right] C_f$ ----- (49)

C_{m_o} is called Miller output Capacitance.

Statement of Millar's theorem:

A capacitance C_f connected between the input and output nodes of an inverting amplifier can be replaced by

(i) Miller input capacitance, $C_{m_i} = = [1 - A_V]C_f$ connected between input node and ground.

(ii) Miller output capacitance, $C_{m_o} = \left[1 - \frac{1}{A_V}\right] C_f$ connected between output node and ground.

For an non-inverting amplifier A_V is positive. In order to obtain positive values for C_{m_i} and C_{m_o}. Eq. (46) and Eq. (49) should be modified as follows

$C_{m_i} = = [1 - A_V] C_f$ ----- (50)

$C_{m_o} = \left[1 + \frac{1}{A_V}\right] C_f$ ----- (51)

Applications of Miller's theorem to the amplifier of Fig. (19) results in network shown in Fig. (20).

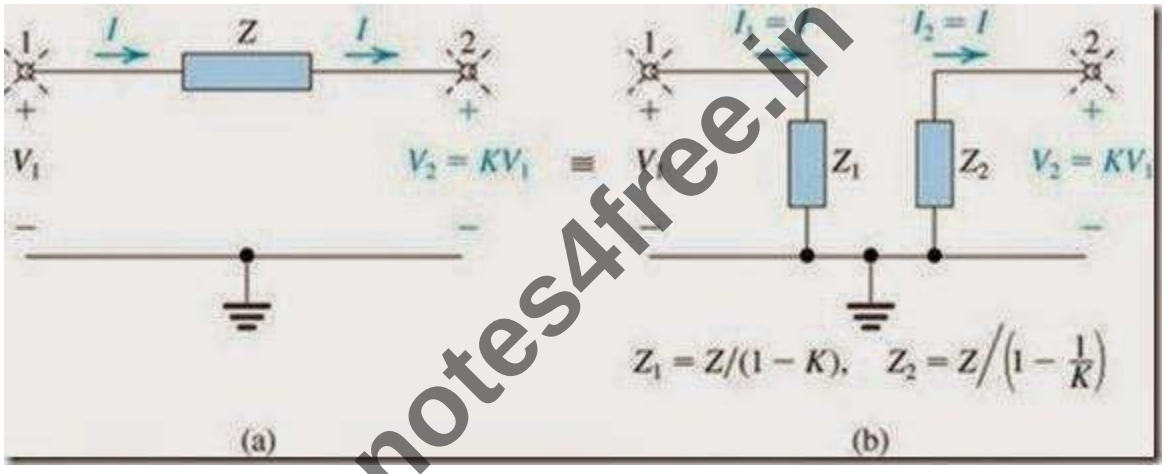


Fig. (20) Amplifier with C_f replaced by Miller's capacitances.

High Frequency Response of BJT amplifier:

In the high frequency response of BJT amplifier, the upper 3dB cut-off point is defined by the following factors.

(i) The network capacitance which includes the parasitic capacitances of the transistor and the wiring capacitances.
(ii) The frequency dependence of short circuit $C_E$current gain h_{f_e} or β.

Network Parameters:

Fig. (21) shows the RC coupled amplifier with parasitic and wiring capacitances. C_{be}, C_{bc} and C_{ce} are the parasitic capacitances of the transistor. C_{wi} and C_{wo} are

input and output wiring capacitances which are introduced during the construction of the amplifier circuit.

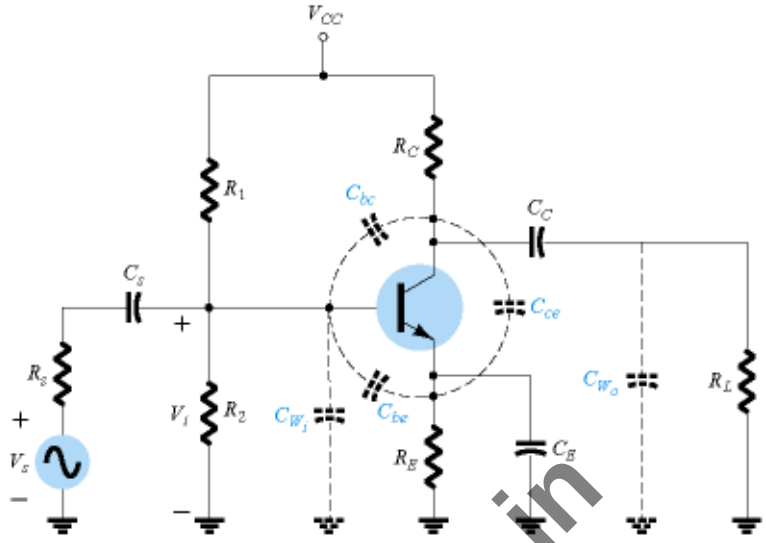


Fig. (21) RC- coupled amplifier with parasitic and wiring capacitances.

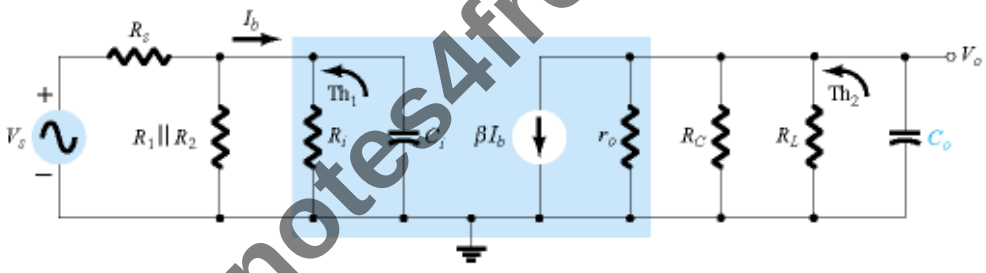


Fig. (22) shows the high frequency AC equivalent circuit of RC-coupled amplifier.

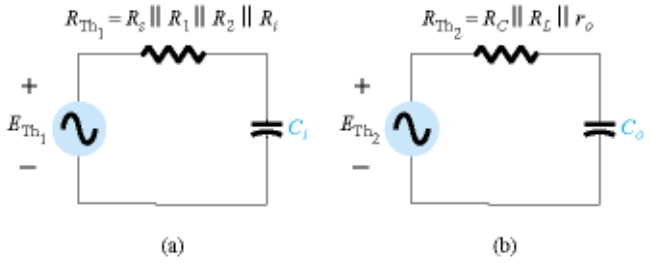


Fig. (23) High frequency AC equivalent circuit of amplifier of Fig. (22).

(i) Using Miller's theorem, the transit capacitance, C_{bc} can be replaced by two capacitances; C_{mi} at the input and C_{mo} at output.

(ii) The total capacitance C_i is the sum of C_{mi}, C_{be} and C_{wi}.
i.e. $C_i = C_{mi}+C_{be}+C_{wi}$ ----- (52)
where $C_{mi}=[1 - A_V]C_{bc}$ ----- (53)

(iii) The total output capacitance is the sum of C_{mo}, C_{ce} and C_{wo}.
i.e. $C_0 = C_{wo}+C_{ce}+C_{mo}$ ----- (54)
where $C_{m_o} = \left[1 + \frac{1}{A_V}\right] C_f$

Upper cut-off frequency due to C_i:

Apply voltage division rule to circuit of Fig. (22),

$E_{Thi} = V_s \left[\frac{R_1 \| R_2 \| \acute{R}_\iota}{R_S + R_1 \| R_2 \| \acute{R}_\iota}\right]$ ----- (56)

From circuit in Fig. (21);

$R_{Thi} = R_S + R_1 \| R_2 \| \acute{R}_\iota$ ----- (57)

Where $\acute{R}_\iota = \beta r_e$

From Fig. (29) (b), Apply V_g division rule,

$|V_i| = |E_{Thi}| \left[\frac{X_{C_i}}{\sqrt{(R_{Thi})^2+(X_{Ci})^2}}\right]$

$|V_i| = |E_{Thi}| \frac{|E_{Thi}|}{\sqrt{1+\left(\frac{R_{Thi}}{X_{Ci}}\right)^2}}$ ----- (58)

Where $X_{Ci} = \frac{1}{2\pi f C_i}$ ----- (59)

In the mid band, the effect of C_i is negligible. As a result, X_{Ci} can be treated as open circuit i.e. $X_{Ci} = \infty$.

Therefore $|V_i|_{mid} \approx |E_{Thi}|$

At high frequencies, C_i cannot be neglected with increase in f, X_{Ci} decreases, $\frac{R_{Thi}}{X_{Ci}}$ increases, $|V_i|$ decreases and hence the voltage gain decreases.

3dB cut-off occurs at a frequency at which

$|V_i| = \frac{|\text{Vi}|\text{mid}}{\sqrt{2}} = \frac{|E_{Thi}|}{\sqrt{2}}$

From (58), this condition occurs, when

$R_{Thi} = X_{Ci}$

$R_{Thi} = \frac{1}{2\pi f C_i}$

Or f= $f_{Hi} = \frac{1}{2\pi R_{Thi} C_i}$

$= \left[\frac{f}{f_{Hi}}\right]$

Therefore Eq. (58) becomes,

$|V_i| = \frac{|E_{Thi}|}{\sqrt{1+\left(\frac{f}{f_{Hi}}\right)^2}}$ ----- (62)

Thus, due to C_i, V_g gain decreases at the rate of 20dB/decade.

Upper cut-off frequency due to output capacitance C_O :

Consider the output circuit of Fig.(22) which is shown in Fig. (23).

βI_b, r_o and $R_C||R_L$ is connected to voltage source as shown in Fig. (22).

$R_{Tho} = r_o \ ||R_C||R_L$ ----- (63)

$E_{Tho} = [-\beta I_b]\ [r_o \ ||R_C||R_L]$ ----- (64)

Using the same procedure as listed above, we have

$|V_o| = \frac{|E_{Tho}|}{\sqrt{1+\left(\frac{R_{Tho}}{X_{Co}}\right)^2}}$ ----- (65)

Where $X_{Co} = \frac{1}{2\pi f C_o}$ ----- (66)

The output voltage in mid band is

$|V_o|_{mid} \approx |E_{Tho}|$ ----- (67)

The Upper 3dB cutoff frequency due to C_o is

$f_{HO} = \frac{1}{2\pi R_{Tho} C_o}$ ----- (68)

and magnitude of voltage gain is

$|A_V| = \frac{1}{\sqrt{1+\left(\frac{f}{f_{Ho}}\right)^2}}$ ----- (69)

Thus due to Co, Vg gain decreases at the rate of 20dB/ Decade.

Combined effect of C_i and C_O on high frequency response:

(i) The input capacitance C_i, defines upper cut-off frequency f_{Hi}.
(ii) The output capacitance C_o, defines another upper cut-off frequency f_{Ho}.
(iii) The lowest of these 2 frequencies will be taken as overall upper cut-off frequency.
(iv) If the variation of h_{fe} with frequency is considered then the actual cut-off frequency may be lower than f_{Hi} or f_{Ho}.

Variation of h_{fe} with frequency:

Fig. (24) shows hybrid-π high frequency small signal model of BJT.

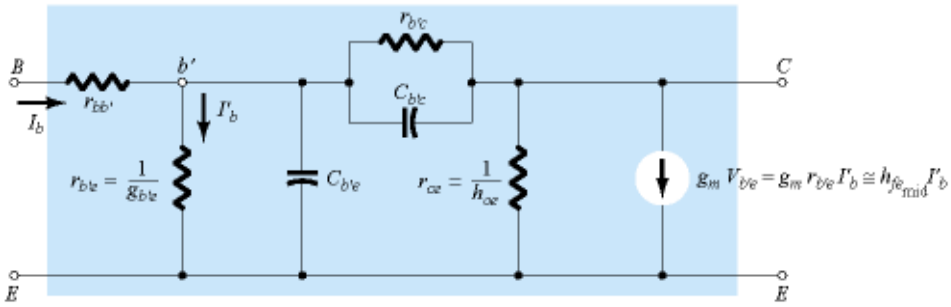


Fig. (24) Hybrid-π high frequency small signal model of BJT.

The B-E input capacitance C_π (C_{be}) and B-C depletion capacitance C_u (C_{bc}) makes the short circuit current gain h_{fe} to vary with frequency in high frequency region.

Expression for h_{fe} as a function of frequency:

Following assumptions are made:

(i) r_b is few tens of Ω. Hence it is treated as short circuit.
(ii) r_u is few tens of MΩ. Hence it is treated as open circuit.

To find h_{fe}, short the output terminals. The resulting circuit is shown in Fig. (24).

Fig. (24) circuit to find h_{fe}.

WKT, $h_{fe}=\frac{I_C}{I_b}\Big|V_{ce}=0$ ----- (70)

The current $g_m\, V_\pi$ flows into short circuit.

Therefore $I_C=g_m\, V_\pi$ ----- (71)

to find I_b FROM Fig 24

Let Z= $r_\pi \| \frac{1}{j\omega(C_\pi+C_u)}$ ----- (72)

Z=$\frac{r_\pi}{1+j\omega(C_\pi+C_u)\, r_\pi}$

Now, $V_\pi = I_b$ Z

$V_\pi = \frac{I_b r_\pi}{1+j\omega(C_\pi+C_u)\, r_\pi}$ ----- (73)

Substitute Eq. (73) in Eq. (71), we have

$I_C = \frac{g_m r_\pi}{1+j2\pi f(C_\pi+C_u)\, r_\pi}$ ----- (74)

Let $f_\beta = \frac{1}{2\pi(C_\pi+C_u)\, r_\pi}$ ----- (75)

Substitute Eq. (75) in Eq. (74), we have

$$h_{fe} = \frac{g_m r_\pi}{1+j\left(\frac{f}{f_\beta}\right)} \text{ ----- (76)}$$

$$|h_{fe}| = \frac{g_m r_\pi}{\sqrt{1+j\left(\frac{f}{f_\beta}\right)^2}} \text{ ----- (77)}$$

In the mid band, f << f_β, As a result $\left(\frac{f}{f_\beta}\right)^2$ <<1

From Eq. (77), we have

$|h_{fe}|_{\text{mid}} = g_m r_\pi = h_{fe\,\text{mid}}$ ----- (78)

$h_{fe\,\text{mid}}$ is also denoted by In β_{mid}.

Substitute Eq. (78) in Eq. (77),

$$|h_{fe}| = \frac{|h_{fe}|\text{mid}}{\sqrt{1+j\left(\frac{f}{f_\beta}\right)^2}} \text{ ----- (79)}$$

Eq. (79) gives the variation of $|h_{fe}|$ withfrequency.

(i) As f increases, $\left(\frac{f}{f_\beta}\right)^2$ increases and hence $|h_{fe}|$ decreases.

(ii) When f=f_β, =$|h_{fe}| = \frac{h_{fe}\text{mid}}{\sqrt{2}} = \frac{\beta_{mid}}{\sqrt{2}}$

f_β defines the upper 3dB cut-off point for short circuit current gain h_{fe}. f_β is also denoted by fh_{fe}. Eq. (75) can be written as

$$f_\beta = fh_{fe} = \frac{1}{2\pi(C_\pi + C_u)\, r_\pi} \text{ ----- (80)}$$

But, $r_\pi = \beta_{re} = \beta_{mid}\, r_e$

$$f_\beta = fh_{fe} = \frac{1}{2\pi\beta_{mid}\, r_e(C_\pi + C_u)} \text{ ----- (80)}$$

f_β is called β cut-off frequency. f_β is also the bandwidth for the short circuit current gain h_{fe}. Fig. (38) shows the variation of $|h_{fe}|$ with frequency. $|h_{fe}|$ decreases from its mid band value $h_{fe\text{mid}}$ with a slope of 20dB/decade.

Expression for gain band width product f_T:

f_T is the frequency at which $|h_{fe}|$ =1 or $|h_{fe}|_{dB}$ =0dB.

Using this in Eq. (79),

$$\left| \frac{h_{fe}\text{mid}}{\sqrt{1+j\left(\frac{f}{f_\beta}\right)^2}} \right|_{f=ft} = 1$$

$$\frac{h_{fe}\text{mid}}{\sqrt{1+j\left(\frac{f_T}{f_\beta}\right)^2}} \text{----- (82)}$$

Since $f_T >> f_\beta$, $\left(\frac{f_T}{f_\beta}\right)^2 >> 1$

Therefore $\sqrt{1+j\left(\frac{f_T}{f_\beta}\right)^2} \approx \frac{f_T}{f_\beta}$

Therefore Eq. (82) becomes

$$\frac{h_{fe}\text{mid}}{\frac{f_T}{f_\beta}} = 1$$

Or $f_T = f_\beta \; h_{fe}\text{mid} = \beta_{mid} \; f_\beta$ ----- (83)

Since $h_{fe}\text{mid}$ is the mid band short circuit current gain and f_β is the bandwidth, f_T is called gain-bandwidth product.

Eq. (81) in Eq. (83),

$$f_T = \beta_{mid} \times \frac{1}{2\pi\beta_{mid}\, r_e(C_\pi + C_u)} = \frac{1}{2\pi(C_\pi + C_u)\, r_e} \text{ ----- (84)}$$

Low frequency response of FET amplifier:

Consider a coomon source amplifier as shown in Fig. 25

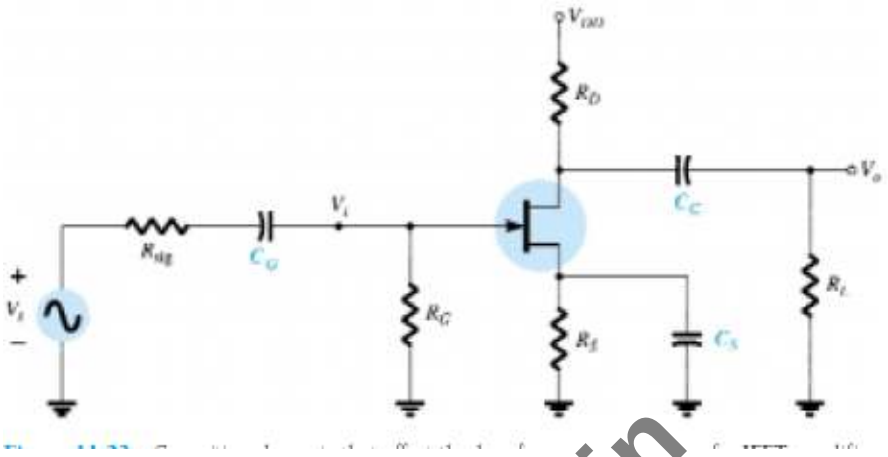


Fig 25 Capacitive elements that affect the low-frequency response of a JFET amplifier.

Effect of C_G on Low frequency response:

The lower cut-off frequency of this network is shown in fig 26

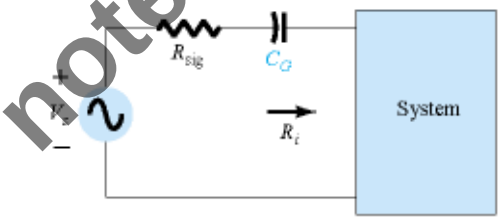


Fig 26 Determining the effect of CG on the low-frequency response.

$f_{C_G} = \frac{1}{2\pi(R_{sig}+R_i)C_G}$

Where $R_i = R_G \| R_{in(gate)}$

$R_{in(gate)} = \left| \frac{V_{GS}}{I_{GSS}} \right|$

I_{GSS} = gate reverse current

$R_G >> R_{sig}$ and $R_{in(gate)} >> R_G$

$R_i \approx R_G$

Therefore $f_{C_G} = \frac{1}{2\pi R_G C_G}$

Effect of C_C on Low frequency response:

Consider output part of equivalent circuit as shown in Fig 27

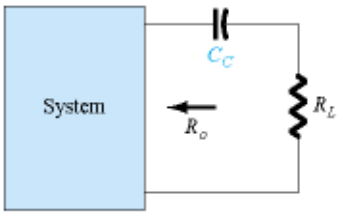


Fig 27 Determining the effect of Cc on the low-frequency response.

$R_o = r_d \parallel R_D$

Therefore $f_{L_C} = \frac{1}{2\pi(R_o+R_L)C_G}$

Effect of C_S on Low frequency response:

Consider the RC network shown in Fig 28 formed by C_S and let R_{eq} be the resistance looking in at the source.

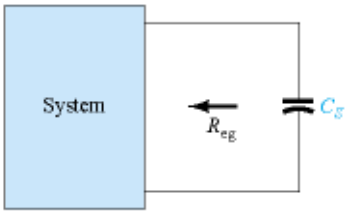


Fig 28 Determining the effect of CS on the low-frequency response.

$f_{L_S} = \frac{1}{2\pi(R_{eq})C_S}$

$R_{eq} = \frac{R_S}{1+R_S(1+g_m r_d)|\,(r_d+R_D||R_L)}$

$= R_S \parallel \frac{1}{g_m}$

Therefore $r_d >> R_D$

High Frequency Response FET amplifier:

Fig. 29 shows CS JFET amplifier with inter electrode capacitances and wiring capacitances. The capacitors C_{gs} and C_{gd} vary from 1pF, whereas the capacitance C_{ds} is smaller ranging from 0.1pF to 1pF.

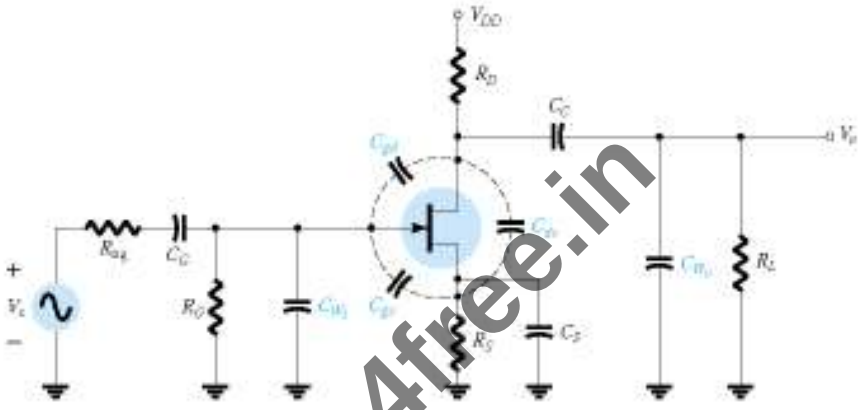


Fig 29 Capacitive elements that affect the high frequency response of a JFET amplifier

Fig. 30 shows high-frequency AC equivalent circuit. At high frequencies, C_i will approach a short circuit equivalent and V_{gs} will drop in value and reduce the overall gain. At frequencies where C_o approaches its short circuit equivalent, the parallel output voltage Vo will drop in magnitude.

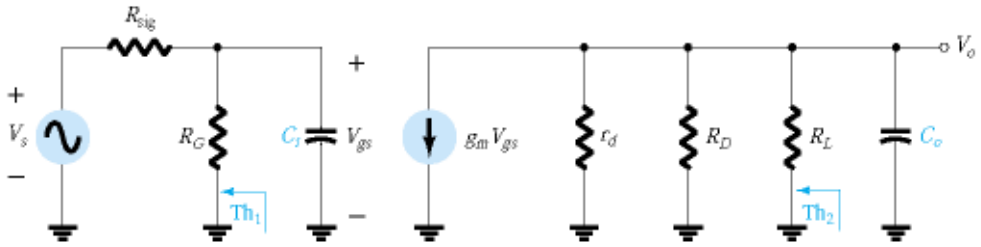


Fig 30 High-frequency ac equivalent circuit for Fig. 29.

Effect of C_i on high frequency response:

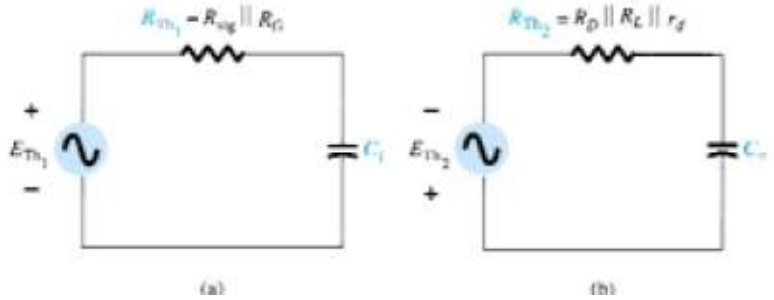


Fig 31 The Thévenin equivalent circuits for the (a) input circuit and (b) output circuit.

$$f_{H_i} = \frac{1}{2\pi(R_{Thi})C_i}$$

Where $R_{Thi} = R_{sig} \parallel R_G$

$C_i = C_{wi} + C_{gs} + (1 - A_V)C_{gd}$

Effect of C_o on high frequency response:

$$f_{H_o} = \frac{1}{2\pi(R_{Tho})C_o}$$

Where $R_{Tho} = r_d \parallel R_D \parallel R_L$

$C_o = C_{wo} + C_{ds} + (1 - 1/A_V)C_{gd}$

Multistage Frequency Effects:

For a second transistor stage connected directly to the output of a first stage, there will be a significant change in the overall frequency response. In the high frequency region, the output capacitance C_O must include the wiring capacitance (C_{W1}), parasitic capacitance (C_{be}) and miller capacitance (C_{mi}) of the following stage. There will be additional low frequency cut-off levels due to the 2nd stage, which will further reduce the overall gain of the system in the region. For each additional stage, the upper cutoff frequency will be determined by the stage having the lowest cutoff frequency. The low frequency cutoff is determined by the stage

having the highest low-frequency cutoff frequency. The multistage amplifier frequency response is shown in Fig 32.

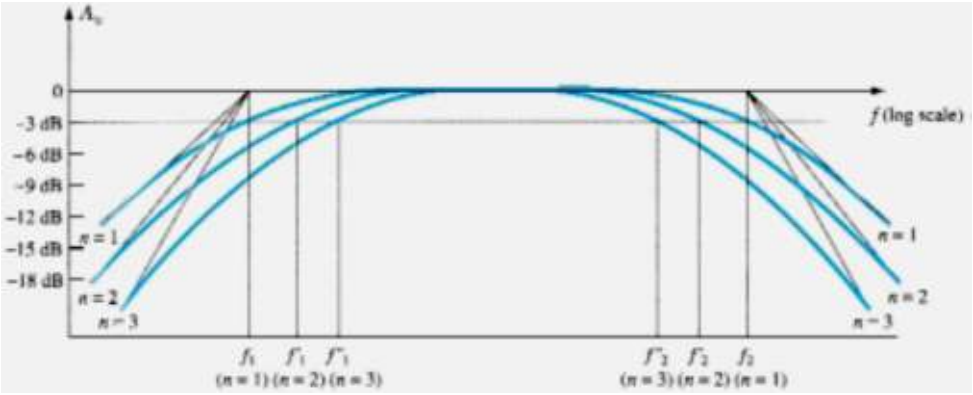


Fig 32 Effect of an increased number of stages on the cutoff frequencies and the bandwidth.

Assuming identical stage, for low frequency region

$A_{V\ low_{(overall)}} = A_{V1\ low}\ \ A_{V2\ low}$ ---------- $A_{Vn\ low}$

Since all stages are identical, $A_{V1\ low} = \ A_{V2\ low}$ = etc.

Therefore $A_{V\ low_{(overall)}} = \left(A_{V1\ low}\right)^n$

Or $\frac{A_{V\ low_{(overall)}}}{A_{V\ mid\ (overall)}} = \left(\frac{A_{V\ low}}{A_{V\ mid}}\right)^n = \frac{1}{\left(1-j\frac{f_1}{f}\right)^n}$

At 3dB frequency

$$\frac{1}{\sqrt{\left(1+j\left(\frac{f_1}{f}\right)^2\right)^n}} = \frac{1}{\sqrt{2}}$$

$$\left(1+\left(\frac{f1}{f}\right)^{1/2}\right)^n = 2^{1/2}$$

$$f1' = \frac{f1}{\sqrt{2^{1/n}-1}}$$

Similarly $f2' = \sqrt{2^{1/n}-1}$ f2

Module 4: Feedback and Oscillator Circuits

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SYLLABUS

Feedback concepts, Feedback connection types, Practical feedback circuits, Oscillator operation, FET Phase shift oscillator, Wein bridge oscillator, Tuned Oscillator circuits, Crystal oscillator, UJT construction, UJT Oscillator.

Courtesy:

Robert L. Boylestad and Louis Nashelsky, "Electronics Devices and Circuit Theory", Pearson, 10th Edition, 2012, ISBN: 978-81-317-6459-6.

Adel S. Sedra and Kenneth C. Smith, "Micro Electronic Circuits Theory and Applications," Oxford University Press, 5th Edition, ISBN:0198062257.

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Feedback Concepts:

Feedback plays an important role in every system. Majority of practical electronics systems and circuits employ feedback. Feedback in electronic circuits can be of two types

1. Positive Feedback 2. Negative Feedback

1. Positive Feedback

Here feedback voltage adds to the incoming input OR feedback voltage has same phase as that of incoming signal. Positive Feedback is used for generation of oscillations. All oscillators employ positive Feedback. Figure 4.1 illustrates Positive feedback. Any feedback system comprises of Amplifier and a feedback network. Amplifier amplifies the incoming signal. Feedback network attenuates the output signal and generates feedback signal. A- Gain of open-loop Amplifier and β- Gain of Feedback network.

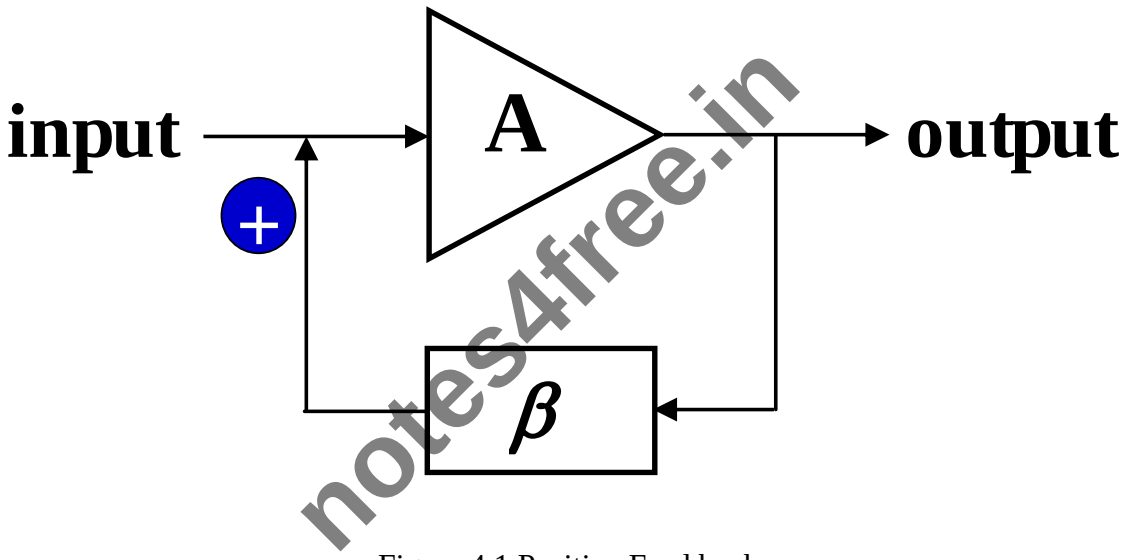

Figure 4.1 Positive Feed back

2. Negative Feedback

Here feedback voltage subtracts from the incoming input signal OR feedback voltage has opposite phase as that of incoming signal. Negative Feedback is used for amplification of input signal. Amplifiers employ negative Feedback. Figure 4.2 illustrates Negative feedback. Any Negative feedback system comprises of open loop Amplifier and a feedback network. Amplifier amplifies the incoming signal. Feedback network attenuates the output signal and generates feedback signal. A- Gain of open-loop Amplifier and β- Gain of Feedback network.

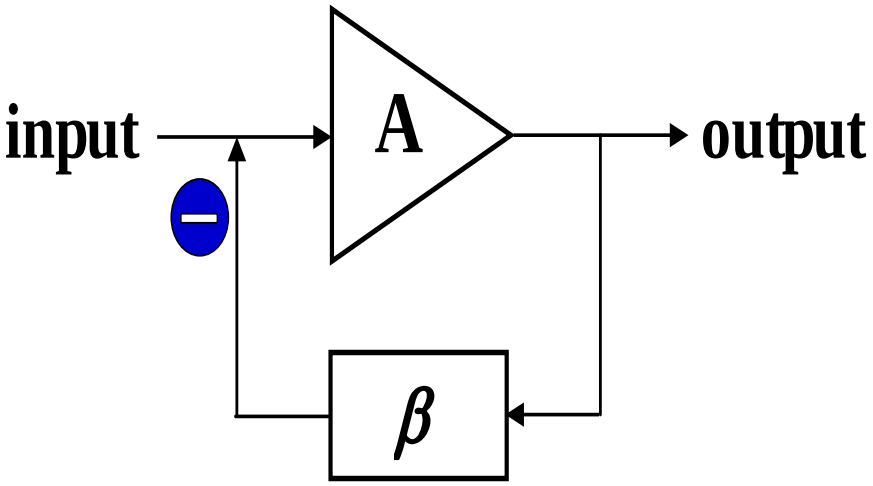

Figure 4.2 Negative feedback

Concepts of Negative feedback

A typical feedback connection is shown in Figure 4.3. The input signal Vs is subtracted with a feedback signal Vf. The difference of these signals Vi is the input voltage to the amplifier. A portion of the amplifier output Vo is connected to the feedback network (β), which provides a reduced portion of the output as feedback signal at the input.

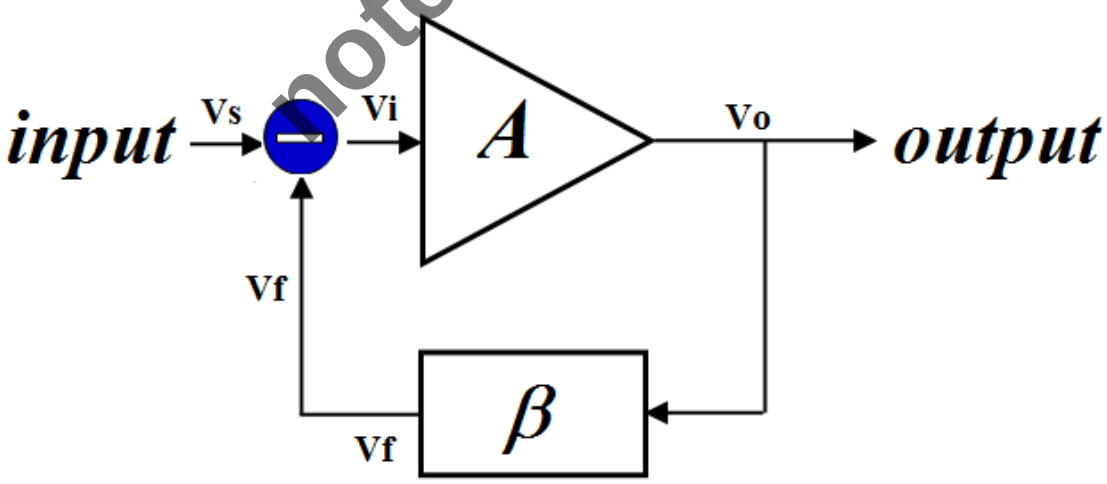

Figure 4.3 Feedback Amplifier

Overall Gain of the closed loop system shown in the above Figure 4.3 is given by,

$$Af = \frac{V_O}{V_S} = \frac{A}{1+A\beta} \quad \text{.....(1)}$$

Af denotes the closed loop gain OR gain with feedback

Negative feedback results in reduced gain but results in lot of improvements:

Advantages :

4. Higher input impedance

2. More stable gain

3. Improved frequency response

4. Lower output impedance

5. Reduced noise

6. More linear operation

Feedback Connection Types

Depending on whether voltage OR current is subjected to feedback and feedbacks mixing at the input, feedback circuits are classified into four types:

- Voltage-series feedback
- Voltage-shunt feedback
- Current-series feedback
- Current- Shunt feedback

1) Voltage-series feedback

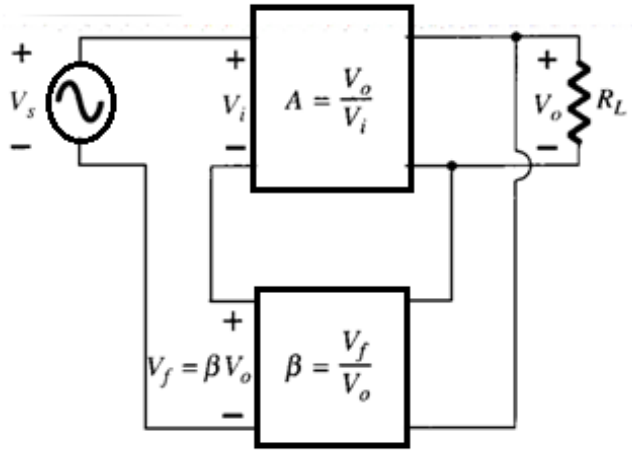

Figure 4.4 Voltage series feedback

Here part of output voltage is fed as input to the feedback network; Output of feedback network mixes in series with the input signal voltage. Series feedback connection increases the input impedance. Voltage feedback at output reduces the output impedance. Voltage amplifiers employ this feedback connection.

Gain with feedback is given by,

$$Af = \frac{V_O}{V_S} \text{.....(2)}$$

Analysis of Voltage Series Feedback To Find Closed Loop Gain

In the above Figure 4.4,

$$V_i = V_s - V_f \text{..... (3)}$$

Since,

$$V_o = AV_i = A(V_s - V_f) = AV_s - AV_f$$

$$V_o = AV_s - A(\beta V_o)$$

then

$$(1 + \beta A)V_o = AV_s$$

Therefore, the Overall voltage gain with feedback is

$$Af = \frac{V_o}{V_S} = \frac{A}{1+A\beta} \text{..... (4)}$$

Input impedance of Voltage series feedback

Detailed block diagram of voltage series feedback connection is shown in Figure 4.5

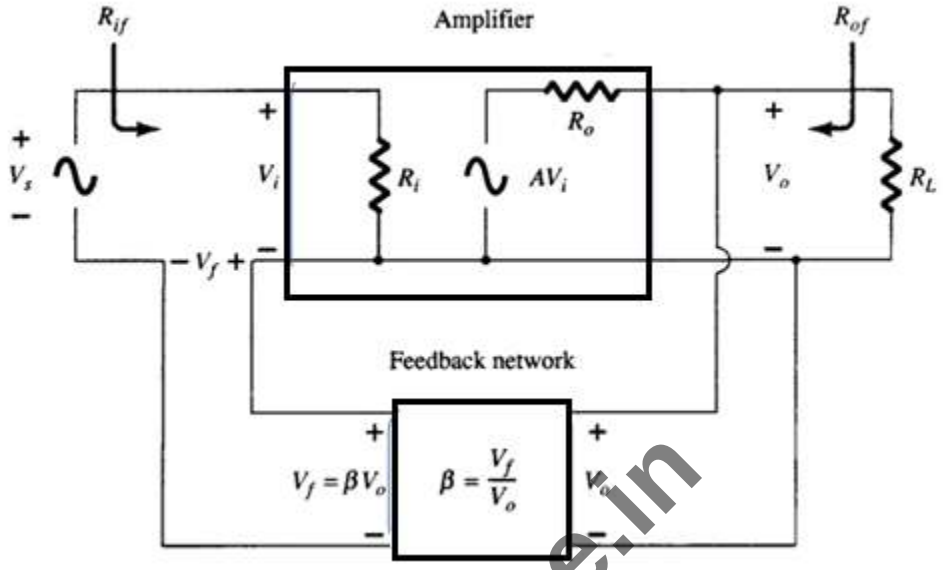

Figure 4.5 Voltage series feedback with more details

Input impedance can be derived as,

$Ii = Vi/Zi = Vs - Vf/Zi$

$= Vs - \beta Vo/Zi$

$= Vs - \beta AVi/Zi$

$IiZi = Vs - \beta AVi$

$Vs = IiZi + \beta AVi = IiZi + \beta AIiZi$

$Zif = Vs/Ii$

$= Zi + (\beta A)Zi$.....(5)

Output impedance of Voltage series feedback

The output impedance is determined by applying a voltage V, at the o/p resulting in a current I , with V_s shorted out (V_s = 0). Figure 4.6 shows the section of output of amplifier.

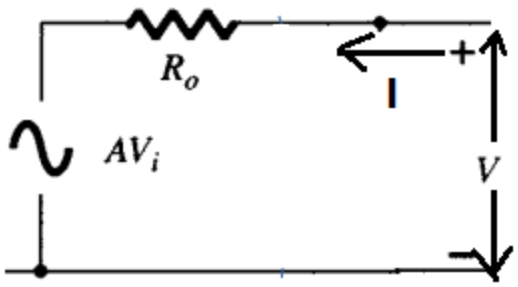

Figure 4.6 Network at the output of amplifier with test input V.

The voltage V is then given by

$$V = IZ_o + AV_i$$

For $V_s = 0$, $V_i = -V_f$

Which implies, $V = IZ_o - AV_f = IZ_o - A(\beta V)$

Rewriting the equation as

$$V + \beta AV = IZ_o$$

$$Zof=V/I=Zo/(1+A\beta).....(6)$$

2) Voltage-shunt feedback Configuration

Here output voltage is fed back to feedback network and feedback signal is connected in parallel with the input current source. Shunt feedback connection decreases the input impedance. Voltage feedback at output also reduces the output impedance. Transresistance amplifiers employ this type feedback connection.

$$Af=Vo/Is.....(7)$$

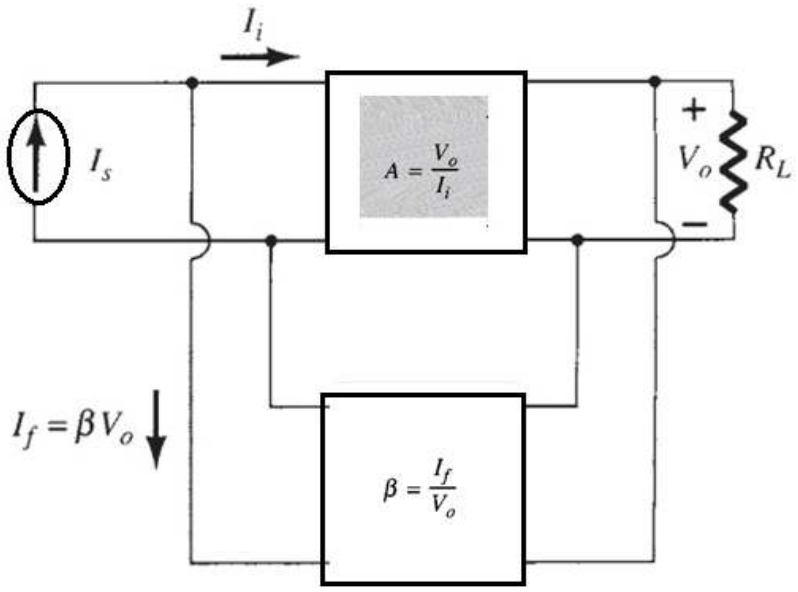

Figure 4.7 Voltage shunt feedback configuration

Gain with Voltage-shunt feedback Configuration

Overall Gain OR Gain with feedback can be expressed as,

Af =Vo/Is

=AIi/(Ii +If)

=AIi/(Ii +βVo)

=AIi/(Ii +βAI)

Af =$\frac{A}{1+A\beta}$.....(8)

Input impedance with Voltage-shunt feedback Configuration

To determine input impedance, the Figure 4.7 can be redrawn as,

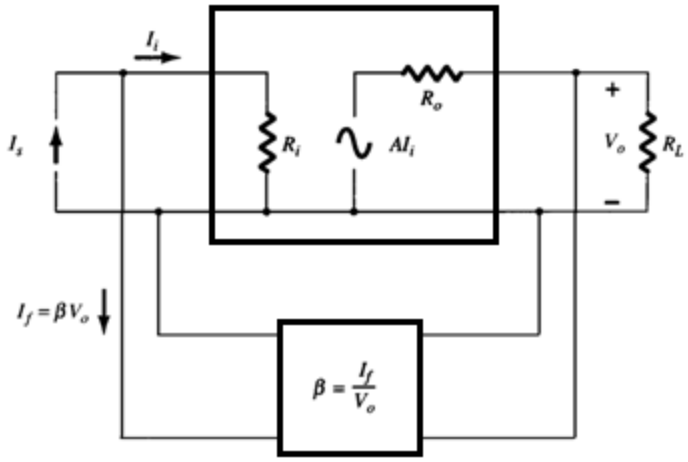

Figure 4.8 Voltage shunt feedback configuration with details

From, the Figure 4.8,

Zif =Vi/Is

=Vi/(Ii +If)

=Vi/(Ii +βVo)

=(Vi/Ii)/((Ii/Ii)+β(Vo/Ii))

Zif =Zi/1+βA .....(9)

3) Current-series feedback Configuration

Here current from output is feedback to input. The fed back signal is mixed in series with the input current. Series feedback connection increases the input impedance. Current feedback at output also increases the output impedance. Transconductance amplifiers employ this type feedback connection.

Overall Gain or Gain with feedback can be expressed as,

Af= Io /Vs..... (40)

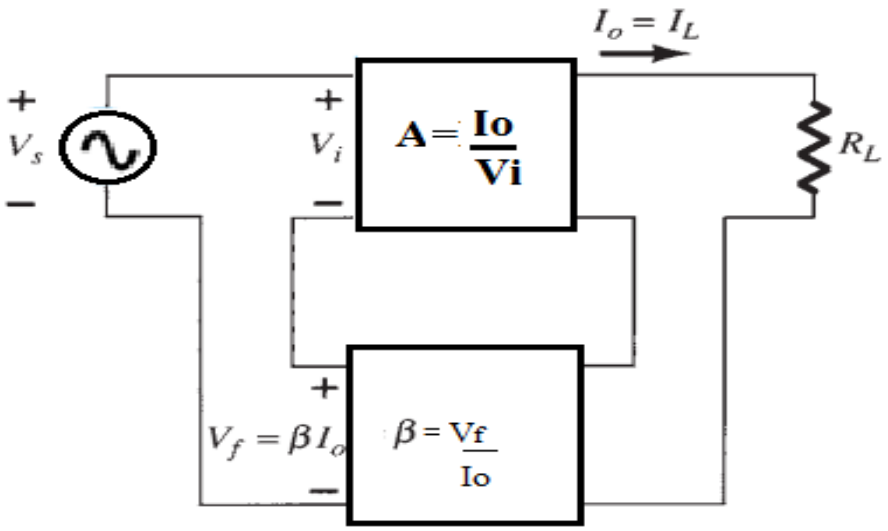

Figure 4.9 Current series feedback

Output impedance of current series feedback configuration

To determine output impedance the current series feedback configuration can be drawn as shown in Figure 4.10

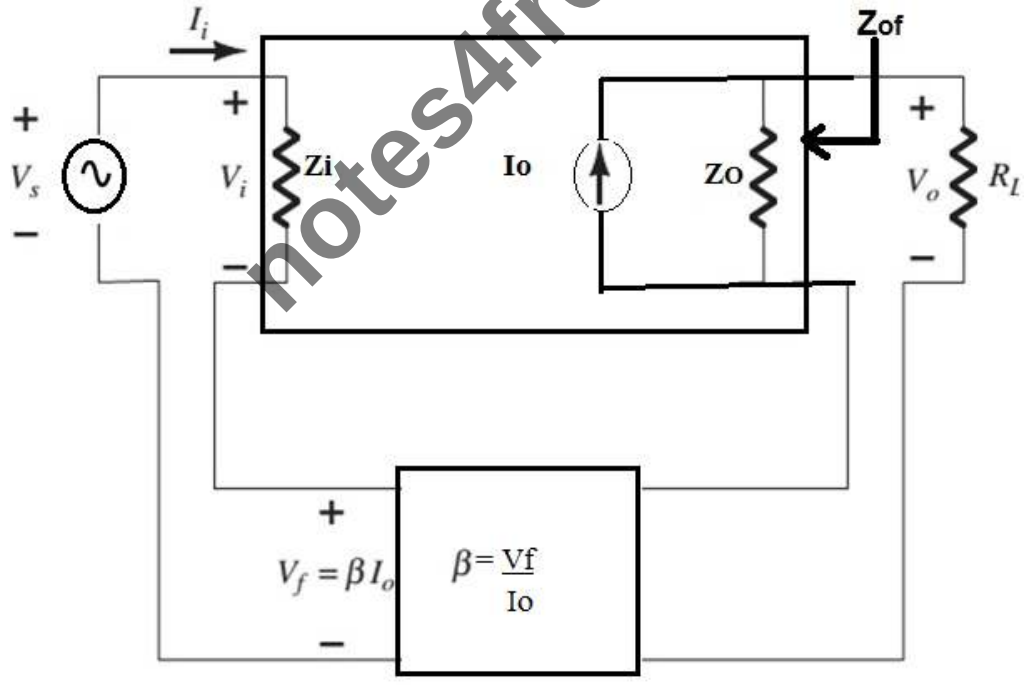

Figure 4.10 current series feedback configuration in detail

Output impedance is determined by applying a test signal V to the output with V_s shorted out (V_s =0), resulting in a current I, the ratio of V to I being the output impedance. The circuitry at the output is redrawn as shown in the Figure 4.11

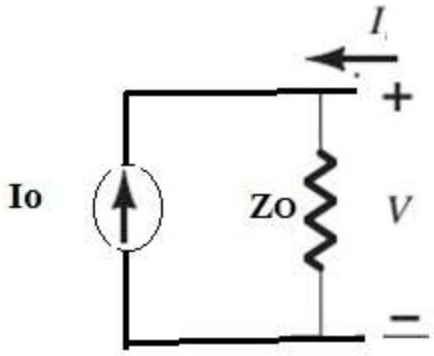

Figure 4.11 Output section of current series feedback configuration

With Vs=0,

Vi =Vf

I =(V/Zo)-AVi

=(V/Zo) -AVf

=(V/Zo)-AβI

Zo(4 +βA)I =V

Zof=V/I=Zo(1+Aβ).....(11)

4) Current-shunt feedback Configuration

Here current is fed to feedback network. Fed back signal is mixed in parallel with the input current source. Shunt feedback connection decreases the input impedance. Current feedback at output increases the output impedance.This topology is applied in current amplifiers.

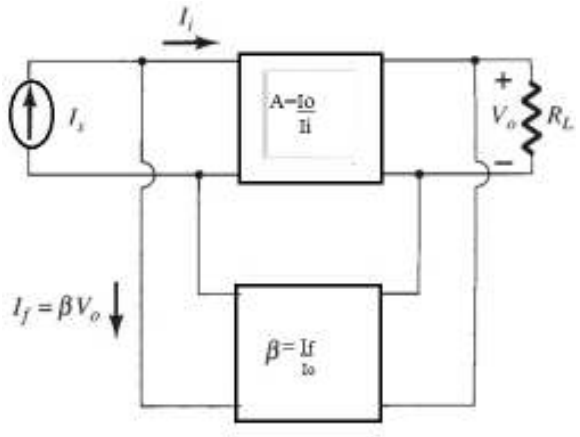

Figure 4.12 Current shunt feedback configurations

Here Overall Gain OR Gain with feedback can be expressed as,

$$Af = Io / Is$$

Frequency Distortion with Feedback (Reduction in Frequency Distortion)

- If loop gain $A\beta >> 1$, then closed loop gain becomes, $Af \equiv 1/\beta$

  Thus if the feedback network is purely resistive then closed loop gain becomes independent of reactive components although amplifier has a reactive response.

Noise and Nonlinear Distortion (Reduction in Noise and Nonlinear Distortion)

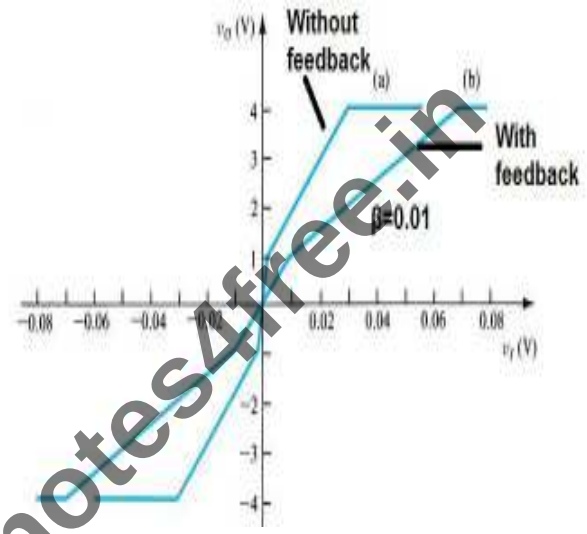

Figure 4.13 Reductions in Non-Linear Distortion

Application of negative feedback makes the system more linear. In Figure 4.13, Curve (a) shows transfer characteristic without negative feedback. Curve (b) shows the curve with negative feedback of β=0.01. We can see that The amplifier transfer characteristic can be considerably linearized (through the application of negative feedback). Thus large changes in open-loop gain (1000 to 100 in this case) give rise to much smaller corresponding changes in the closed-loop gain We can say that Feedback reduces noise and non-linear distortion

Effect of Negative Feedback on Gain and Bandwidth

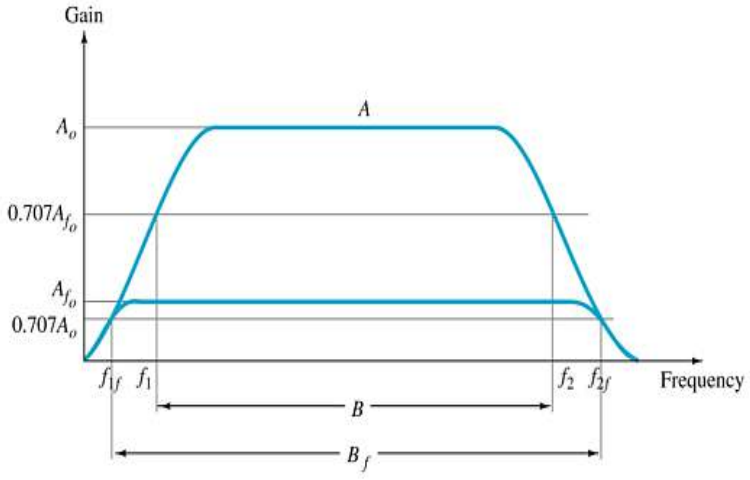

Figure 4.14 Effect of negative feedback on Bandwidth

Negative feedback results in improved Bandwidth. If f_1 is the lower cutoff frequency without feedback then we can see that it is pre-poned. New lower cutoff frequency is given by

$f_{1f} = f_1/(1+A\beta)$....(12)

. If f_2 is the upper cutoff frequency without feedback then we can see that it is postponed. New upper cutoff frequency is given by

$f_{2f} = (1+A\beta)f_2$..... (13)

Thus overall Bandwidth is improved by Negative feedback. B_f is more than B.

Gain Stability with Feedback

Gain becomes more stable with feedback. From equation (4), we can deduce that,

$$\left|\frac{dAf}{Af}\right| = \frac{1}{|1+\beta A|}\left|\frac{dA}{A}\right|$$

$$\left|\frac{dAf}{Af}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| \quad for\ \beta A >> \cdots (14)$$

This shows that the Magnitude of the relative change in gain $\left|\frac{dAf}{Af}\right|$ is reduced more by the factor $|\beta A|$ compared to that of without feedback$\left(\left|\frac{dA}{A}\right|\right)$. This can be illustrated by the problem.

Thus effect of negative feedback can be summarized as,

Table 1: Effect of Negative feedback

Parameter	Voltage series	Current Series	Voltage Shunt	Current shunt
Gain with feedback	**Decreases**	**Decreases**	**Decreases**	**Decreases**
Stabilty	**Improves**	**Improves**	**Improves**	**Improves**
Frequency Response	**Improves**	**Improves**	**Improves**	**Improves**
Frequency Distortion	**Decreases**	**Decreases**	**Decreases**	**Decreases**
Noise and non linear distortion	**Decreases**	**Decreases**	**Decreases**	**Decreases**

Practical feedback circuits

Voltage-Series Feedback:

Let us study the voltage series feedback by the following circuits shown in Figures 4.15, 4.16 and 4.17:

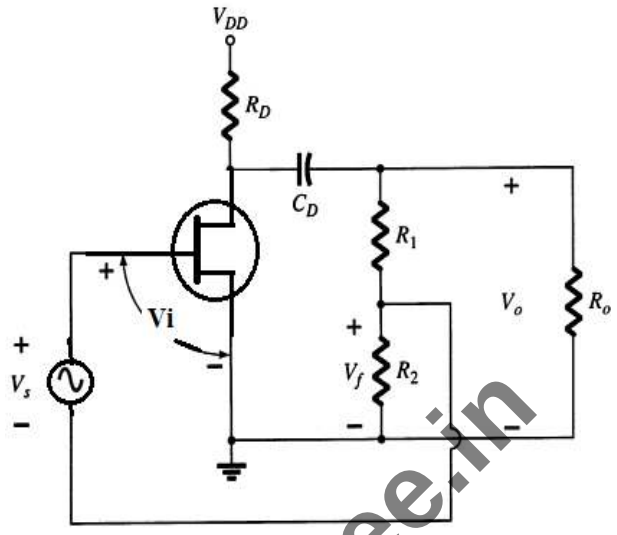

Figure 4.15 Practical Voltage Series Feedback

Figure 4.15 shows an FET amplifier stage with voltage-series feedback. A part of the output signal (V_o) is obtained using a feedback network of resistors R_1 and R_2. The feedback voltage V_f is connected in series with the source signal V_s,

Without feedback the amplifier gain is

$$A = \frac{Vo}{Vi} = -g_m R_L \text{..... (15)}$$

where R_L is the parallel combination of resistors:

$$R_L = R_D\, R_o\, (R_1 + R_2) \text{ ----------(16)}$$

The feedback network provides a feedback factor of

$$\beta = \frac{Vf}{Vo} = \frac{-R2}{R1+R2} \text{.....(17)}$$

Using the values of A and β above in Eq. For series feedback gain , we find the gain with negative feedback to be

$$Af = \frac{1}{1+\beta A} = \frac{-g_m R_L}{1+\left[\frac{R2R_L}{R1+R2}\right] g_m} \ldots\ldots\ldots\ldots\ldots (18)$$

If βA >> 1, we have,

$$Af \cong \frac{1}{B} = -\frac{R1+R2}{R2} \ldots\ldots\ldots (19)$$

Problem.

1. Calculate the gain without and with feedback for the FET amplifier circuit with the following circuit values: R1 =80 kΩ, R2 =20 kΩ, Ro =10 kΩ, RD=10 kΩ, and gm=4000 μS .

Solution:

$$R_L \cong \frac{R_o R_D}{R_o + R_D} = \frac{10\,\text{k}\Omega(10\,\text{k}\Omega)}{10\,\text{k}\Omega + 10\,\text{k}\Omega} = 5\,\text{k}\Omega$$

Neglecting the 100-kΩ resistance of R_1 and R_2 in series gives

$$A = -g_m R_L = -(4000 \times 10^{-6}\,\mu\text{S})(5\,\text{k}\Omega) = \mathbf{-20}$$

The feedback factor is

$$\beta = \frac{-R_2}{R_1 + R_2} = \frac{-20\,\text{k}\Omega}{80\,\text{k}\Omega + 20\,\text{k}\Omega} = -0.2$$

The gain with feedback is

$$A_f = \frac{A}{1 + \beta A} = \frac{-20}{1 + (-0.2)(-20)} = \frac{-20}{5} = \mathbf{-4}$$

Voltage series Feedback using OPAMP

Here op-amp is connected in a Non-inverting amplifier mode. Input signal is applied to Non-inverting terminal. Output voltage is feedback via potential divider network to inverting terminal. Op-amp amplifies difference between its Non-Inverting and Inverting terminals.

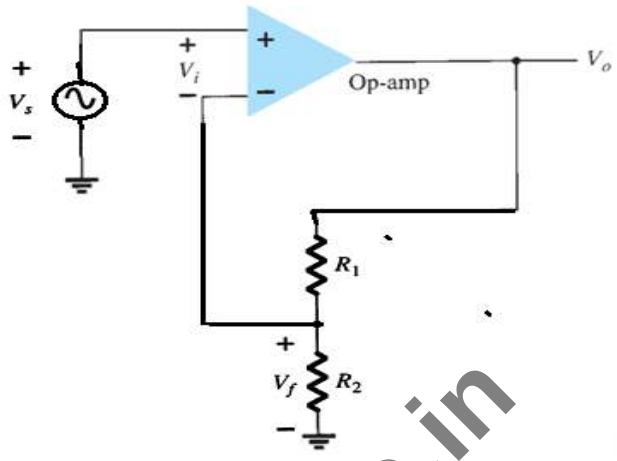

Figure 4.16 Voltage series feedback using OPAMP

Here,

Gain of feedback network is given by, $\beta = \frac{R2}{R1+R2}$ ... ... (20)

Voltage Series Feedback Emitter Follower:

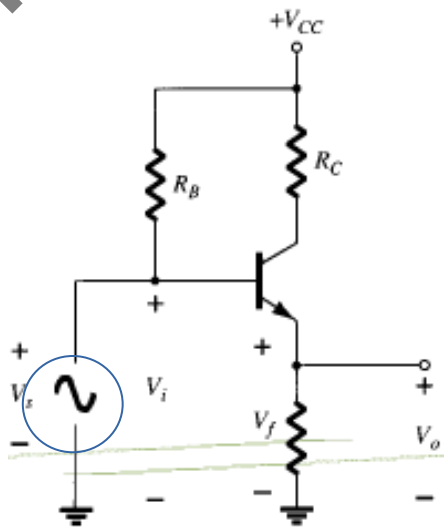

Figure 4.17 Voltage Series Feedback Emitter Follower

The emitter-follower circuit of Fig. 4.17 provides voltage-series feedback. The signal voltage V_s is the input voltage V_i. Resistor R_E acts as feedback resistor and also as a output resistance. The output voltage V_o subtracts in series with the input voltage. The amplifier, as shown in Fig. 4.18, provides the operation with feedback.

The operation of the circuit without feedback provides $V_f = 0$, so that

$$A = \frac{Vo}{Vs} = \frac{h_{fe} I_b R_E}{Vs} = \frac{h_{fe} R_E (\frac{Vs}{h_{ie}})}{Vs} = \frac{h_{fe} R_E}{h_{ie}} \quad \text{.....(21)}$$

and

$$\beta = \frac{Vf}{Vo} = 1 \ldots\ldots\ldots (22)$$

The operation with feedback then provides that,

$$Af = \frac{Vo}{Vs} = \frac{A}{1+BA} = \frac{h_{fe} R_E / h_{ie}}{1+(1)(h_{fe} R_E / h_{ie})} = \frac{h_{fe} R_E}{h_{ie} + h_{fe} R_E} \text{.....(19)}$$

for $h_{fe} R_E >> h_{ie}$

$$Af \cong 1$$

Current-series feedback:

Let us study the current series feedback by the following circuit shown in Figure 4.18.

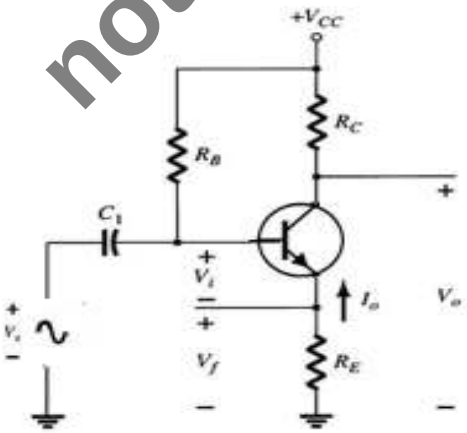

Figure 4.18 Practical Current series feedback

Transistor amplifier is an example of Current series feedback. Resistor R_E acts as a feedback resistor as it is common to input and output sections of amplifier. Here Effective voltage at input increases/decreases depending on feedback voltage. This effective voltage at input further alters the input current in proportion which brings changes in output voltage in proportion.

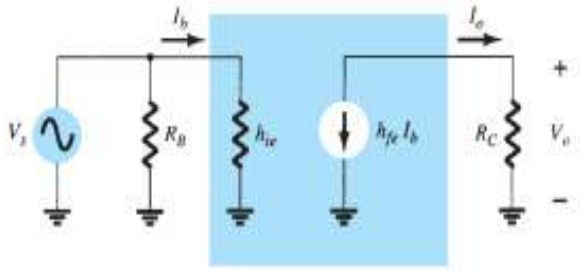

Figure 4.19 AC equivalent of amplifier without feedback

$$A = \frac{Io}{Vi} = \frac{h_{fe}\, I_b}{h_{ie} Re} \ldots\ldots\ldots (23)$$

$$\beta = \frac{Vf}{Io} = \frac{-IoRe}{Io} = -Re \ldots\ldots\ldots (24)$$

$$Zi = R_B || (h_{ie} + Re) \cong h_{ie} + Re$$

Zo = Rc

The input and output impedances are calculated as specified in summary table :

$$Zif = Zi(1 + \beta A) \cong h_{ie}\left(1 + \frac{h_{fe} Re}{h_{ie}}\right) = h_{ie} + h_{fe} Re \ldots\ldots\ldots (25)$$

$$Zof = Zo(1 + \beta A) = Rc\left(1 + \frac{h_{fe} Re}{h_{ie}}\right) \ldots\ldots (26)$$

The voltage gain A with feedback is

$$Avf = \frac{Vo}{Vs} = \frac{IoRc}{Vs} = \left(\frac{Io}{Vs}\right) Rc = AfRc \cong \frac{-h_{fe} Rc}{h_{ie} + h_{fe} Re} \ldots\ldots (27)$$

Voltage-shunt Feedback:

Let us study the Voltage-shunt feedback by the circuit shown in Figures 4.20 and 4.21. In Figure 4.20 Voltage-Shunt Feedback is demonstrated using op-amp. Here op-amp is connected in a Inverting amplifier mode. Input signal is applied to Inverting terminal. Output voltage is feedback via potential divider network to the Non-inverting terminal. Op-amp amplifies difference between its Non-Inverting and Inverting terminals. Output voltage is fed back in parallel with the input.

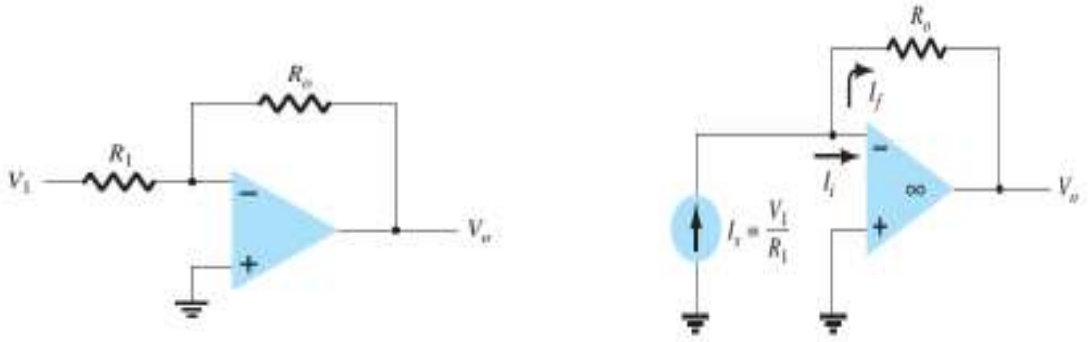

Figure 4.20 Voltage Shunt Feedback using OPAMP

The constant-gain op-amp circuit of Figure 4.21 provides voltage-shunt feedback. Referring to Figure 4.21 and the op-amp ideal characteristics $I_i = 0$, $V_i = 0$, and voltage gain of infinity, we have

$$A = \frac{Vo}{Ii} = \infty$$

$$\beta = \frac{I_f}{Vo} = \frac{-1}{Ro}$$

The gain with feedback is then

$$Af = \frac{Vo}{Is} = \frac{Vo}{Ii} = \frac{A}{1+\beta A} = \frac{1}{\beta} = -Ro$$

This is a transfer resistance gain. The more usual gain is the voltage gain with feedback,

$$Avf = \frac{Vo}{Is}\frac{Is}{V1} = (-Ro)\frac{1}{R1} = \frac{-Ro}{R1}$$

Voltage-Shunt Feedback using FET

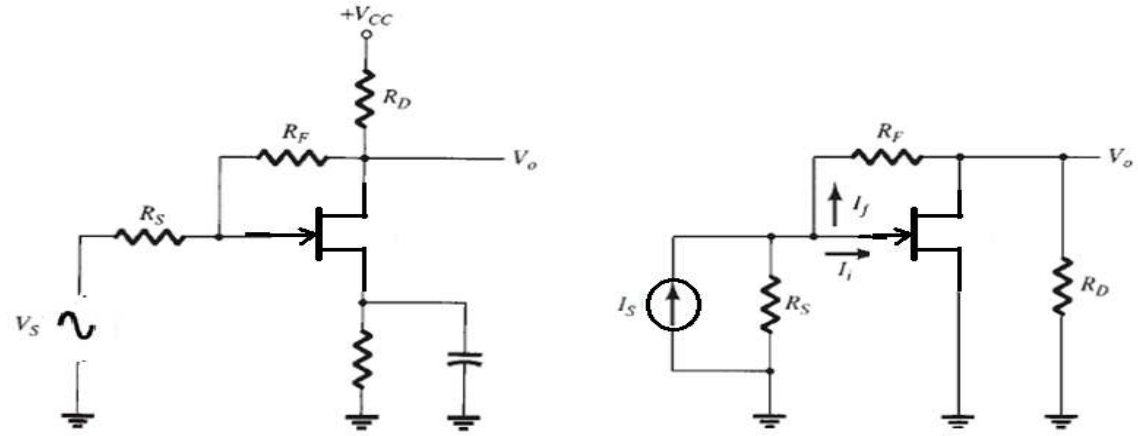

Figure 4.21 Voltage Shunt Feedback using FET

The circuit of Fig. 4.21 is a voltage-shunt feedback amplifier using an FET. Resistor R_F acts as a feedback resistor and is present between Drain and Gate of FET. Output voltage is fed back in parallel with the input.

with no feedback, $V_f = 0$.

$$A = \frac{Vo}{Ii} \cong -g_m R_D R_s$$

The feedback is

$$\beta = \frac{I_f}{Vo} = \frac{-1}{R_f}$$

With feedback, the gain of the circuit is

$$Af = \frac{Vo}{Is} = \frac{A}{1+BA} = \frac{-g_m R_D R_s}{1+\left(-\frac{1}{R_F}\right)(-g_m R_D R_S)} = \frac{-g_m R_D R_s R_F}{R_f + g_m R_D R_s} \ldots\ldots\ldots (28)$$

The voltage gain of the circuit with feedback is then

$$A_{vf} = \frac{Vo}{Is}\frac{Is}{Vs} = \frac{-g_m R_D R_s R_F}{R_f + g_m R_D R_s}\left(\frac{1}{Rs}\right) \ldots\ldots (29)$$

$$= \frac{-g_m R_D R_F}{R_f + g_m R_D R_s} = (-g_m R_D)\frac{R_F}{R_F + g_m R_D R_s} \ldots (30)$$

Current shunt feedback

Let us study the Current-shunt feedback by the circuit shown in Figures 4.22. In the circuit of Figure 4.22 two transistor amplifiers are cascaded to have more current gain. Feedback from 2nd transistors Emitter to 1st transistors Base.

At input side $I_i = I_s - I_f$.....(31)

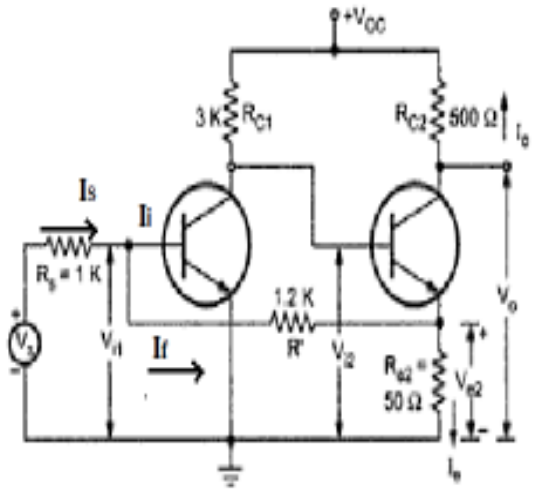

Figure 4.22 Current Shunt Feedback using transistors

Stability problem in feedback amplifiers

Usually both Amplifier and feedback network are reactive in nature, Then, Closed loop transfer function is given by

$$Af(s) = \frac{A(s)}{1 + A(s)\beta(s)}$$ Where, s =jw,

In Negative feedback, Feedback network produces signal which is 180^o out of phase with input.

At a Certain frequency, the total loop phase shift becomes 180^o, Therefore net phase shift will be 360^o. Therefore Loop Gain becomes,

$$L(j\omega) = A(j\omega)\beta(j\omega) = -1$$.

The feedback is thus positive and the amplifier, itself, becomes unstable and begins to break into oscillations due to positive feedback. If the amplifier oscillates at some low or high frequency, it is no longer useful as an amplifier. Proper feedback-amplifier design requires that the circuit will be stable at all frequencies, not merely those in the range of interest. Otherwise, a transient disturbance could cause a seemingly stable amplifier to suddenly start oscillating. The conditions of instability can be studied using Bode plots shown in Figure 4.22.

Stability study using Bode Plots

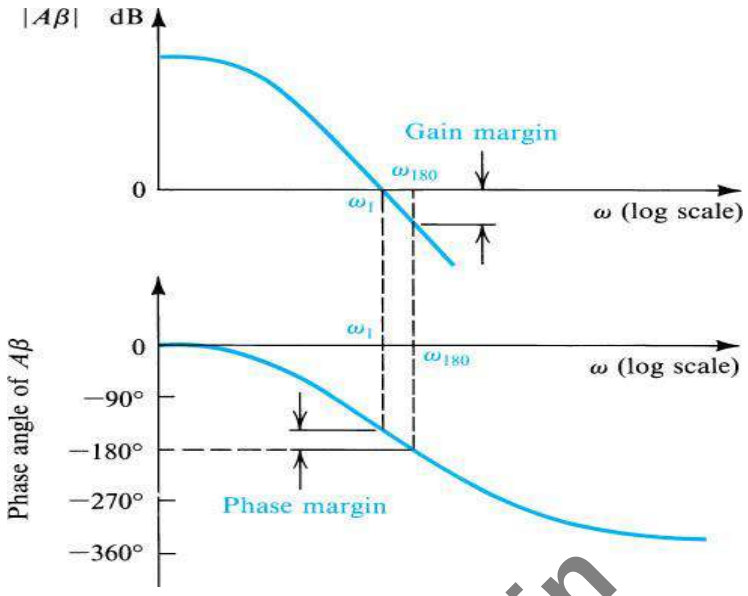

Figure 4.22 Stability study using Bode plots

Here loop gain Aβ is plotted as a function of frequency for one example of closed loop transfer function. If loop gain of unity and phase shift of 180° occurs at same time then there is threat of instability at corresponding frequency. Gain margin represents the amount by which the loop gain can be increased while stability is maintained.Phase margin represents the amount by which the loop phase shift can be changed while stability is maintained.

Oscillators

Oscillators are the electronics circuits which generate voltages of desired frequency amplitude and shape. Oscillators can be classified based

- Based on output waveform

  Example: Sinusoidal, Square wave or saw-tooth etc

- Based on circuit components

  Example: RC Oscillator, LC Oscillator and Crystal Oscillator etc

- Based on range of frequency

  Example: Audio frequency Oscillator, Radio Frequency Oscillator etc

- Based on presence of feedback

  Oscillators with feedback circuit and without feedback.

Barkhausen criterion

Any oscillator comprises of two stages:

- The Amplilfier stage
- A feedback network

For any oscillator to generate and sustain oscillations Barkhausen criteria needs to be satisfied. Barkhausen criterion states that to sustain oscillations,

- The total phase shift around the loop should be 360° or 0°.
- The product of open loop gain of the amplifier and the feedback network should be unity.

Oscillations start with a noise voltage and are sustained at a frequency at which Barkhausen criteria is satisfied.

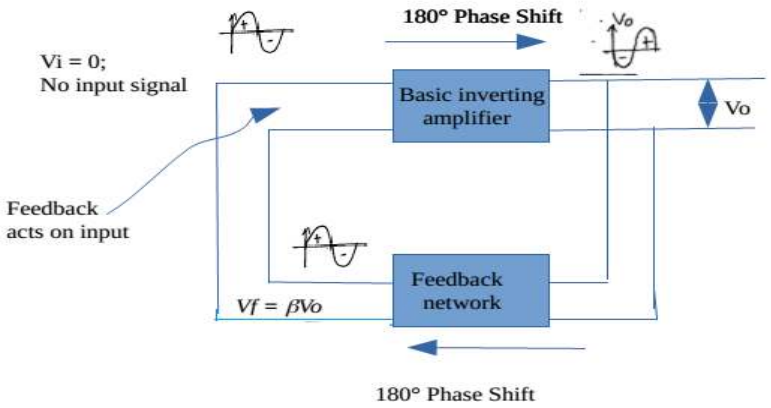

Figure 4.23 Barkhausen Criteria

As shown in the figure 4.23, The output of inverting amplifier is given by

$$V_o = AV_i \text{ .....(32)}$$

The feedback network decides the amount of feedback to be given to the input i.e.,

$$V_f = \beta V_o \text{.....(33)}$$

From equation (32) we can write equation (33) as,

$$V_f = \beta A V_i \text{ ..... (34)}$$

LOOP GAIN Aβ

Depending on the value of loop gain Aβ, the circuit generates oscillations as shown below.

If | Aβ | >1 circuit generates oscillations of growing type as shown in Figure 4.27

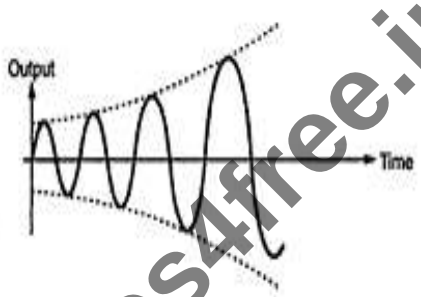

Figure 4.27 | Aβ | >1

If | Aβ | =1 the circuit generates oscillations of fixed amplitude as shown in Figure 4.28

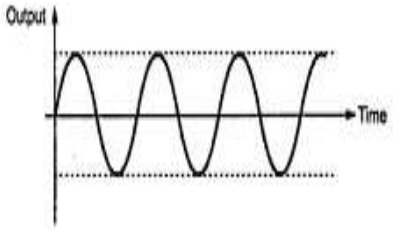

Figure 4.28 | Aβ | =1

If | Aβ | < 1 the circuit generates oscillations of decaying nature as shown in Figure 4.29

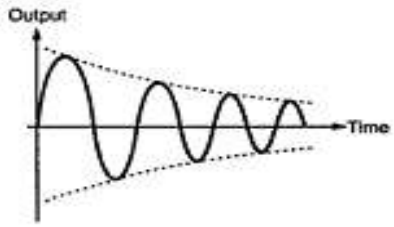

Figure 4.29 |Aβ | >1

Types of Oscillator Circuits

- FET Phase shift oscillator
- Wein bridge oscillator
- Tuned Oscillator circuit
- Crystal oscillator
- UJT Oscillator.

Phase-Shift Oscillator

Phase shift oscillator consists of an amplifier and Phase shift network constituted by RC elements as shown in Figure 4.30.

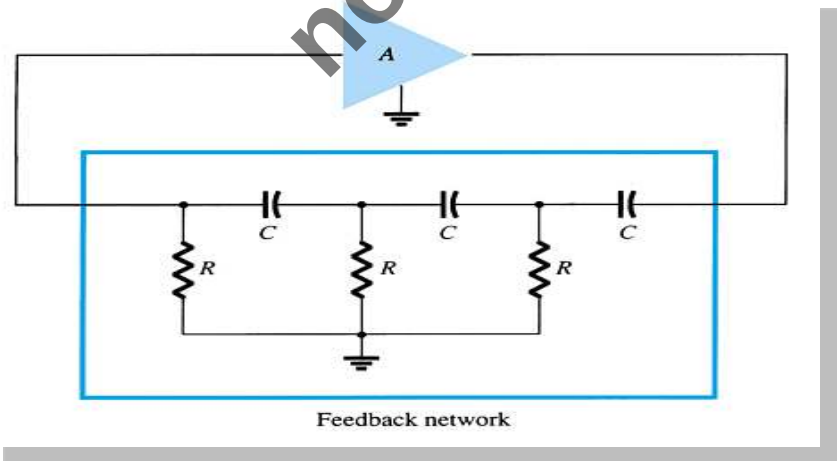

Figure 4.30 Phase shift oscillator feedback network

In phase shift oscillator,

- The amplifier and a feedback network consisting of RC Sections are present
- The RC networks provide the necessary phase shift for a positive feedback.
- The values of the RC components determine the frequency of oscillation:

Frequency of generated oscillations is given by,

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

FET Phase Shift Oscillator

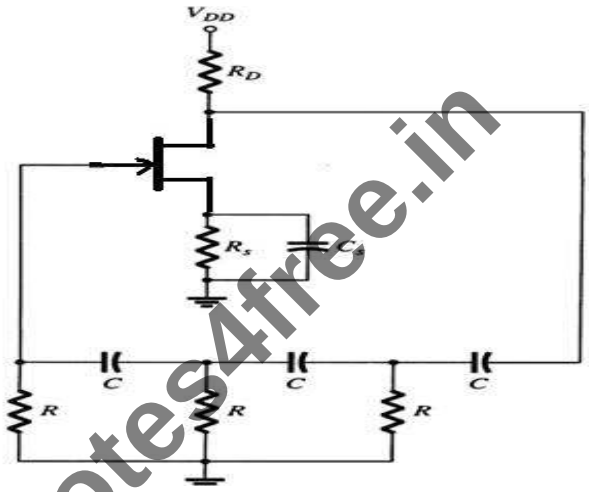

Figure 4.31 FET phase shift oscillator

A practical version of a phase-shift oscillator circuit is shown in Figure 4.31. The circuit is drawn to show clearly the amplifier and feedback network. Here FET amplifier introduces 180° phase shift. The 3 RC sections further introduce 180° phase shift. Total phase shift around the loop is 360° ensuring Positive feedback. The amplifier stage is self biased with a capacitor bypassed source resistor R_S and a drain bias resistor R_D . The FET device parameters of interest are g_m and r_d . From FET amplifier theory, the amplifier gain magnitude is calculated from

$$|A| = g_m R_L \quad \text{------- (35)}$$

where R_L in this case is the parallel resistance of R_D and r_d ,

$$R_L = \frac{R_D r_d}{R_D + r_d} \quad \text{------ (36)}$$

Let us assume that the input impedance of the FET to be infinity. This assumption is valid as long as the oscillator operating frequency is low enough so that FET capacitive

impedances can be neglected. The output impedance of the amplifier stage given by R_L should also be small compared to the impedance seen looking into the feedback network so that no attenuation due to loading occurs.

$$f = \frac{1}{2\pi\sqrt{6}RC} \quad \text{.....(37)}$$

Wien-Bridge Oscillator

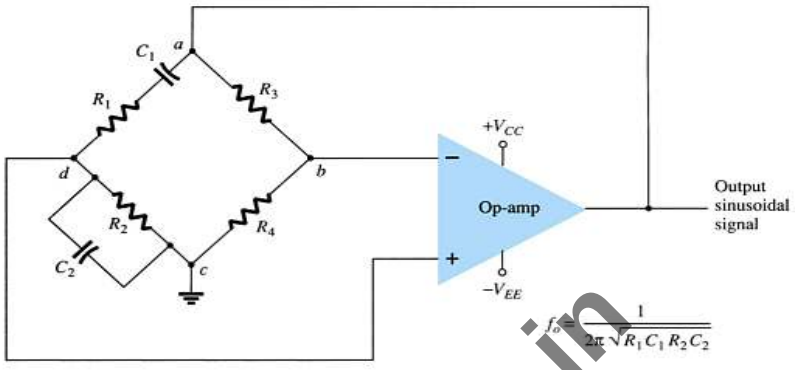

Figure 4.32 Wein Bridge oscillator

Wien-Bridge Oscillator circuit uses an op-amp and RC bridge circuit, with the oscillator frequency set by the R and C components of bridge. Note that in basic bridge connection. Resistors R_4 and R_2 and capacitors C_4 and C_2 form the frequency-adjustment elements, and resistors R_3 and R_4 form part of the feedback path. The op-amp output is connected as the bridge input at points a and c. The bridge circuit output at points b and d is the input to the op-amp.

Neglecting loading effects of the op-amp input and output impedances, the analysis of the bridge circuit results in

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \quad \text{----------(38)}$$

and,

$$f_o = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} \quad \text{---------- (39)}$$

If, in particular, the values are $R_4 = R_2 = R$ and $C_4 = C_2 = C$, the resulting oscillator frequency is

$$f_o = \frac{1}{2\prod RC} \quad \text{----------(40)}$$

and also,

R3/R4=2 ---------- (41)

Thus a ratio of R3 to R4 greater than 2 will provide sufficient loop gain for the circuit to Oscillate at the frequency calculated using eqn. (40)

RC Phase shift Oscillator

1. Circuit is simple to design.
2. Can produce output over audio frequency range.
3. Produces sinusoidal waveform.
4. It is a fixed frequency oscillator. Cannot achieve a variable frequency.
5. Frequency stability is poor due to temperature, aging etc...

Tuned Oscillator Circuits

- Tuned oscillators use a parallel LC resonant circuit (LC tank) to provide the oscillations. Frequency range from KHZ to several GHz.
- Frequency of generated oscillations is given by,

$$f = \frac{1}{2\pi\sqrt{LC}} \text{.....(41)}$$

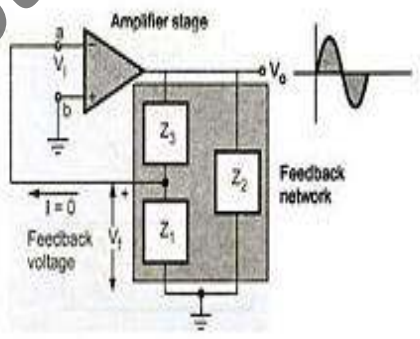

Figure 4.33 Basic form of LC oscillations

Basic form of LC oscillator circuit consists of an Amplifier and a feedback network consisting of LC resonant circuit. In the feedback network, either L or C is broken down into two impedances Z1 and Z3. Depending on the arrangement we have two types of tuned oscillator circuits.

Colpitts Oscillator— The feedback network consists of two inductive and one capacitive impedances.

Hartley Oscillator— The feedback network consists of two inductive and one capacitive impedances**.**

Colpitts Oscillator Circuit

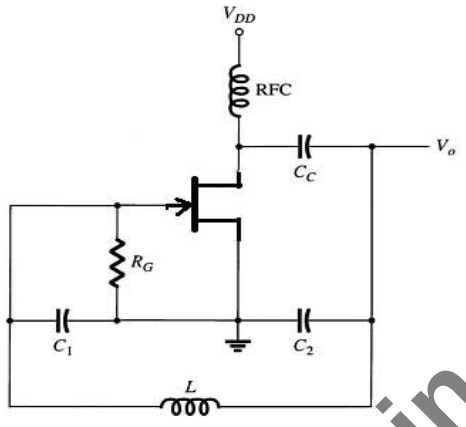

Figure 4.34 Colpitts oscillator

A practical version of an FET Colpitts oscillator is shown in Figure 4.34. The circuit is basically the same form as shown in resonant oscillator circuit with the addition of the components needed for dc bias of the FET amplifier. Here FET amplifier introduces 180^o phase shift. The LC feedback network further introduces 180^o phase shift. Thus, Total phase shift around the loop is 360^o ensuring Positive feedback.

The oscillator frequency can be found to be

$$f_o = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad .....(42)$$

$$\text{where, } C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

Hartley Oscillator:

A practical version of an Hartley oscillator is shown in Figure 4.35. The circuit is basically the same form as shown in resonant oscillator circuit with the addition of the components needed for dc bias of the BJT amplifier. Here BJT amplifier introduces 180^o phase shift. The LC feedback network further introduces 180^o phase shift. Thus, Total phase shift around the loop is 360^o ensuring Positive feedback.

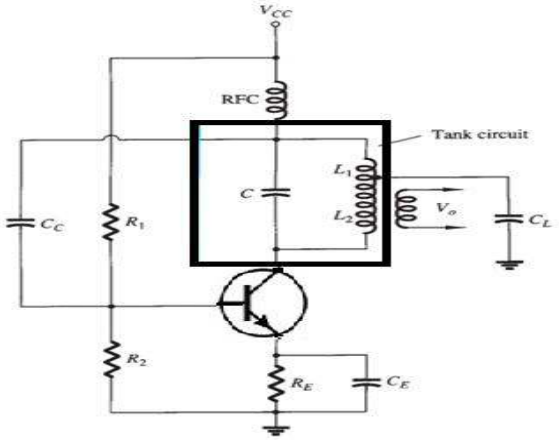

Figure 4.35 Transistorized Hartley Oscillator

The oscillator frequency can be found to be

$$f_o = \frac{1}{2\pi\sqrt{L_{eq}C}} \quad \text{----------(43)}$$

where,

$$L_{eq} = L_1 + L_2 + 2M \quad \text{----------(44)}$$

To sustain oscillations the desired value of hfe is given by,

$$hfe = \frac{L1 + M}{L2 + M} \quad \text{----------(45)}$$

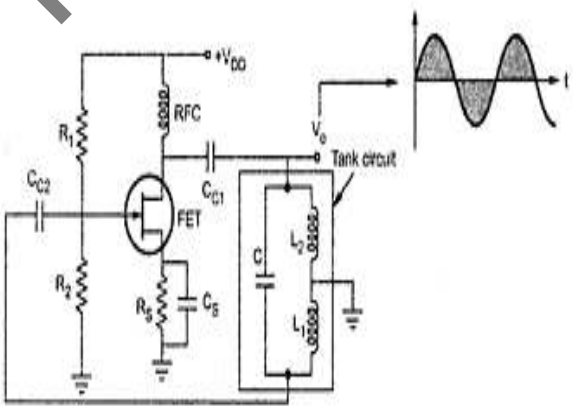

Figure 4.36 FET Hartley Oscillator Circuit

An FET Hartley oscillator circuit is shown in Fig.4.36. The circuit is drawn so that the feedback network conforms to the form shown in the basic resonant circuit. Note, however, that inductors L4 and L2 have a mutual coupling M, which must be taken into account in determining the equivalent inductance for the resonant tank circuit. Here FET

amplifier introduces 180° phase shift. The LC feedback network further introduces 180° phase shift. Thus, Total phase shift around the loop is 360° ensuring Positive feedback. The frequency of oscillations is then given by equation (43) and (44).

Frequency stability of LC oscillator

1. Due to change in temperature values of L and C in tank circuit changes. This affects frequency of oscillator.
2. Due to change in temperature transistor parameters are also affected.
3. Variation in power supply affect the frequency of oscillator.
4. Aging of circuitry also affects the frequency of oscillation.
5. Change in Q_L affects the internal resistance of tank circuit. This affects frequency of oscillations.
6. The internal capacitance of transistor also affects the frequency of oscillations.

Crystal Oscillators

The Quartz, Tourmaline and Rochelle salt exhibit piezo-electric effect. This means under the influeence of mechanical stress, The voltage gets generated across opposite faces of crystal. Conversely, if electric potential is applied across the crystal, it vibrates causing mechanical distortion in the crystal sheet. This mechanical vibration generates electrical signalat constant frequency. Crystal has greater stability in holding its frequency. Out of Quartz, Tourmaline and Rochelle salt, Rochelle salt exhibits high piezo-electric activity and Rochelle salt are mechanically weakest. They break easily. Tourmaline is the strongest of three but is very expensive. Quartz crystal is the compromise between the two, it is naturally available in abundant quantity and exhibits reasonably good piezo-electric activity. Quartz crystals are used in all ratio frequency oscillators and filters.

AC Equivalent Circuit:

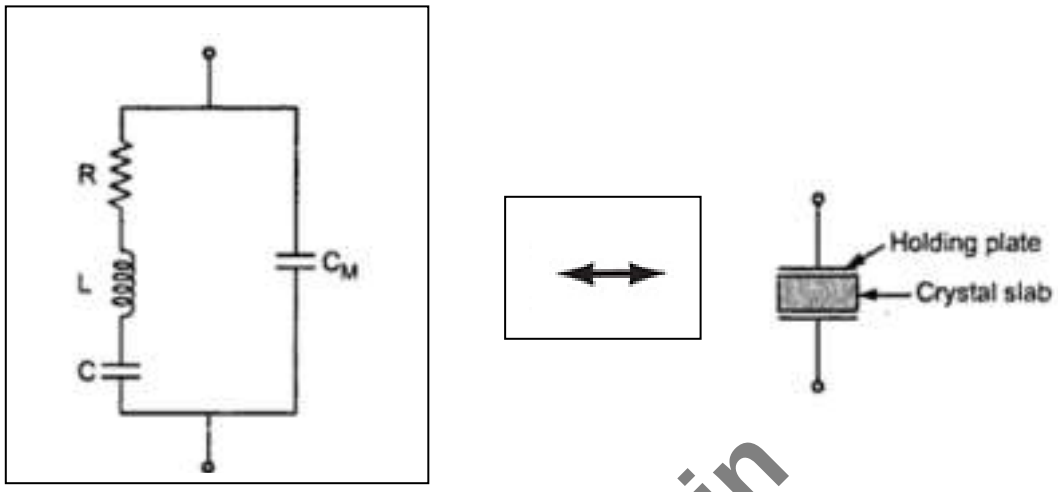

Fig. 4.37 AC equivalent circuit of Crystal Oscillator

For the practical views, Crystal is cut as a rectangular slab and is held between two mechanical plates.When the crystal is not vibrating it is equivalent to parallel plate capacitor, i.e., a dielectric medium (Crystal slab) present between two metallic plates of the capacitor. This is represented as capacitane C_M .

When the crystal is vibrating there are internal frictional loss which is denoted by resistance "R". The mass of crystal corresponds to its inertia represented by "L". The stiffness of crystal is denoted by "C". This forms a series RLC circuit and corresponding series resonant frequency is

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad \text{.....(46)}$$

Actually frequency of generated oscillations is inversely proportional to thickness. There exists a parallel resonant circuit also. This is formed due to the presence of inductor L and capacitance Ceq. At parallel resonant frequency, impedance is maximum. It is given by,

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad \text{.....(47)}$$

where,

$$C_{eq} = \frac{C_M C}{C_M + C}$$

Actually fr and fp are very close to each other. The graph of impedance vs Frequency is as shown in Figure 4.38.

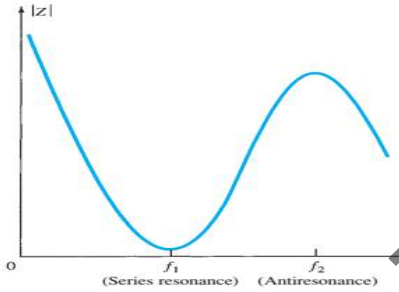

Figure. 4.38 Impedance of a crystal oscillator

Crystals can be used in both series and parallel resonant mode to generate oscillations.

Series Resonant Crystal Oscillator using BJT

Here Crystal is connected in feedback path of the amplifier. The voltage feedback from collector to base is a maximum when the crystal impedance is minimum (in series-resonant mode). The resulting circuit frequency of oscillation is set by the series-resonant frequency of the crystal. The resistance R_1, R_2 and RE provide DC bias while Capacitor C_E is emitter bypass capacitor. RFC coil provides for dc bias while decoupling any ac signal on the power lines from affecting the output signal. The resonant frequency is given equation (46). The crystal oscillator provides good frequency stability i.e., the oscillating frequency is not affected by supply variations, temperature and transistor parameters.

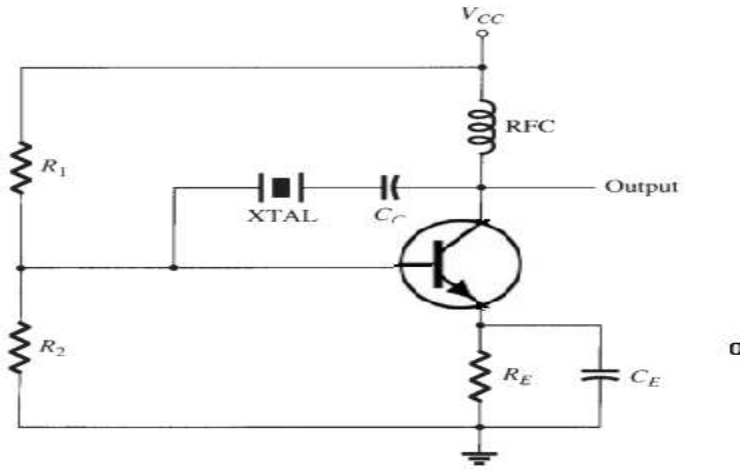

Figure 4.39 Series Resonant Crystal Oscillator using BJT

Series Resonant Crystal Oscillator using FET

Here Crystal is connected in feedback path of the FET amplifier. The voltage feedback from Drain to Gate is a maximum when the crystal impedance is minimum (in series-resonant mode). The resulting circuit frequency of oscillation is set by the series-resonant frequency of the crystal. RFC coil provides for dc bias while decoupling any ac signal on the power lines from affecting the output signal. Changes in supply voltage, transistor device parameters, and so on, have no effect on the circuit operating frequency. The resulting circuit frequency of oscillations is set by the series-resonant frequency of the crystal. The resonant frequency is given equation (46).

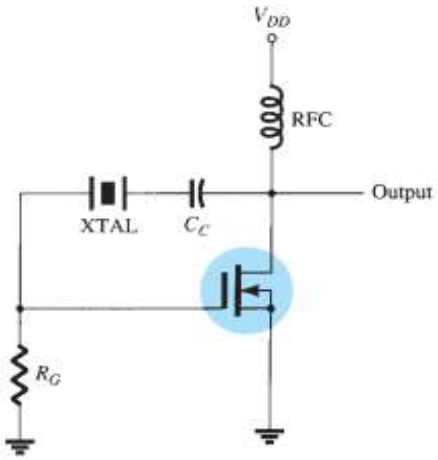

Fig 4.40 Series Resonant Crystal Oscillator using FET

Parallel Resonant Crystal Oscillators

Crystal is connected as a inductor in the modified Colpitts oscillator circuit. At the parallel-resonant operating frequency, a crystal appears as an inductive reactance of large value. The resulting circuit frequency of oscillation is set by the parallel-resonant frequency of the crystal. The resistance R_1, R_2 and RE provide DC bias while Capacitor C_E is emitter bypass capacitor. RFC coil provides for dc bias while decoupling any ac signal on the power lines from affecting the output signal. The resonant frequency is given equation (47).

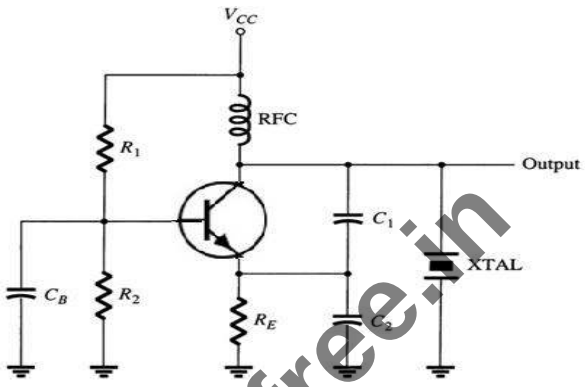

Figure. 4.44 Parallel Resonant Crystal Oscillator

Miller's Crystal Oscillator

The Hartley oscillator can be modified using crystal at one of the inductors of the tank circuit. The crystal behaves as inductor "L" connected to base and ground. The internal capacitance of transistor acts as capacitors C_1 and C_2 of the tank circuit. The crystal decides operating frequency of oscillator. A tuned LC circuit in the drain section is adjusted to the crystal parallel-resonant frequency. The resonant frequency is given equation (47).

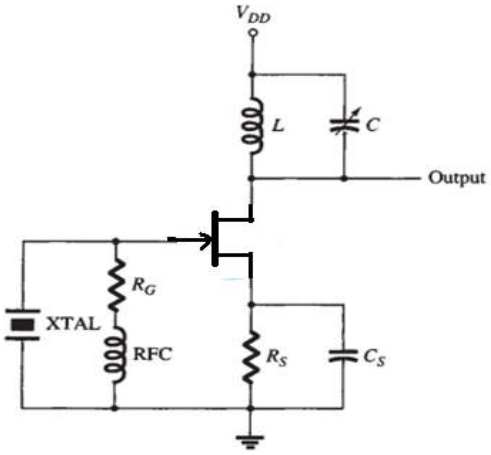

Fig. 4.45 Millers Crystal Oscillator

Unijunction Transistor

The Unijunction Transistor (UJT) has three terminals: an emitter (E) and two bases (B_1 and B_2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B_1 and B_2 are attached at its ends. The emitter is of p-type and it is heavily doped; this single PN junction gives the device its name. The resistance between B1 and B2 when the emitter is open-circuit is called inter-base resistance. The emitter junction is usually located closer to base-2(B2) than base-1(B1) so that the device is not symmetrical, because symmetrical unit does not provide optimum electrical characteristics for most of the applications (Refer Figure 4.46).

The schematic diagram symbol for a unijunction transistor represents the emitter lead with an arrow, showing the direction of conventional current flow when the emitter-base junction is conducting a current. A complementary UJT would use a p-type base and an n-type emitter, and operates the same as the n-type base device but with all voltage polarities reversed.

The structure of a UJT is similar to that of an N-channel JFET, but p-type (gate) material surrounds the N-type (channel) material in a JFET, and the gate surface is larger than the emitter junction of UJT. A UJT is operated with emitter junction forward- biased while the JFET is normally operated with the gate junction reverse-biased. It is a current controlled negative resistance device.

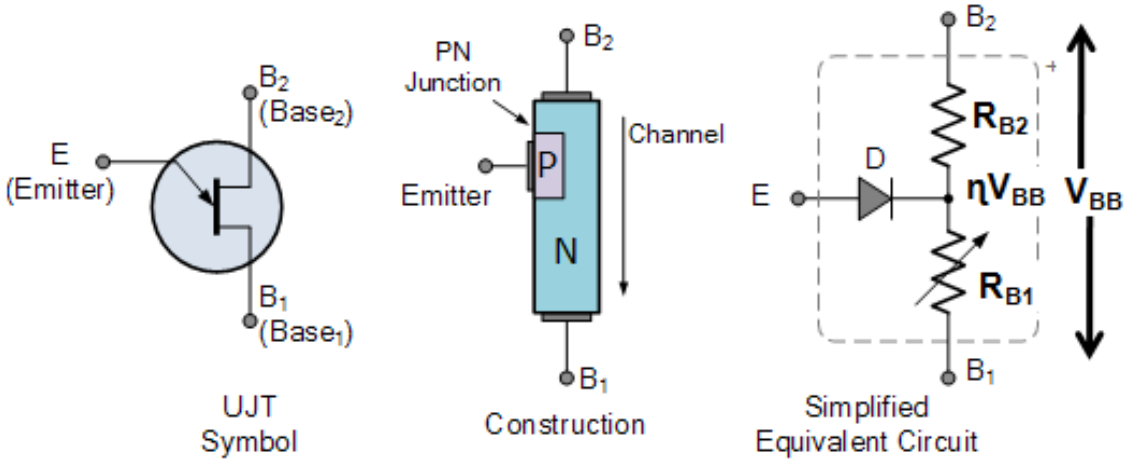

Figure 4.46 UJT Transistor

The device has a unique characteristic that when it is triggered, its emitter current increases regenerativaly until it is restricted by emitter power supply. It exhibits a negative resistance characteristic and so it can be employed as an oscillator.UJT has a instrinsic stand-off ratio denoted by,

$$\eta = \frac{R_{B1}}{(R_{B1} + R_{B2})} \quad \text{.....(48)}$$

Where,η is termed as intrinsic standoff ratio with values between 0.4 to 0.6

The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes conductivity modulation which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits.

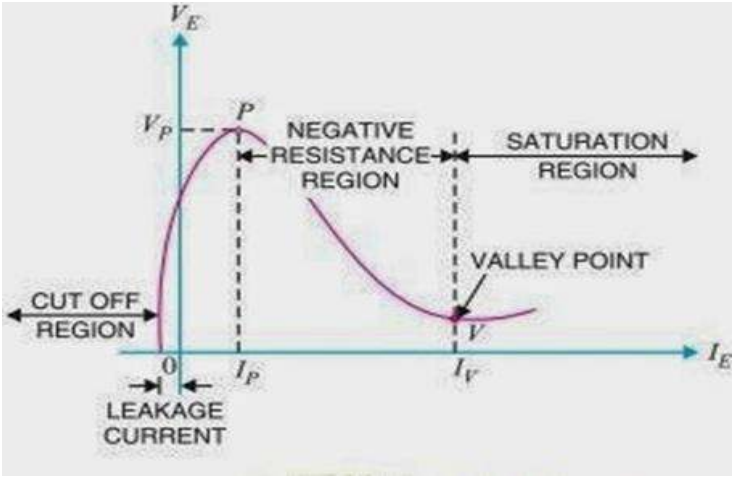

Figure 4.47 UJT Characteristics

Unijunction as a Relaxation Oscillator

The unijunction transistor can be as a relaxation oscillator as shown by the basic circuit in Figure 4.48. Resistor R_T and capacitor C_T are the timing components that set the circuit oscillating rate. The oscillating frequency may be calculated using Equation (44) shown below. Which includes the unijunction transistor intrinsic stand-off ratio η as a factor (in addition to R_T and C_T) in the oscillator operating frequency.

$$f_o = \frac{1}{T} = \frac{1}{R_3 C_1 \ln[1/(1-\eta)]} \quad \text{.....(49)}$$

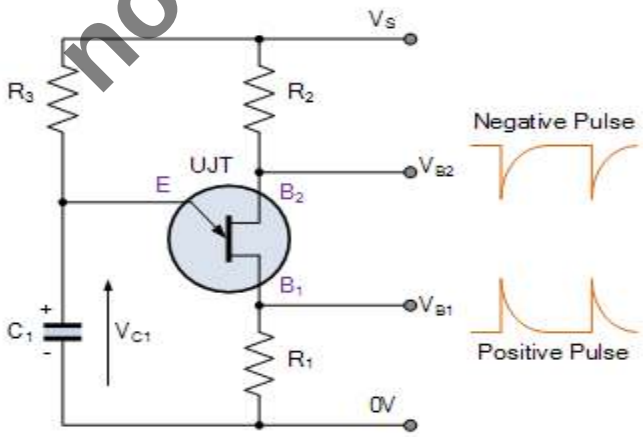

Figure 4.48 UJT as a Relaxation Oscillator

Capacitor C1 is charged through resistor R3 toward supply voltage Vs . As long as the capacitor voltage V_E is below a stand-off voltage (V_P) the unijunction emitter lead appears as an open circuit. When the emitter voltage across capacitor C1 exceeds this value V_P , the unijunction transistor conducts discharging into the capacitor. The signal at

the emitter is a sawtooth voltage waveform which represents capacitor charging and discharging action. Base 2 is a signal representing sudden discharge of capacitor voltage.

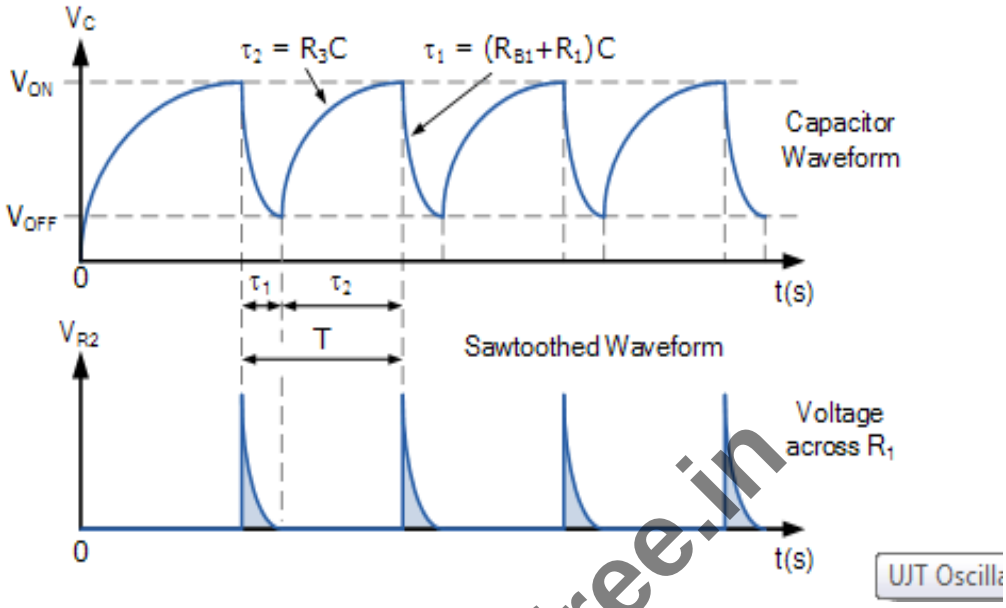

Figure 4.50 Waveforms of UJT as a Relaxation Oscillator

Module 5: Power Amplifiers and Voltage Regulators

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Syllabus:

Power Amplifiers: Definition and amplifier types, Series fed class A amplifier, Transformer coupled class A amplifier, Class B amplifier operation and circuits, Amplifier distortion, Class C and Class D amplifiers. Voltage regulators: Discrete transistor voltage regulation - Series and Shunt Voltage regulators.

Courtesy:

Robert L. Boylestad and Louis Nashelsky, "Electronics Devices and Circuit Theory", Pearson, 10th Edition, 2012, ISBN: 978-81-317-6459-6.

Adel S. Sedra and Kenneth C. Smith, "Micro Electronic Circuits Theory and Applications," Oxford University Press, 5th Edition, ISBN:0198062257.

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5.1 Introduction

When the power requirement to drive the load is in terms of several Watts rather than mili-watts the power amplifiers are used. Power amplifiers form the last stage of multistage amplifiers. If we consider the example of Public address systems where, microphone output or a CD player output is to be driven across loudspeakers then these signals undergo series of small signal amplifiers. The output of small signal amplifiers intern acts as input to Power amplifiers. The output of Power amplifier drives the loudspeaker.

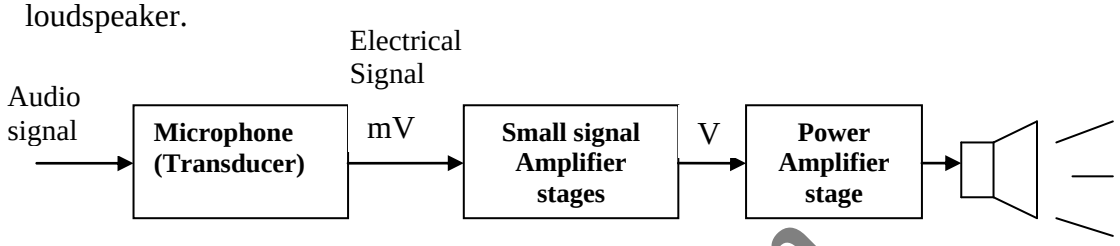


Figure 5.1 Public Address Systems

The power amplifier makes use of power transistors for signal amplification. Power amplifiers are classified depending upon the operating point (Q point) of operation and nature of output waveforms they produce. Basically, amplifier classes represent the amount the output signal variation over one cycle of operation for a full cycle of input signal. Power amplifiers are classified as CLASS A, CLASS B, CLASS AB, CLASS C and CLASS D Power amplifiers.

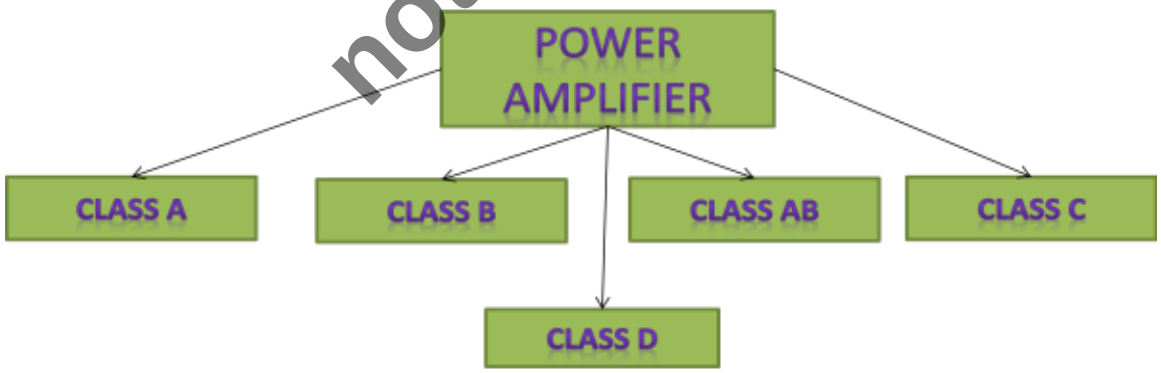


Figure 5.2 Classification of power amplifiers

5.2 Classification of Power Amplifiers:

5.2.1 CLASS A Power Amplifier

Here the Q pt & input signal are selected such that the output signal is entire 360^{o} amplified version of the input. This power amplifier is widely used for amplification of audio signals. Here Q pt is selected such that both Positive & Negative half cycle of the

ac input are amplified. The efficiency of class A Power amplifies is between 25% to 50%.

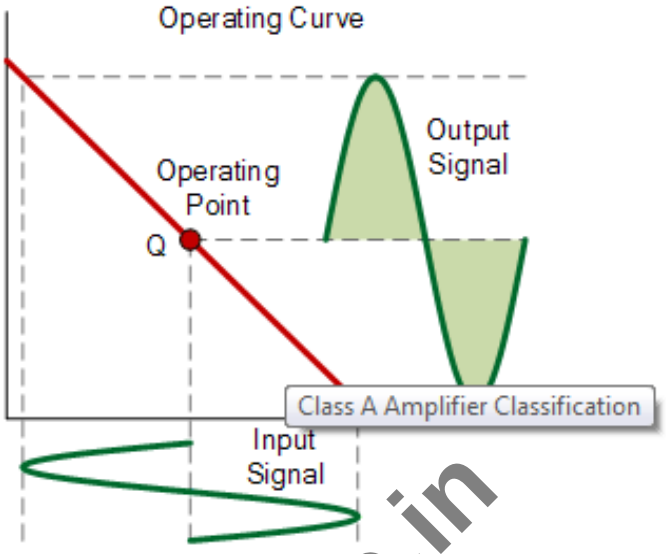


Figure 5.3 CLASS A Power Amplifier

5.2.2 CLASS B Power Amplifier

Here Q pt & input signal are selected that output signal is obtained for only one half of input signal. Usually class B operation is very much necessary for large signal amplification. Here Q pt is set at the x-axis. To have full cycle output, two class B operations—one to provide output on the positive output half-cycle and another to provide operation on the negative-output half-cycle are necessary. The combined half-cycles then provide an output for a full 360° of operation. This type of connection is referred to as push-pull operation, which is discussed later in this section. Efficiency of class B power amplifiers is more than 75%.

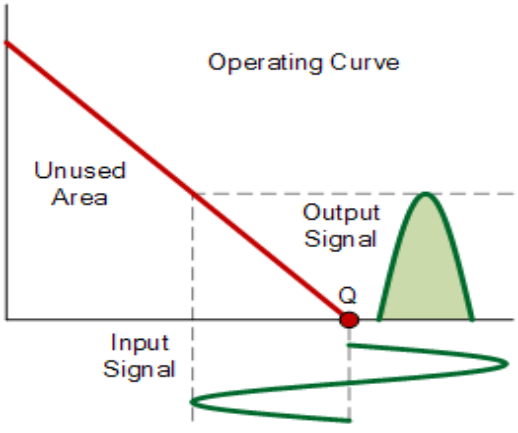


Figure 5.4 Class B Operation

5.2.3 CLASS AB Power Amplifier

Here Q pt & input signal are selected such that output signal is obtained for more than 180^{o} but less than 360^{o}. The 'Q' pt of class AB amplifiers is above the x-axis but below the midpoint of operation. Efficiency of class AB power amplifiers is more than class A & less than class B.

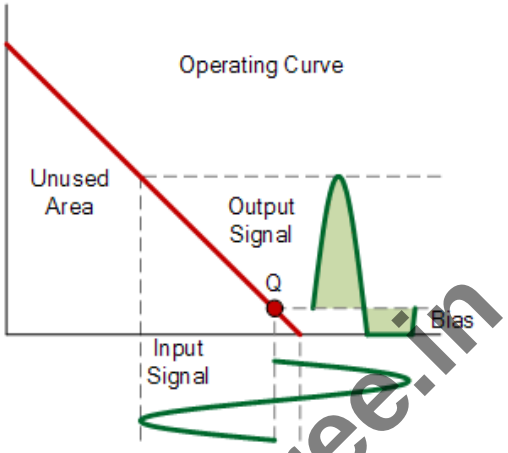


Figure 5.5 Class AB Operation

5.2.4 CLASS C Power amplifiers

Here 'Q' pt & input signal are selected such that output signal is present for less than 180o of input cycle. Class C power amplifies are not suitable for audio frequency amplification. These are useful in tuned circuits of all communication transmitters & receivers.

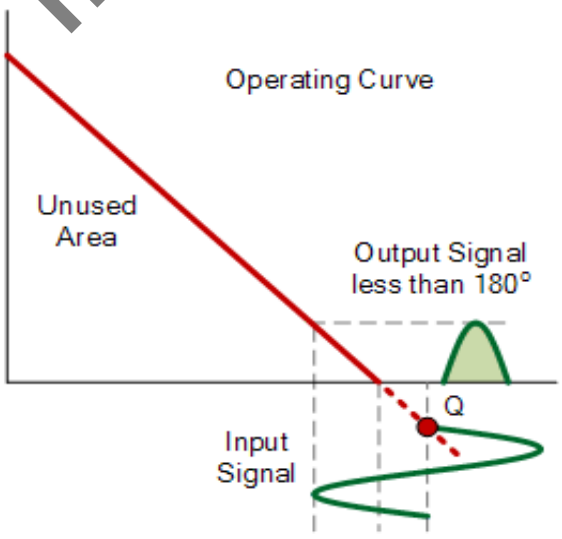


Figure 5.6 Class C operation

5.2.5 CLASS D power amplifiers

The class D amplifiers make use of digital signals to provide power amplification. The major advantage of class D operation is that the amplifier is on (using power) only for short intervals and the overall efficiency can practically be very high, as described in the next sections.

5.3CLASS A Power amplifiers

Class A power amplifiers can be classified as Directly coupled CLASS A power amplifiers & transformer coupled CLASS A power amplifiers

5.3.1 Directly coupled class A power amplifiers

The Figure 5.7 shows directly coupled class A amplifier. Where load resistance Rc to be driven is present at collector of the transistor amplifier. The Common Emitter Amplifier Circuitry is modified to act as class A power amplifier.

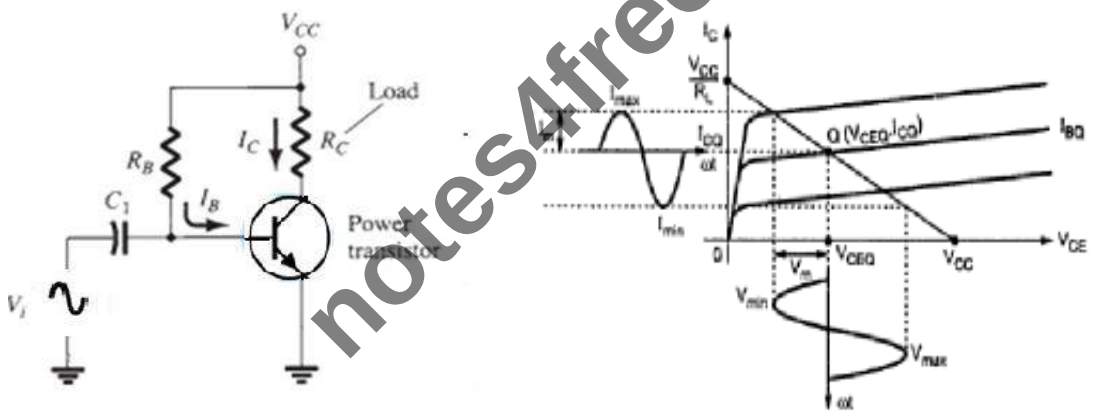


Figure 5.7 Directly coupled Class A Power Amplifiers Figure 5.8 Output Characteristics

The design equations are shown as below:

V_{CC}-$I_B R_B$-V_{BE}=0

$I_B = \frac{Vcc - V_{BE}}{R_B}$ ---------- (1)

$I_{CQ} = \beta I_B$ ---------- (2)

V_{CC}-$I_C R_C$ -V_{CE}=0

$V_{CEQ} = Vcc - I_C R_C$---------- (3)

Derivation of Efficiency of Class A Power Amplifier

Output Power:

The ac power delivered to the load can be expressed in a number of ways. The ac power delivered to the load R_L may be expressed using rms signals as

$Pac = V_c I_c = I_c^2 R_L$ ---------- (4)

Where V_c & I_c are the rms values of the output voltage

$$I_c = \frac{I_m}{\sqrt{2}} = \frac{I_{max} - I_{min}}{2\sqrt{2}} \quad \text{---------- (5)}$$

$$V_c = \frac{V_m}{\sqrt{2}} = \frac{V_{max} - V_{min}}{2\sqrt{2}} \quad \text{---------- (6)}$$

$$Pac = VcIc = \frac{V_m I_m}{2} = \frac{I_m^2 R_L}{2} = \frac{V_m^2}{2R_L} \quad \text{---------- (7)}$$

Input Power:

The power to an amplifier is provided by the DC supply. With no input signal, the dc current drawn is the collector bias current, I_{CQ}. Therefore power then drawn from the supply is

$DC\ power\ P_{dc} = V_{CC}\ I_{CQ}$ ---------- (8)

Efficiency can be expressed as,

η=Output Power/Input Power

= Pac/Pdc

$$\eta = \frac{P_{ac}}{P_{dc}} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \quad \text{---------- (9)}$$

To derive maximum efficiency, it is assumed that Class A is operating at its Full efficiency, the voltage and current waveforms are as shown in figure 5.9.

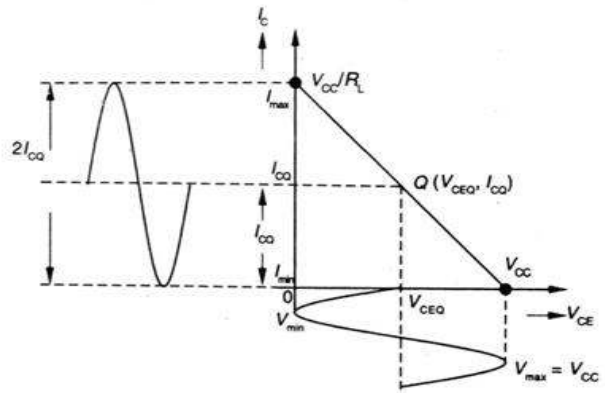


Figure 5.9 Output characteristics at maximum efficiency

We can observe from the above diagram that,
For maximum efficiency,

$$V_{max} = V_{CC} \ \& V_{min} = 0 \quad \text{---------- (10)}$$

$$I_{max} = 2I_{CQ} \ \& I_{min} = 0 \quad \text{---------- (11)}$$

Therefore, maximum efficiency,

$$\eta_{max} = \frac{V_{CC}\, 2I_{CQ}}{8V_{CC}\, I_{CQ}} = 25\% \quad \text{---------- (12)}$$

Advantages of directly coupled class A amplifier,

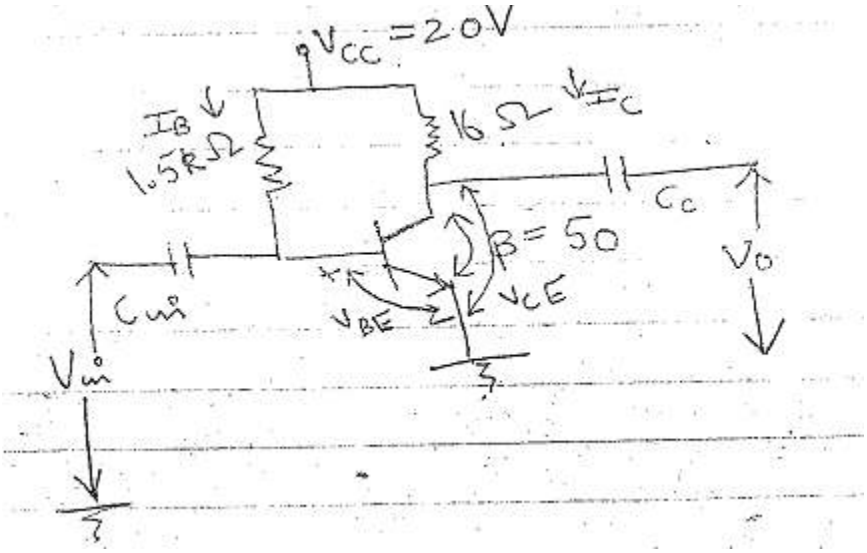
1. Circuit is simple to design.
2. Used as audio signal amplifier.
3. Less costly.

Disadvantages:

1. Efficiency is less
2. Transistor's output impedance is large.
3. Typical load impedance is very low (loud speakers having resistances only from 5-16Ω) **therefore, Impedance mismatch exists and maximum power transfer cannot be achieved. Efficiency is limited to 25%.**

Problems

1) A class A power amplifier operates from a DC source and applied sinusoidal signal generates a peak 9mA. Calculate I_{CQ}, V_{CEQ}, P_{DC}, P_{AC}, η
Assume β=50, V_{BE} =0.7V. It is given that applied signal generates peak base current of 9mA .



To calculate DC Power,

Applying KVL to BE loop we get,

V_{CC}-I_BR_B-V_{BE}=0

$I_B = \frac{Vcc-V_{BE}}{R_B}$ =12.87mA

$I_{CQ} = \beta I_B$=643.5mA

KVL to CE loop,
V_{CC}-I_CR_C -V_{CE}=0
$V_{CEQ}= Vcc - I_CR_C$ =9.704V

Therefore, DC input power, $P_{DC}=V_CI_{CQ}$

P_{DC}=12.87W

AC output power= $I^2_{RMS}.R_L$
$=i^2_{CRMS}.R_C$
It is given that,
i_{bm}= 9mA.
$i_{cm}=\beta i_{bm}$
i_{cm}=45mA
$i^2_{CRMS}=\frac{450mA}{\sqrt{2}} = 0.318A$

$P_{AC}=(0.318)^2X16=1.618W$

$\eta=\frac{P_{AC}}{P_{DC}}X100\% = \frac{1.618}{12.87} = 12.57\%$

5.3.2 Transformer Coupled Class A Power Amplifier

Disadvantages associated with directly coupled class A amplifier can be over-come by my making use of transformer at the output. In case of directly coupled class A amplifier output impedance of amplifier is large. The typical loads such as loudspeaker have very low input impedance 5 to 16Ω, due to this impedance mismatching maximum power transmission to the load cannot be achieved. If transformer is used as a impedance matching device then maximum power transfer to the load and efficiency of up to 50% can be achieved.

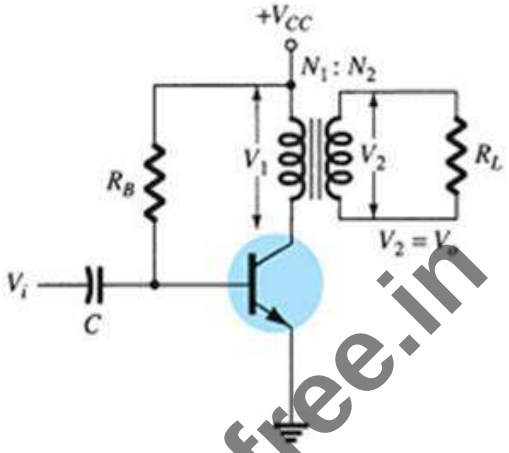


Figure 5.10 Transformer coupled class A Power amplifier

Impedance transformation property of the transformer

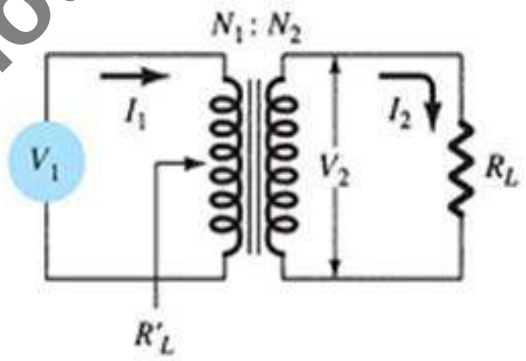


Figure: 5.11 Transformer windings

We know that Turns ratio, $\eta=\frac{V_2}{V_1}=\frac{N_2}{N_1}$ $-----------(13)$

Also, $\frac{N_2}{N_1}=\frac{I_1}{I_2}$ $-----------(14)$

At secondary, load resistance can be expressed as, $R_L=\frac{V_2}{I_2}$ $----(15)$

Reflected impedance at the 1^o side of the transformer can be expressed as

$$R^I_L = \frac{V_1}{I_1}$$

$$= \frac{\left(\frac{N1}{N2}\right)V2}{\left(\frac{N2}{N1}\right)I2} = \left(\frac{N1}{N2}\right)^2 R_L$$

$$R^I_L = \left(\frac{1}{n^2}\right)R_L \quad ----------(16)$$

It can be seen that impedance at the 2^o gets reflected at the 1^o by the square of turn's ratio. This makes impedance matching possible.

DC operation: Applying KVL to CE loop, we get In an ideal transformer, there is no primary drop. Thus the supply voltage appears as the collector-emitter voltage of the transistor. Winding offers no resistance.

$$V_{CC} = V_{CE} \quad .....(17)$$

When the values of the resistance R_B and V_{CC} are known, the base current at the operating point may be calculated by the equation,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \approx \frac{V_{CC}}{R_B} \quad .....(18)$$

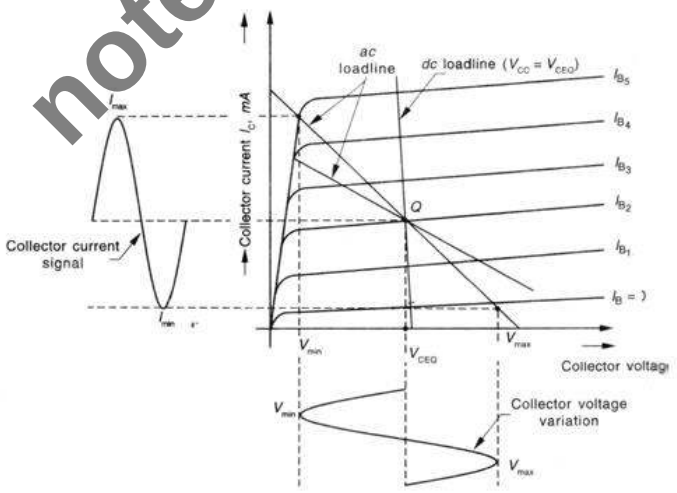


Figure 5.12 Output Characteristics of transformer coupled Power A Power Amplifiers

Efficiency of transformer coupled Class A Power Amplifier can be expressed as,

Efficiency $\eta = \frac{\left(\frac{o}{p}\right)power}{\left(\frac{i}{p}\right)power} = \frac{P_{AC}}{P_{DC}}$ – – – – – – – – – – – – –(19)

DC Power, $P_{DC}=V_{CC}*I_{CQ}$ ---------- (20)

AC Output power can be derived as,

$$P_{AC}(primary)=I_1{}^2{}_{RMS}R^I{}_L=\frac{V_{1RMS}{}^2}{R^I{}_L}=V^2{}_{1RMS}I^1{}_{RMS}=\frac{V_{1M}}{\sqrt{2}}.\frac{I_{1M}}{\sqrt{2}}=\frac{V_{1M}I_1}{2}$$.....(21)

$P_{AC}(2^O)=I^2{}_{2RMS}.R_L=\frac{V_{2RMS}{}^2}{R_L}=V_{2RMS}I_{2RMS}$

$$=\frac{V_{2M}}{\sqrt{2}}.\frac{I_{2M}}{\sqrt{2}}=\frac{V_{2M}I_{2M}}{2}$$.....(22)

Assuming lossless Transformer,

AC power at 1^o=AC Power at 2^o

$P_{AC}(1^O)=P_{AC}(2^O)$

$P_{ACMAX}=\frac{V_{PP}I_{PP}}{8}$

$=(V_{CEMAX}-V_{CEMIN})(I_{CMAX}-I_{CMIN})/8$

$=\frac{(2V_{CC}-0)(2I_{CQ}-0)}{8}$

$=\frac{V_{CC}I_{CQ}}{2}$.....(23)

Assuming that class A amplifier is operating at its full efficiency then the waveforms of current and voltages as shown in Figure 5.13.

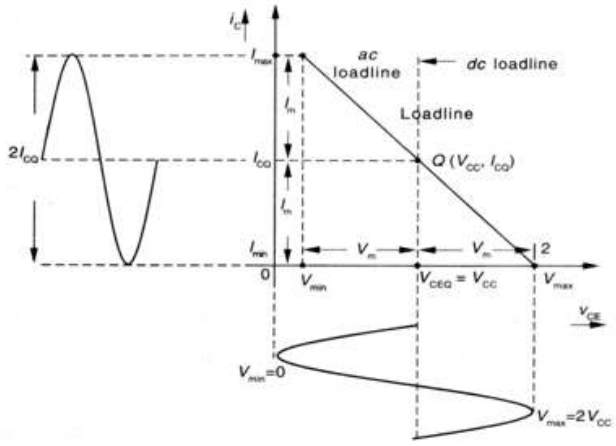


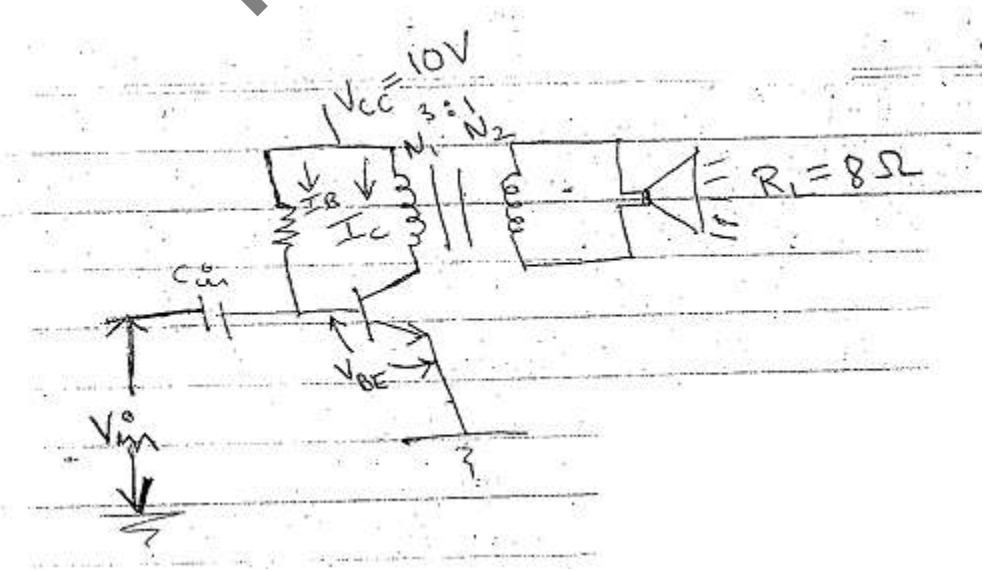
Figure 5.13 Output Characteristics of transformer coupled Power A Power Amplifiers at maximum efficiency

Maximum efficiency of class A amplifier can be expressed as

$$\eta_{max} = \frac{(2V_{CC}-0)(2I_{CQ}-0)}{8} = \frac{V_{CC}I_{CQ}}{2} \text{.....(24)}$$

$$\eta_{max} = 50\%$$

1) A transformer coupled class A amplifier has a loudspeaker of 8Ω connected across its secondary. The Q pt of collector current is 140mA. The turns ratio of the transformer is 3:1. The collector supply voltage is 10V. If the transformer is lossless, calculate power delivered to the 1^o of the transformer, rms load current, rms 1^0 current η and power dissipation. The power delivered to the load is 0.48W



Solution:
It is given that, $P_{AC}(sec)=0.48W$, $I_{CQ}=140mA$, $R_{L}=8\Omega$
N2 / N1=1/3 = V2 / V1=I1 / I2
Transformer is lossless,
Therefore, $P_{AC(1*)}=P_{AC(2*)}=0.48W$

$P_{AC}(sec)=\frac{V_{2RMS}^{2}}{R_L}$

$V_{2RMS}=1.96V$
We know that, $\frac{V_{2RMS}}{V_{1RMS}}=\frac{N_2}{N_1}$

$V_{1RMS}=\frac{1.96*3}{1}=5.88V$

$I_{2RMS}=\frac{V_{2RMS}}{R_L}=0.245A$

Output Power, $P_{DC}=V_{CC}I_{CQ}$

$=10*140*10^{-3}=1.4W$

Therefore, Efficiency, $\eta=\frac{P_{AC}}{P_{DC}}$
$=\frac{0.48}{1.4}*100\%$

=34.29%

Power dissipation

It is the amount of power that is dissipated as heat across the power amplifier.
$P_D=P_{DC}-P_{AC}$ =1.4-0.48=0.92W

In Class A power amplifier, maximum power dissipation occurs when applied AC signal is zero. $P_{dmax}=P_{DC}=V_{CC}I_{CQ}$

Drawbacks of Class A power amplifier

- Less Efficiency of 25-50%.
- Power dissipation is high, therefore less reliability.
- Directly coupled class A power amplifier cannot be employed to drive low impedance loads such as loud speaker.
- Total harmonic distortion is very high.
- The output transformer is subjected to saturation problem due to the dc current in the primary.

5.4 Class B power amplifier

In class B power amplifier, output waveform is present only for 180^o of the input cycle. This is because Q pt is biased at x-axis, therefore negative half cycle is clipped and only the Positive half cycle appears at the load. If we make use of 2 class B amplifiers, each for 180^o conduction, than full power will be applies to the load. There are 2 categories of class B amplifiers. (i) Transformer coupled Push-Pull class B Power Amplifier and

(ii) Complimentary Symmetry Class B Power Amplifier

i) Transformer coupled Push-Pull class B Power Amplifier

Push-Pull Power Amplifier: These make of two identical npn or pnp transistors whereas complementary symmetry makes use of 1 pnp and 1 npn transistors. As shown in the Figure 5.14, push pull PA makes use of two centre tapped transformers, one is called as driver transformer as it drives input to the circuitry, another is a output transformer which acts a impedance matching device and couples the power to the load. The center tapped end of the driver transformer is connected to the ground and the center tapped output transformer is connected to V_{CC}. The 2 transistors Q_1 and Q_2 should be both either pnp or npn. During positive half cycle end A becomes Positive with respect to end B, therefore Q_1 gets forward biased and Q_2 gets reverse biased. Q_1 conducts and Positive half cycle is connected to the load by making use of output transformer. During negative half cycle, end B becomes positive with respect to A. therefore Q_2 gets forward biased and Q_1 gets reverse biased. Q_2 conducts and negative half cycle is connected to the load by making use output transformer. Amplified output appears for entire 360^o of the input cycle.

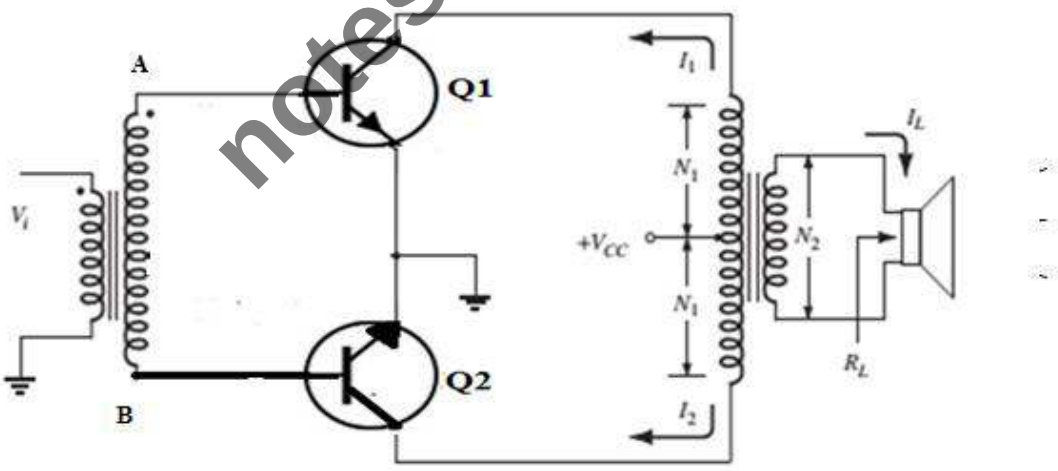


Figure 5.14 Class B Power Amplifier

Derivation of efficiency of Class B Power Amplifier

We know that Efficiency of Power Amplifier can be expressed as,

$$\eta=\frac{P_{AC}}{P_{DC}} \quad \text{.....(25)}$$

DC Operation

Applying KVL to output,
V_{CC}-V_{CE}=0
Therefore; $V_{CC}=V_{CE}$ .....(26)
DC load line is straight line as shown in the output characteristics.

Here each transistor conducts only for half cycle. Therefore it can be treated as half wave rectifier.

$P_{DC}=V_{CC}I_{DC}=V_{CC}\frac{2I_M}{\pi}=\frac{2V_{CC}I_M}{\pi}$.....(27)
Current flowing through half wave rectifier is I_{DC}, therefore overall DC current $I_{DC}=\frac{2I_M}{\pi}$
Output power, $P_{AC}(1^o)=V_{RMS}I_{RMS}$

$$=\frac{V_{1RMS}{}^2}{R_L{}^I}=I^2{}_{RMS}R_L{}^I=\frac{V_{1M}}{\sqrt{2}}\frac{I_{1M}}{\sqrt{2}}=\frac{V_{1M}I_{1M}}{2}$$

$P_{AC}(2^O)= V_{2RMS}I_{2RMS}$

$$=\frac{V^2{}_{2RMS}}{R_L}=I^2{}_{2RMS}R_L=\frac{V_{2M}I_{2M}}{2}$$

For a lossless transformer,
$P_{AC}(1^o)= P_{AC}(2^O)=\frac{V_{PP}I_{PP}}{8}==\frac{V_{PP}}{8}\left(\frac{V_{PP}}{R_L}\right)=\frac{V_{PP}{}^2}{8R_L}=\frac{(2V_M)^2}{8R_L}=\frac{V_M{}^2}{2R_L}$

Efficiency:

η=Pac/Pdc

$$\eta=\frac{(\frac{V^2{}_M}{2R_L})}{2V_{CC}I_MV_M}=\frac{\pi}{4}\frac{V_M}{V_{CC}}$$

For max efficiency:
$V_M= V_{CC}$

$$\eta_{MAX}=\frac{\pi}{4}\frac{V_{CC}}{V_{CE}}=78.55\%$$

Power dissipation of class B power amplifier

We know that Power dissipation, $P_D=P_{DC}-P_{AC}=\frac{2V_{CC}I_M}{\pi}-\frac{V_M{}^2}{2R_L}$

$$P_D=\frac{2V_{CC}I_M}{\pi R_L}-\frac{V_M{}^2}{2R_L}-----------(28)$$

To calculate the condition for max power dissipation is $\frac{dP_D}{dV_M} = 0$

$0=\frac{2V_{CC}}{\pi R_L} - \frac{2V_M}{2R_L}$

$\frac{V_M}{R_L} = \frac{2V_{CC}}{\pi R_L}$

Therefore, $V_M = \frac{2V_{CC}}{\pi}$ is the condition for max power dissipation.

Sub $V_M=\frac{2V_{CC}}{\pi}$ $in\ (28) to\ get$ max $power\ dissipation$

$P_D=\frac{2V_{CC}}{\pi R_L} * \frac{2V_{CC}}{\pi} - (\frac{2V_{CC}}{\pi})^2 \frac{1}{2\pi R_L}$

$=\frac{V^2{}_{CC}}{\pi^2 R_L} - \frac{4V^2{}_{CC}}{\pi^2 R_L}$

Therefore, Maximum Power dissipation, $P_{DMAX}=\frac{2V^2{}_{CC}}{\pi^2 R_L} - - - - - - - - (29)$

Power dissipation of each transistor is $P_D=\frac{V^2{}_{CC}}{\pi {R_L}^2}$.....(30)

Problems:

1) Calculate the efficiency of class B amplifier for a supply voltage of V_{CC}=24V with the output load of i) $V_L(p)$=22V ii) $V_L(p)$=6V

Solution: Efficency, (i) $\eta=78.5(\frac{V_M}{V_{CC}})$ =78.5(22/24)=71.95%

V_M=6V, (ii) η =78.5*6/24=19.625%

2) For a class B amplifier providing a 20 V peak signal to a 16Ω loud speaker and a power supply of V_{CC}=30V. Calculate DC input power, AC output power and its efficiency.

Solution: V_M=20V; R_L=16 Ω

DC input power =$\frac{2V_{CC}V_M}{\pi_{RL}}=\frac{2*30*20}{\pi*16}$=23.87W

$P_{AC}=\frac{V^2{}_M}{2R_L}$=12.5W

$\eta =\frac{P_{AC}}{P_{DC}} = 52.37\%$

3) For a class B PA using a supply voltage of V_{CC}=30V and driving a load of rR_L=16 Ω, determine max power dissipation and power dissipation of each transistor

Solution: Maximum efficiency, $V_{CC}=V_M$

$P_{DC}(max)=\frac{2V_{CC}V_M}{\pi R_L} = 35.81W$

$P_{AC}(max)=\frac{V^2{}_M}{2R_L} = 28.125W$

$P_D(max)=\frac{2V^2{}_{CC}}{\pi R^2{}_L} = 11.396W$

Each transistor, P_D(max)=5.698W

ii) Complimentary-Symmetry Class B Power Amplifier

Complimentary-symmetry makes use of npn and pnp transistors. Compared to a push pull configuration, this circuitry provides many advantages.

1) No transformers are used; hence circuitry is less bulky and less costly.

2) Matched pair of npn and pnp are used in common collector configuration. CC configuration has high input impedance; therefore impedance matching is achieved in the circuitry itself.

3) Frequency response is improved as transformers are absent.

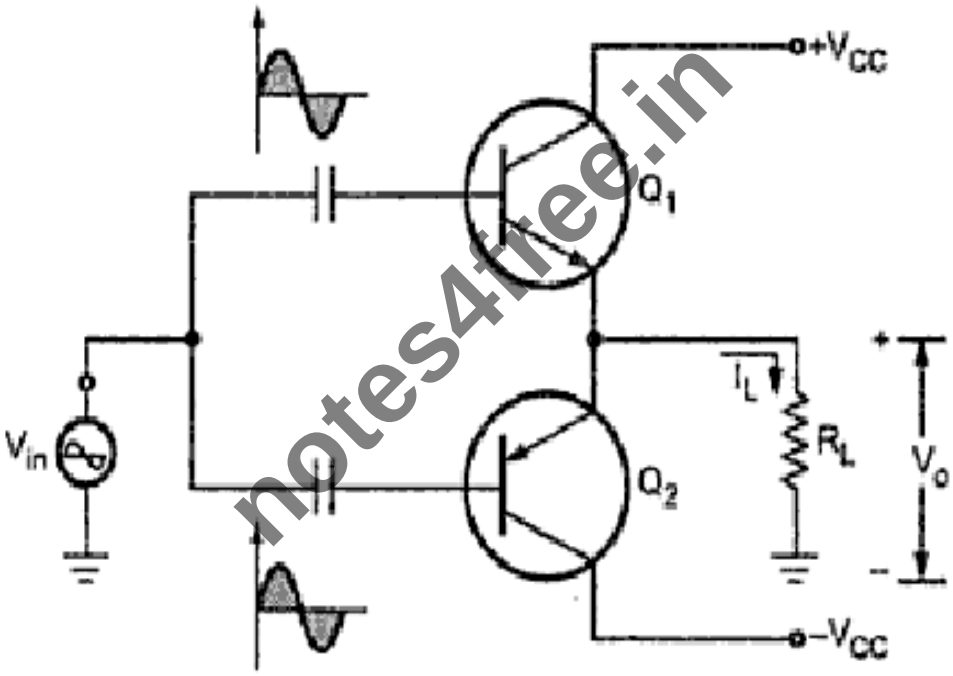


Figure 5.15 Complimentary Symmetry Class B Power Amplifier

Operation:

The basic circuitry of Complimentary-symmetry configuration is driven by dual power supply of +Vcc and –Vcc. Here Q1 is an npn and Q2 is pnp transistor. During Positive half cycle Q1 gets forward biased and conducts when input voltage becomes >0.7V, Q1 conducts and Positive half cycle appears across the load. During negative half cycle Q2 gets forward biased when the applied voltage becomes more negative than -0.7V, Q2 conducts and negative half cycle appears across the load, therefore output is present for entire 360^{o} of the input cycle.

There are 2 disadvantages associated with circuitry
1) Circuitry requires dual power supply.
2) Cross over distortion is present in the output.

Cross over distortion:

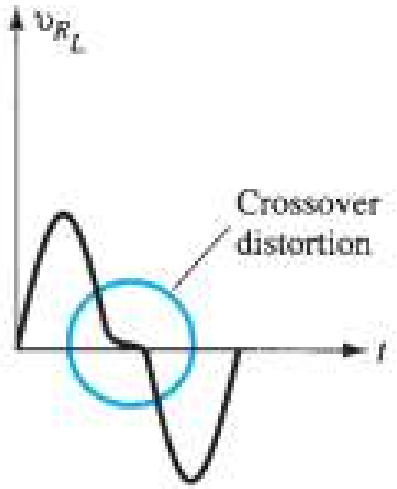


Figure 5.16 Cross over distortion in Class B Power Amplifier

In both transformers coupled push pull and complimentary symmetry configurations distortion is present at the zero crossings of the half cycle. This itself is termed as cross over distortion. In class B, There is no biasing done to ensure that transistor are on before an AC signal is applied. Typically transistors require a forward bias of 0.7V to turn on, therefore none of the transistors are on during zero crossing of half cycle.

Elimination of Cross over distortion:

To eliminate cross over distortion, some modifications are done in the basic circuits of class B amplifier circuit.

i) **Transformer coupled Push-pull Configuration:**

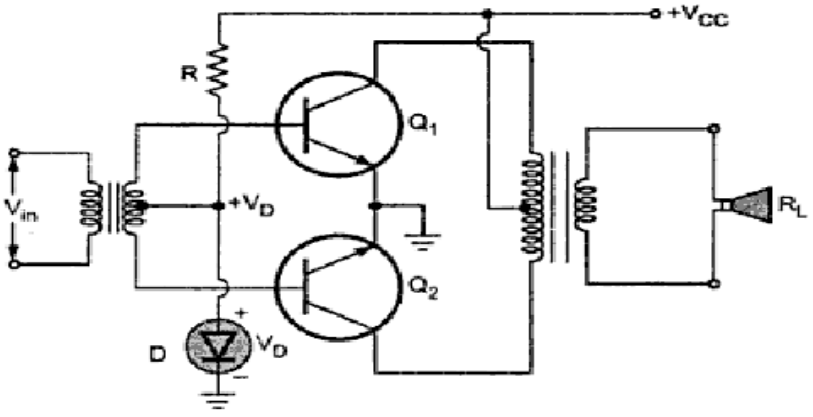


Figure 5.17 Transformer coupled Class B Power Amplifier free from Cross over distortion

Here push pull configuration is modified with the biasing circuitry so that it is free from cross over distortion. The forward bias of base to emitter junctions for both the transistors is provided by making use of a diode. The voltage drop across diode is equal to cut-in voltage of both the transistors. Therefore both the transistors conduct for full cycle making the circuit free from distortion.

Shift in Q pt: Due to forward bias supply Q pt shifts upwards on the DC load line characterizes. The circuit operation will be class AB instead of a class B operation. But shifts in Q pt can be neglected as it is very small.

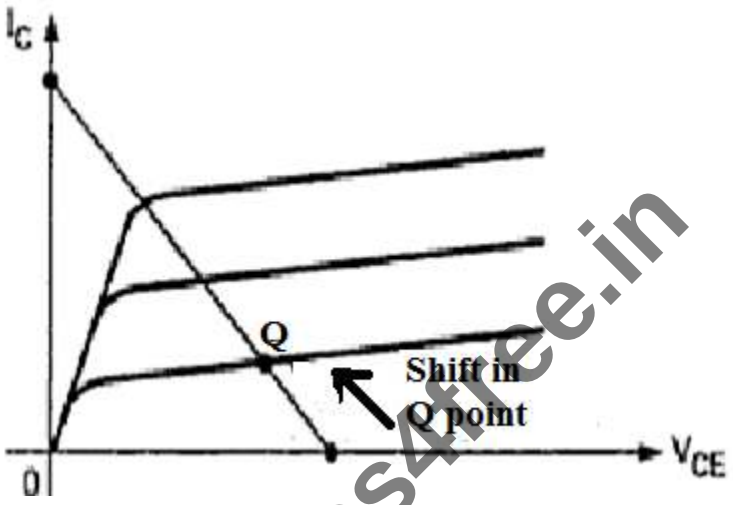


Figure 5.18 Change in Output characteristics of Class B Power Amplifier

5.4.1 Complimentary-Symmetry Circuits free from cross over distortion:

Here, Complimentary-Symmetry circuit is modified so that it is free from cross over distortion. The transistor Q1 should be provided with 0.7V across to its Base to emitter terminals and Q2 is -0.7V. This can be achieved by making value of resistances adjusting such that voltage drop across R2 is 1.4V therefore both the transistors conduct for full cycle eliminating cross over distortion at the output. The circuitry is show in Figure 5.19. It has a disadvantage with respect to change in temperature i.e. as the temperature increases, resistance associated with R2 increases and behavior of base to emitter junctions of Q1 and Q2 is opposite to it. This can be further nullified by making use of 2 diodes. The behavior of diode and p-n junction with respect to temperature and other external factors remains same. The modified circuitry is shown in Figure 5.20.

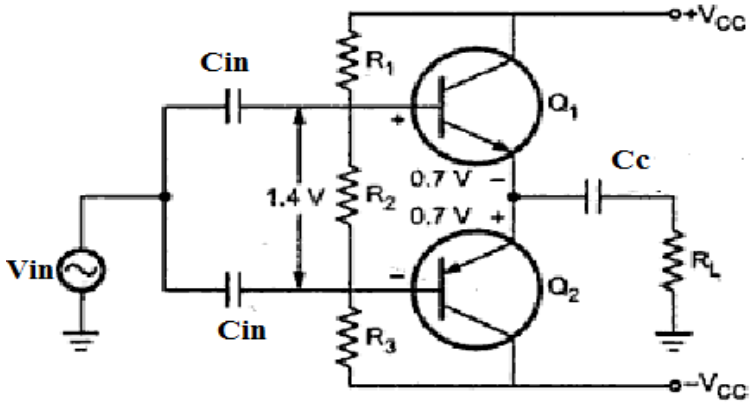


Figure 5.19 Class B Power Amplifier free from cross-over distortion

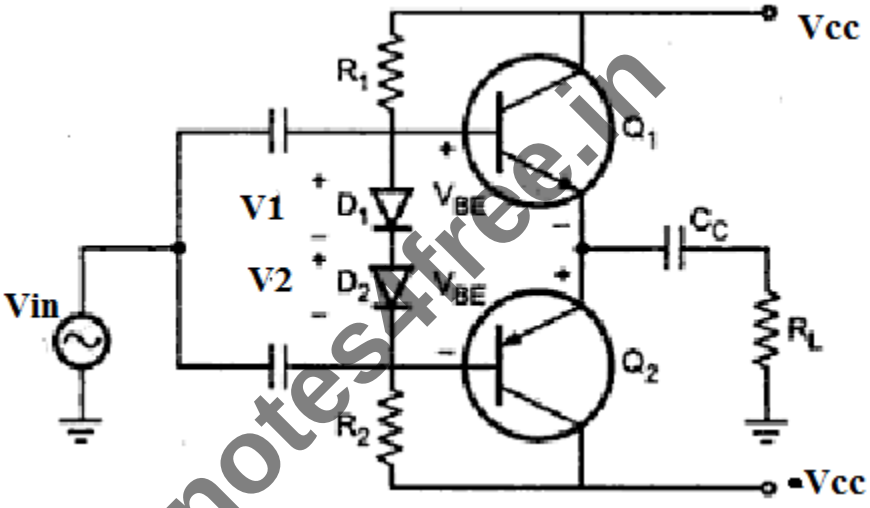


Figure 5.20 Modified Class B Power Amplifier free from cross-over distortion

Complimentary–symmetry circuit with single supply version

The drawback of dual power supply of Complimentary–symmetry configuration can be removed by making use of single supply. But fixed power supply of VCC is shared as VCC/2 by both the transistors.

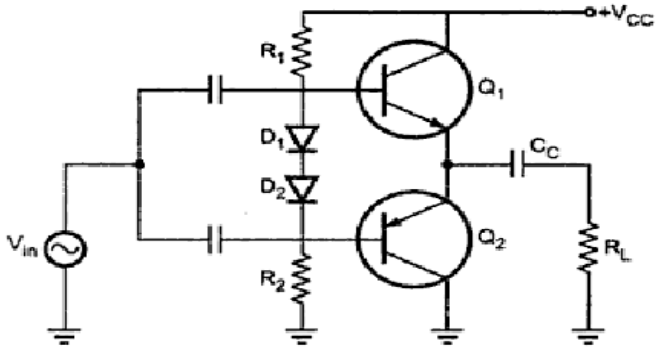


Figure 5.21 Complimentary–symmetry circuit with single supply version

Quasi – Complimentary Push pull configuration

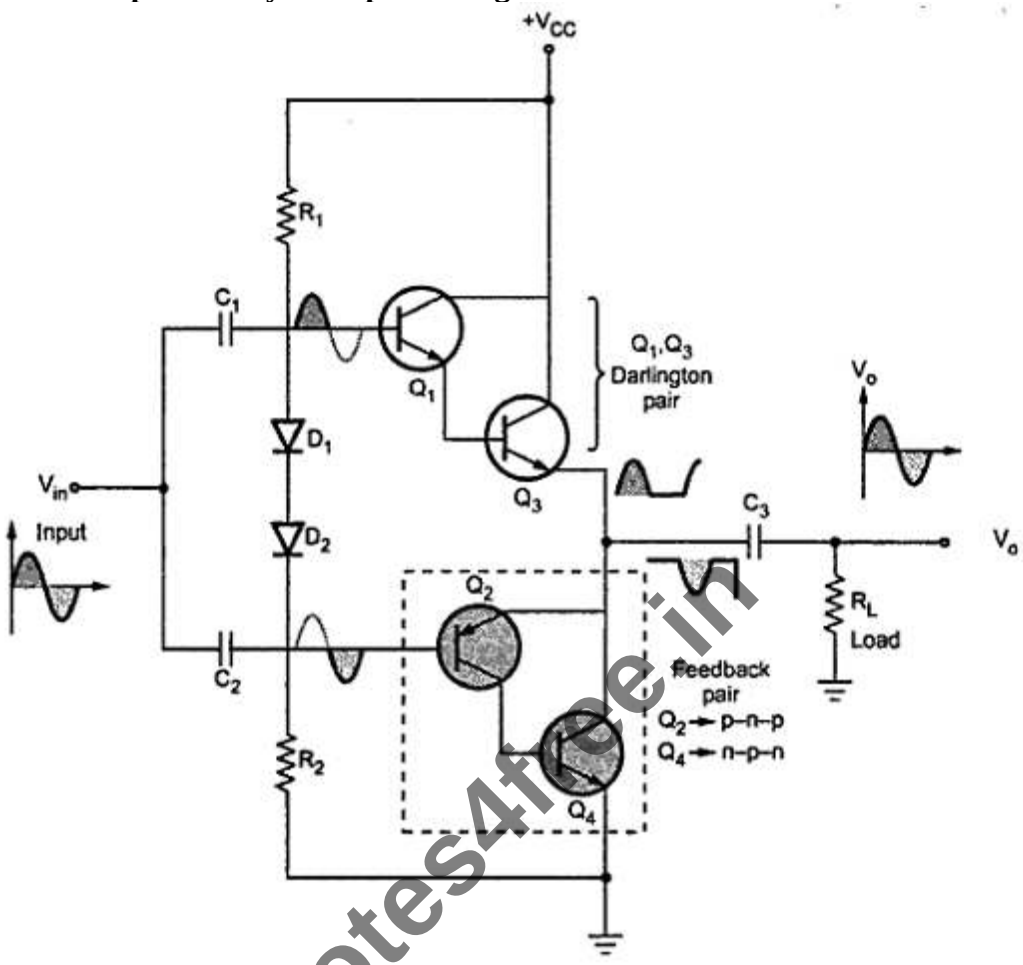


Figure 5.22 Quasi – Complimentary Push pull configuration

In order to provide high current output Complimentary–symmetry configuration can be modified by making use of additional npn transistors. So the above circuitry shows Quasi – Complimentary configuration where high gain npn transistor Q1 and Q2 are connected in a Darlington Configuration providing high current output during Positive half cycle. Q2 and Q4 forms a feedback pair providing high current output during negative half cycle. This is the most popular circuit of class B configuration.

Note: The formula derived for push pull configuration is applicable to all the circuits of class B amplifiers. In case of single supply version Vcc should be considered as Vcc/2 in all calculations.

1) Calculate output power, power dissipation, power handled by each transistor and circuit efficiency for an input of $+12V_{RMS}$

Solution: Peak input voltage $=\sqrt{2}\ V_{RMS}=\sqrt{2}*12=17V$, $Vcc=+25V, R_L=4\Omega$

DC input power, $P_{DC}=VccI_{DC}=\frac{V_{CC}2I_M}{\pi}=\frac{2V_{CC}V_M}{\pi R_L}=67.63W$

AC output power, $P_{AC}=\frac{V^2{}_M}{2R_L}=36.125W$

$P_D=P_{DC}-P_{AC}=31.625W$

Power handled by each transistor, $P_D/2$ =15.8W

$\eta = \frac{P_{AC}}{P_{DC}} * 100\% = 53.4\%$

2) For the same circuit shown calculate maximum input power, max output power and power dissipation

Max input power, V_M=Vcc

$P_{DC} = \frac{2VCC^2}{\pi R_L} = 99.46W$

$P_{AC} = \frac{V^2 CC}{\pi^2 R_L} = 31.654W$

Power dissipation, P_{DC}-P_{AC}=21.335W

5.5 Distortion in Power amplifiers

Any amplifier is subjected to three types of distortions,

1) Amplitude distortion 2) Frequency distortion and 3) Phase distortion.

Typically power amplifier should be free from all these distortions, human errors are not sensitive to phase of the signal, therefore phase distortion can be neglected as well as frequency distortion. Amplitude distortion is a major source of distortion in power amplifiers.

Amplitude distortion (Harmonic Distortion)

It is caused due to harmonics present in the output signal. Hence it is referred to as harmonic distortion. If the desired freq component is coswt, the output contains harmonics which are multiples of fundamentals at freq 'w' i.e. output contain cos 2wt, cos3wt.....cosnwt. Refer Figure 5.23. As the order of harmonic increases with coswt, the amplitude of harmonics decreases. Therefore net output is resultant of all these harmonics.

Harmonic distortion caused by n^{th} harmonic component can be expressed as

$D_n = \frac{|A_N|}{|A_1|} * 100\% - - - - - - - - (31)$

Where A_n is the amplitude of the n^{th} harmonic component and A_1 is the amplitude of fundamental harmonic component.

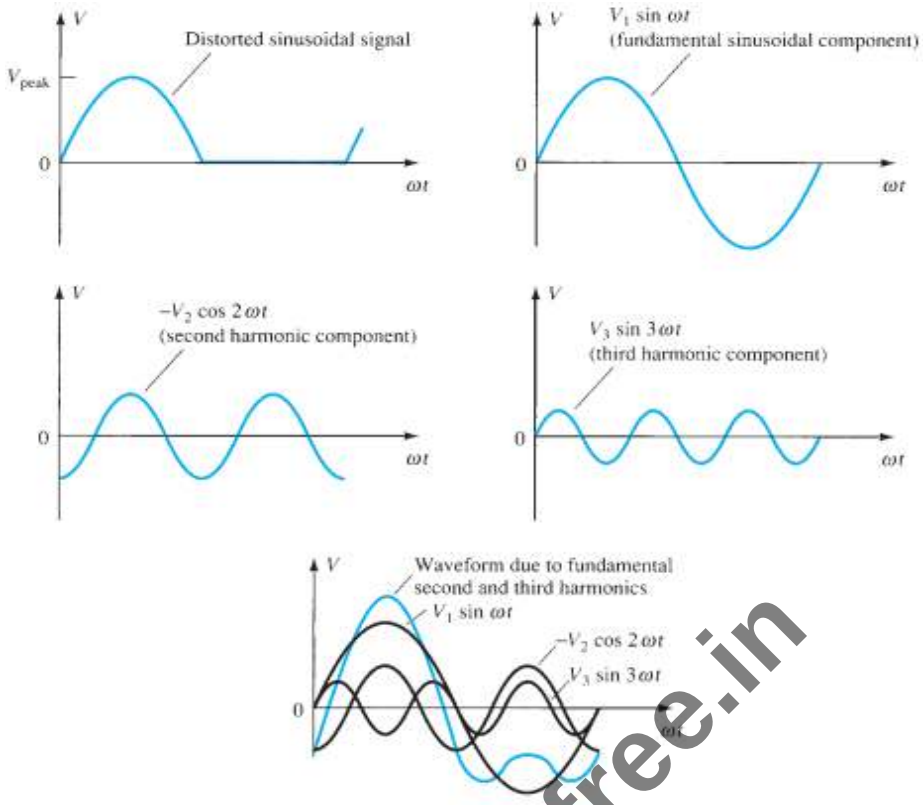
The amplitude distortion due to 2^{nd} harmonic component can be expressed as

$D_2 = \frac{|A_2|}{|A_1|} * 100\% - - - - - - - - (32)$

Where A_2 is amplitude of 2^{nd} harmonic component..

Harmonic distortion caused by all the harmonics can be expressed as

$D = (\sqrt{D_2^2 + D_3^2 + \cdots D_N^2}) * 100\% - - - - - (33)$



. Figure 5.17 Harmonic distortion in Class B Power Amplifiers

1) Calculate harmonic distortion component for an output signal having fundamental component of 2.5V, 2nd harmonic component of 0.25 and third harmonic component of 0.1V 4th harmonic component of 0.05. Also calculate total harmonic distortion

Solution: We know that harmonic distortion caused by nth component is $\frac{|A_N|}{|A_1|} * 100\%$

Distortion caused by 2nd component $\frac{|A_2|}{|A_1|} * 100\%$

i) D_2=0.25/2.5*100% =0.1=10%

ii)D3=0.1/2.5*100%=0.04=40%

iii)D4=0.05/2.5-100%=0.02=20%

Total distortion is given by,

D=$(\sqrt{D_2^2 + D_3^2 + \cdots D_N^2}) * 100\%$=$\sqrt{(0.1)^2 + (0.04)^2 + (0.02)^2}$=0.1095*100%=10.95%

5.5.1 Analysis of 2nd harmonic Distortion

2nd harmonic component has the largest amplitude of all others harmonics these is the major source of harmonic distortion. Harmonics are introduced due to non-linear behavior of transistor as shown in figure 5.18. Transistor is a non-linear device. Output quantity Ic can be related to I_B using the relation given by,

$i_c=G_1i_b+G_2i^2_b$----------(34)

where, G1 and G2 are constants of proportionality, i_c and i_b are instantaneous collector and base currents respectively. Let $i_b= I_m$coswt----------(35)

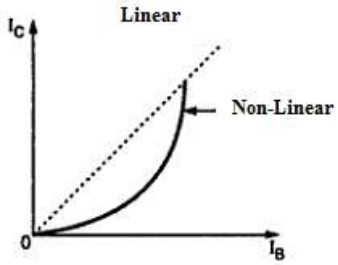


Figure 5.18 Non-linear behavior of transistor

$i_c=G_1(I_m\cos wt)+G_2(I_m\cos wt)^2$-----(36)

$=G_1I_m\cos wt+\frac{G_2I_M^2}{2}+\frac{G_2I_M^2}{2}\cos 2wt$

$i_c=A_0+A_1\cos wt+A_2\cos 2wt$---------(37)

$i_c=I_{CQ}+A_0+A_1\cos wt+A_2\cos 2wt$---(38)

Where A0 is a constant which indicates a rectifying term. $A_1\cos wt$ is the derived fundamental component $A_2\cos wt$ is the derived harmonic component which needs to be calculated since the transistor is DC biased, the collector current can be expressed as in eq(37). Collector current can be represented as shown in the figure 5.19.

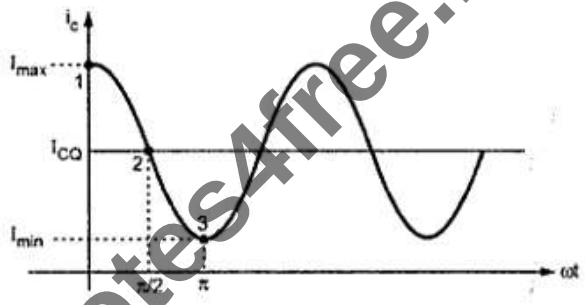


Figure 5.19 Collector current waveform

Put wt=0 in eq(37)

$I_{CMAX}=I_{CQ}+A_0+A_1+A_2$----------(39)

Putting $wt=\frac{\pi}{2}$

$ic=I_{CQ}+A_0-A_2$----------(40)

Putting $wt=\pi$

$I_{CMIN}=I_{CQ}+A_0-A_1+A_2$----------(41)

$I_{CMAX}-I_{CMIN}=8A_1$

$A_1=\frac{I_{CMAX}-I_{CMIN}}{2}$

$I_{CMAX}+I_{CMIN}=2A_0+2I_{CQ}+2A_2$

WKT at $wt=\frac{\pi}{2}$

$Ic=I_{CQ}=I_{CQ}+A_0$

$I_{CMAX}+I_{CMIN}=4A_2+2I_{CQ}$

$A_2=\frac{I_{CMAX}+I_{CMIN}+2I_{CQ}}{4}$----------(42)

Harmonic distortion can be expressed as

$D_2=\frac{|A_2|}{|A_1|}=\frac{\frac{I_{CMAX}+I_{CMIN}+2I_{CQ}}{4}}{\frac{I_{CMAX}-I_{CMIN}}{2}}$

$D_2=\frac{\frac{1}{2}(I_{CMAX}+I_{CMIN})-I_{CQ}}{I_{CMAX}-I_{CMIN}}$----------(43)

In terms of collector voltages harmonics distortion can be expressed as

$D_2=\frac{\frac{1}{2}(v_{CEMAX}+V_{CEMIN})-V_{CEQ}}{V_{CEMAX}-V_{CEMIN}}$----------(44)

Power output due to harmonics:

The input power can be expressed as

$P_i=V_{RMS}I_{RMS}=\frac{V_M I_M}{2}=\frac{I_M^2 R_L}{2}-----(45)$

Where, I_m is peak value of current. The fundamental components power can be expressed as $P_1=\frac{A_1^2 R_L}{2}----------(46)$

Where A_1 is the amplitude of fundamental component. The output power includes fundamental component and all the harmonics. Therefore total output power can be expressed as

$P_0=\frac{A_1^2 R_1}{2}+\frac{A_2^2 R_L}{2}+\cdots+\frac{A_N^2 R_L}{2}$

$=\frac{A_1^2 R_1}{2}(1+\frac{A_1^2}{A_1^2}+\frac{A_3^2}{A_1^2}+\cdots+\frac{A_N^2}{A_1^2}$

$P_I=(1+D_2^2+D_3^2+\cdots+D_N^2$

$P_0=P_1(1+D^2)$ ----------(47)

Where D_n is harmonic distortion due to n^{th} harmonic distortion and D is total harmonic distortion.

Problem

Q) For an harmonic distortion reading $D_2=0.1$, $D_3=0.02$, $D_4=0.01$ with fundamental component of current as 4A and a load resistance of 8Ω, calculate power output due to harmonics, fundamental power and total harmonic distortion.

Solution: $I_1=A_1=4A$, $R_l=8\Omega$

$P_0=P_1(1+D^2)$

$P_I=(1+D_2^2+D_3^2+\cdots+D_N^2)=(0.1)^2+(0.02)^2+(0.01)^2=0.0105$

$P_0=\frac{A_1^2 R_1}{2}(1.0105)=\frac{4^2*8}{2}=64.67W$

5.6 Class C Power Amplifiers

In class C operation, the transistor is biased well beyond cutoff , therefore collector current flows for less than 180^o resulting in an output of all small pulse, therefore class C is not suitable for audio frequency amplification instead it is employed as stable frequency generator in all communication transmitter and receivers. Efficiency of class C power amplifies is nearly 100%. The tuned LC circuit acts as a load for a class c power amplifiers. Class C amplifiers produce series of pulses including fundamentals and

harmonics. LC circuit takes only fundamental frequency and results into oscillations; therefore output is far from harmonics.

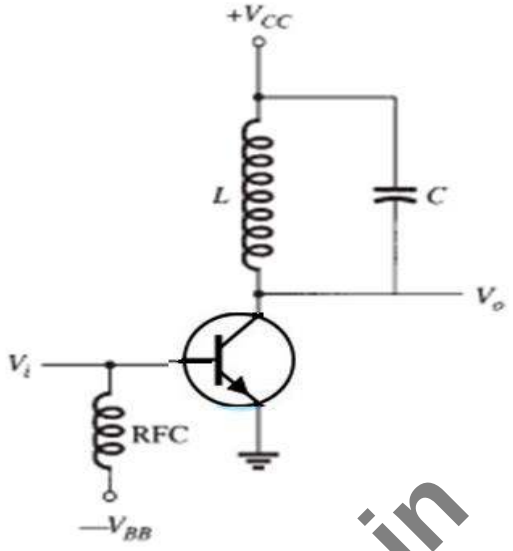


Figure 5.20 Class C Power Amplifier

5.7 Class D Power Amplifier:

Class D power amplifiers make use of digital techniques to provide amplification for Analog Signals. Typical Class D power amplifier switches are shown in Figure 5.22. Figure 5.21 shows the block diagram of Class D Power Amplifier. Comparator compares instantaneous saw tooth waveform amplitude with input signal. If difference is positive comparator output switches the Class D power amplifier. Amplifier output will be Pulse which will be on as long as comparator output being positive difference. This output is fed to low-pass filter which recovers the original signal back.

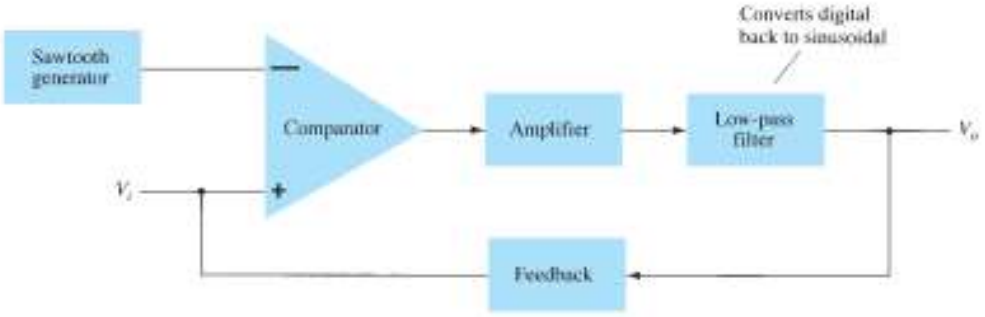


Figure 5.21 Block Diagram of Class D Power Amplifier

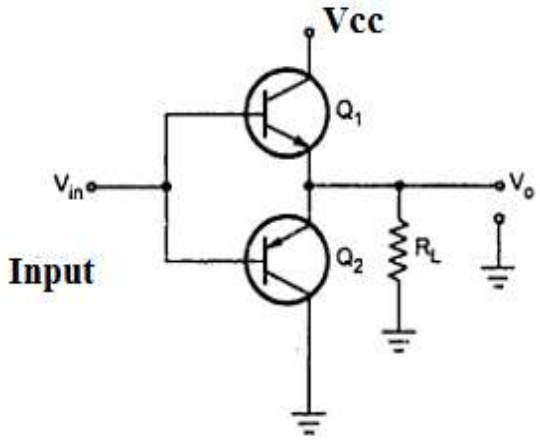


Figure 5.22 Class D Power Amplifier Switches

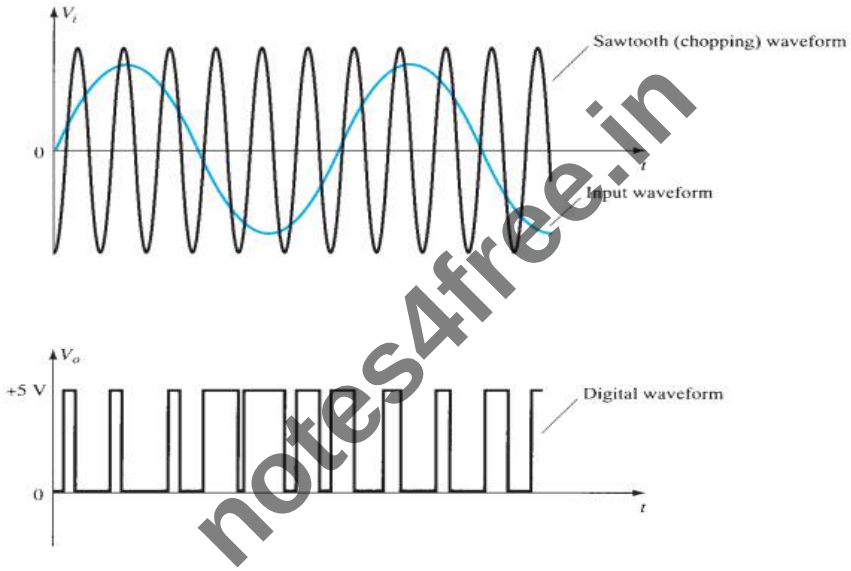


Figure 5.23 Class D Power Amplifier Waveforms

6 Voltage Regulators

6.1 Introduction

Voltage regulators are the important constituents of any power supply. All the Regulated DC Power supplies and Switched-Mode Power supplies make use of voltage regulators. Voltage regulator is used for two reasons:-

1. To regulate or vary the output voltage of the circuit.
2. To keep the output voltage constant at the desired value in-spite of variations in the supply voltage or in the load current.

Figure 6.1 shows the block diagram of typical Power supply. Input ac voltage is stepped down by making use of Transformer. Full wave rectifier converts the incoming ac into a pulsating DC. Further filter smoothens out the pulsating DC. This Pulsating DC is regulated by making use of IC regulator. Output of regulator is a constant DC which is fed to load.

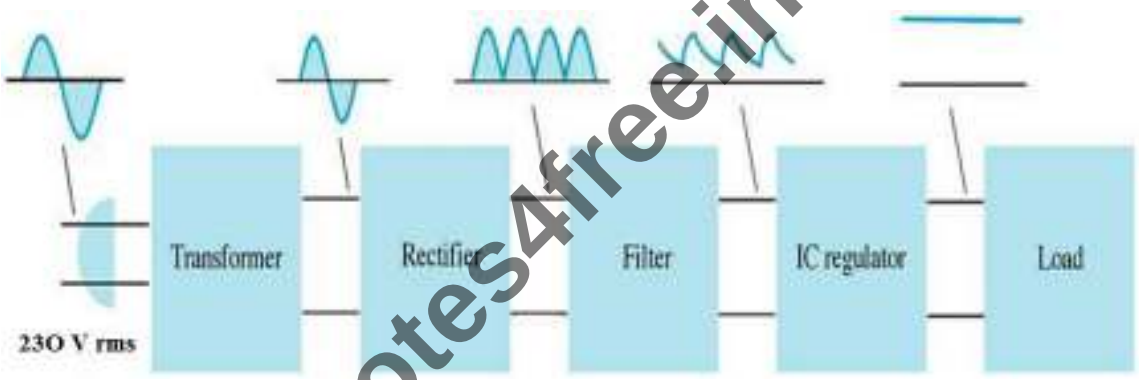


Figure 6.1 Block diagram of Power Supply

6.2 Series voltage regulator

Here the control element transistor/control element is connected in series with the input. Output is fed back to a sampling circuit which samples a part of output and couples it to comparator. Comparator compares the reference voltage with output of sampling circuit. If the output voltage increases, the comparator circuit provides a control signal to cause the series control element to decrease the amount of the output voltage there by regulating the output voltage.

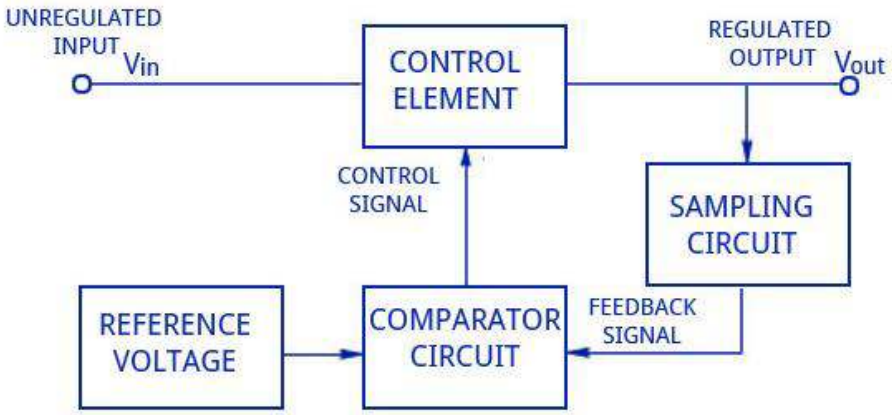


Figure 6.2 Block diagram of series voltage regulator

Courtesy: www.CircuitsToday.com

6.2.1 Simple Series Voltage Regulator Circuit

Here transistor is in series with the load. Such a circuit is also named an emitter follower voltage regulator. It is called so because the transistor used is connected in an emitter follower configuration. The circuit consists of an N-P-N transistor and a zener diode. As shown in the figure below, the collector and emitter terminals of the transistor are in series with the load. Thus this regulator has the name series in it. The transistor used is a series pass transistor. Circuitry is shown in Figure 6.3.

The output of the rectifier that is filtered is then given to the input terminals and regulated output voltage Vout is obtained across the load resistor R_L. The reference voltage is provided by the zener diode and the transistor acts as a variable resistor, whose resistance varies with the operating conditions of base current. The main principle behind the working of such a regulator is that a large proportion of the change in supply or input voltage appears across the transistor and thus the output voltage tends to remain constant. The output voltage can thus be written as,

$$Vout = Vz - V_{BE} \quad \text{.....(48)}$$

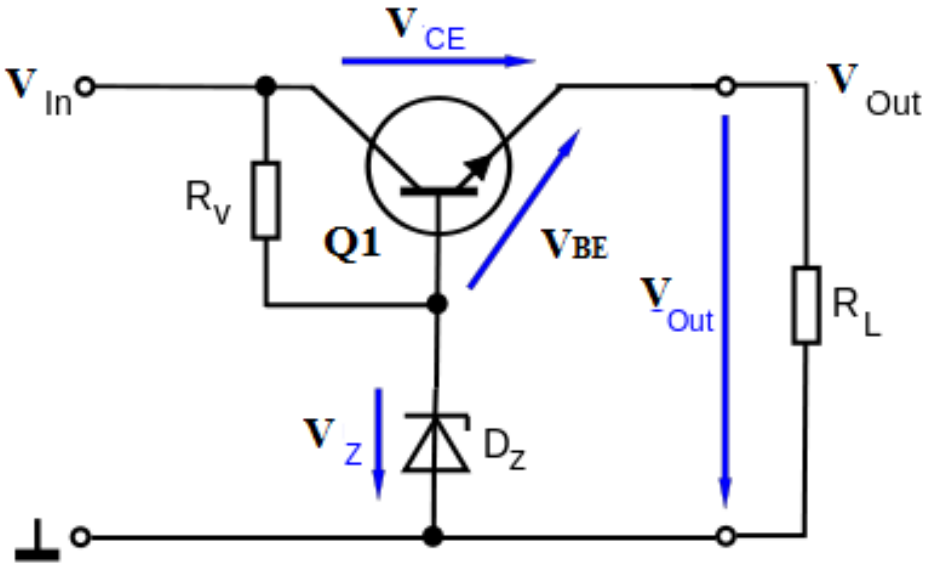


Figure 6.3 Simple Series Voltage Regulator Circuit

When the input supply voltage Vin increases the output voltage Vout also increases. This increase in Vout will cause a reduced voltage of the transistor base emitter voltage Vbe as the zener voltage Vz is constant. This reduction in V_{BE} causes a decrease in the level of conduction which will further increase the collector-emitter resistance of the transistor and thus causing an increase in the transistor collector-emitter voltage and all of this causes the output voltage Vout to reduce. Thus, the output voltage remains constant. The operation is similar when the input supply voltage decreases.

An improved series regulator circuit is shown in Figure 6.4. Resistors R1 and R2 act as a sampling circuit, with Zener diode D_Z providing a reference voltage, and transistor Q2 then controls the base current to transistor Q1 to vary the current passed by transistor Q1 to maintain the output voltage constant

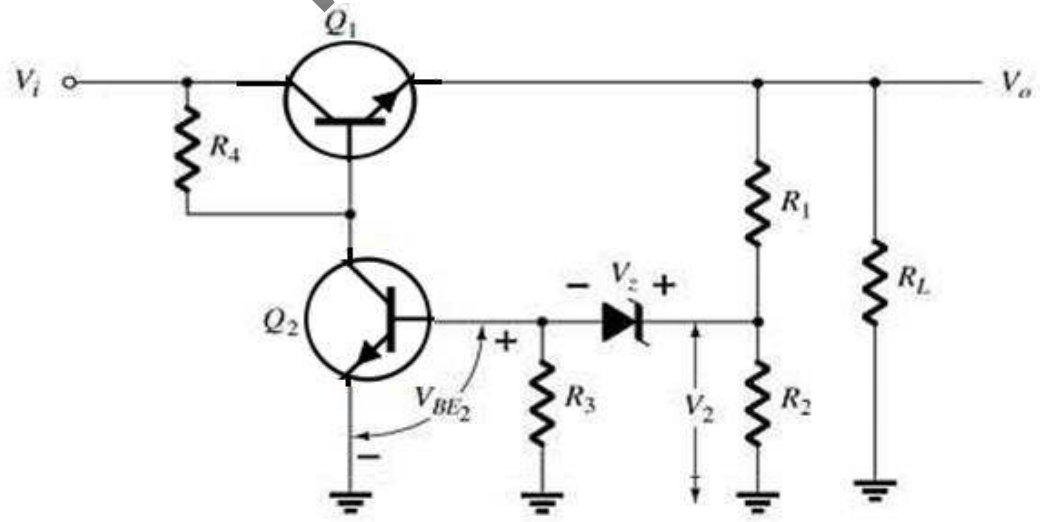


Figure 6.4 Improved Series Voltage Regulator Circuit

6.2.2 Series Voltage Regulator Circuit using op-amp

Here Zener diode provides a constant reference voltage at non-inverting terminal of op-amp. Output voltage is sampled via potential divider network and is fed to inverting terminal. Depending on variation in output voltage the output voltage of op-amp changes and in-turn transistor's control voltage changes. This ensures constant output voltage (Refer Figure 6.5).

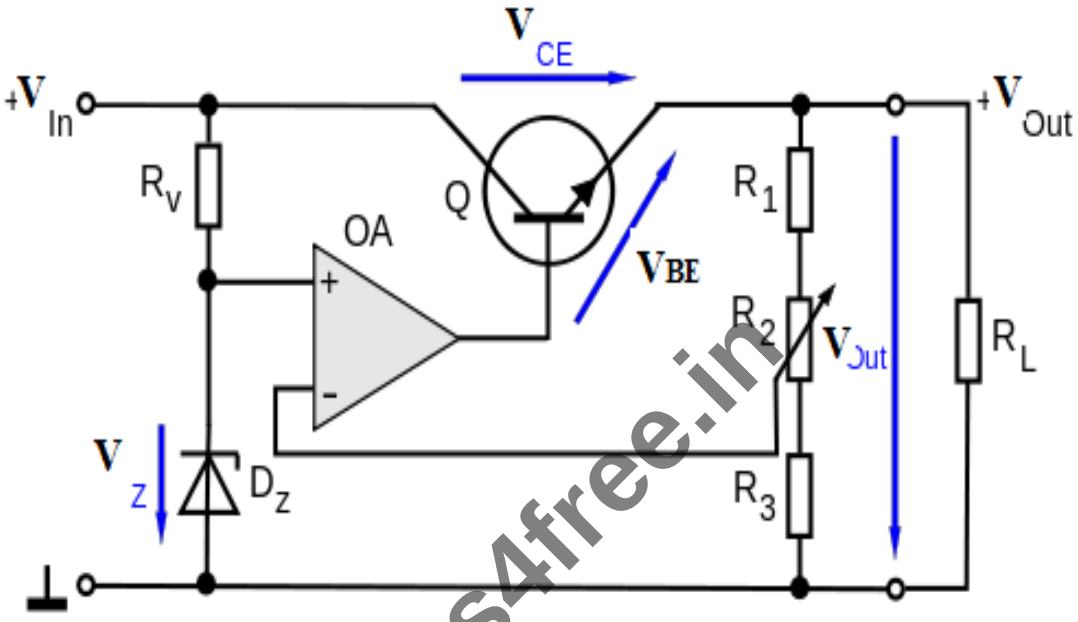


Figure 6.5 Op-amp Series Voltage Regulator

6.2.3 Over-current protection

Figure 6.6 shows how the series stabilizer can be protected against excessive current being drawn by the load. This will prevent damage to the supply in the event of too much current being drawn from the output, or even a complete short circuit across the output terminals. Two components have been added, Q2 and Rp. The resistor Rp is a very low value When the load current rises above a predetermined value, the small voltage developed across Rp will become sufficient to turn Q2 on. As Q2 is connected across the base/emitter junction of the main control transistor Q1, the action of turning Q2 on will reduce the base/emitter voltage of Q1 by an amount depending on the amount of excess current. The output current will not be allowed to increase above a predetermined amount, even if a complete short circuit occurs across the output terminals.

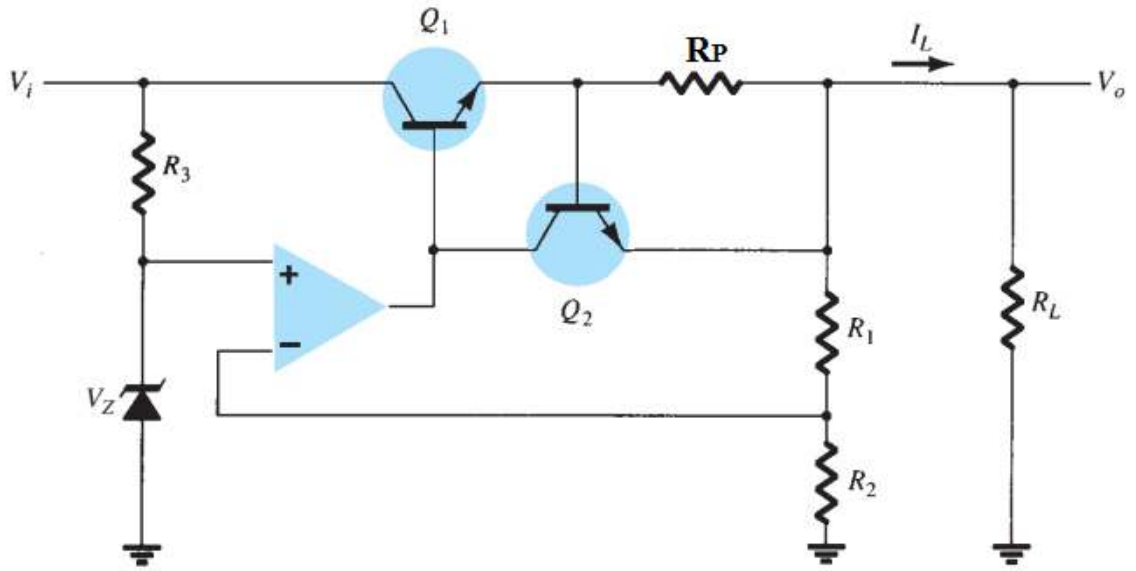


Figure 6.6 Current-Limiting Voltage Regulator Circuit

6.3 Shunt Voltage Regulator

The block diagram of a discrete transistor shunt voltage regulator is given in Figure 6.7. As the name says the voltage regulation is provided by shunting the current away from the load. The control element shunts a part of the current that is produced as a result of the input unregulated voltage that is given to the load. Thus the voltage is regulated across the load. Due to the change in load, if there is a change in the output voltage, it will be corrected by giving a feedback signal to the comparator circuit which compares with a reference voltage and gives the output control signal to the control element to correct the magnitude of the signal required to shunt the current away from the load.

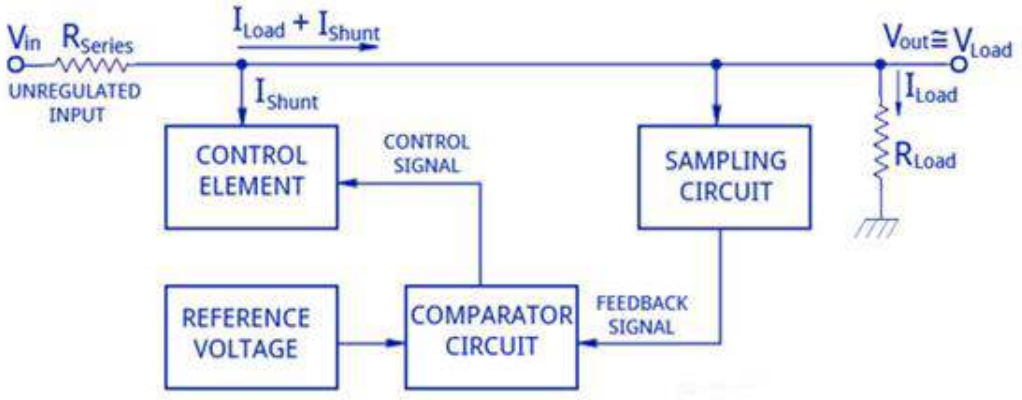


Figure 6.7 Block Diagram of Shunt Voltage Regulator

Courtesy: www.CircuitsToday.com

If the output voltage increases, the shunt current increases and thus produces less load current and maintains a regulated output voltage. If the output voltage reduces, the shunt current reduces and thus produces more load current and maintains a regulated constant

output voltage. In both cases, the sampling circuit, comparator circuit and control element plays an important role.

6.3.1 Simple Shunt Voltage Regulator Circuit

The circuit consists of an NPN transistor and a zener diode along with a series resistor Rs that is connected in series with the input supply. The zener diode is connected across the base and the collector of the transistor which is connected across the output. The circuit consists of an NPN transistor and a zener diode along with a series resistor Rs that is connected in series with the input supply. The zener diode is connected across the base and the collector of the transistor which is connected across the output.

The output voltage to the load is given by,

$$V_L=V_Z+V_{BE}.....(50)$$

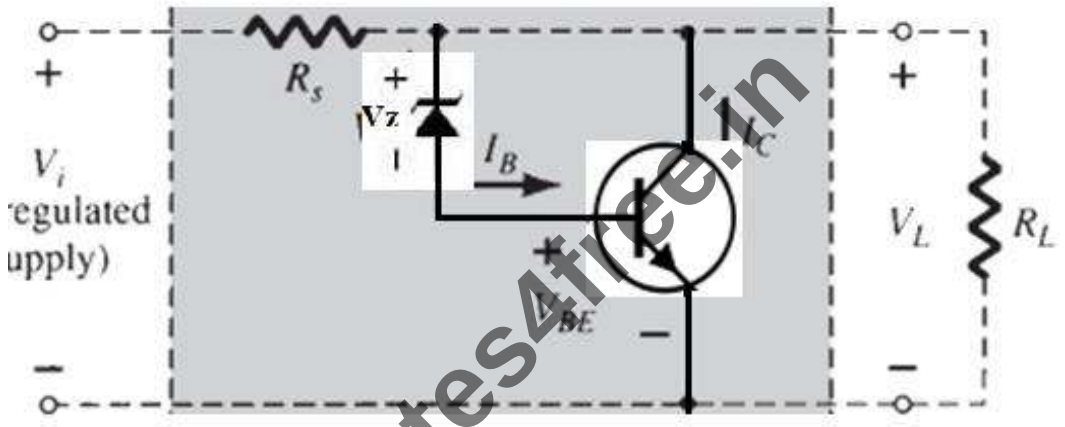


Figure 6.8 Simple Shunt Voltage Regulator Circuit

6.3.2 Improved Shunt Voltage Regulator Circuit

The circuit of Figure 6.8 can be improved as shown in Figure 6.9. As the output voltage tries to change, the current shunted by transistor Q1 is varied to maintain the output voltage constant. Transistor Q2 provides a larger base current to transistor Q1 so that larger load current can be handled.

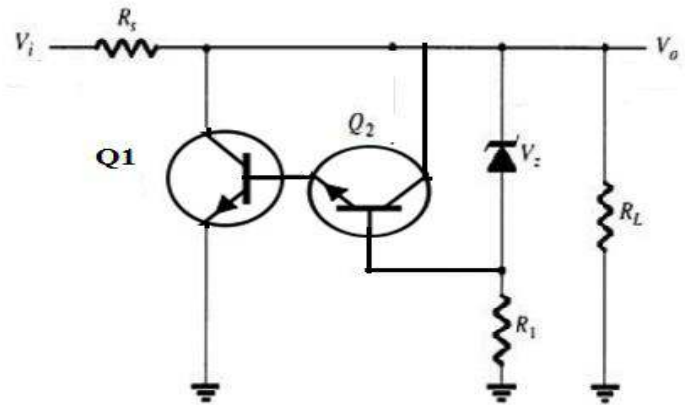


Figure 6.9 Improved Shunt Voltage Regulator Circuit

6.3.3 Shunt Voltage Regulator using op-amp

Here Zener diode provides a constant reference voltage at non-inverting terminal of op-amp. Output voltage is sampled via potential divider network and is fed to inverting terminal. Depending on variation in output voltage the output voltage of op-amp changes and in-turn transistor's control voltage changes. This ensures constant output voltage (Refer Figure 6.10).

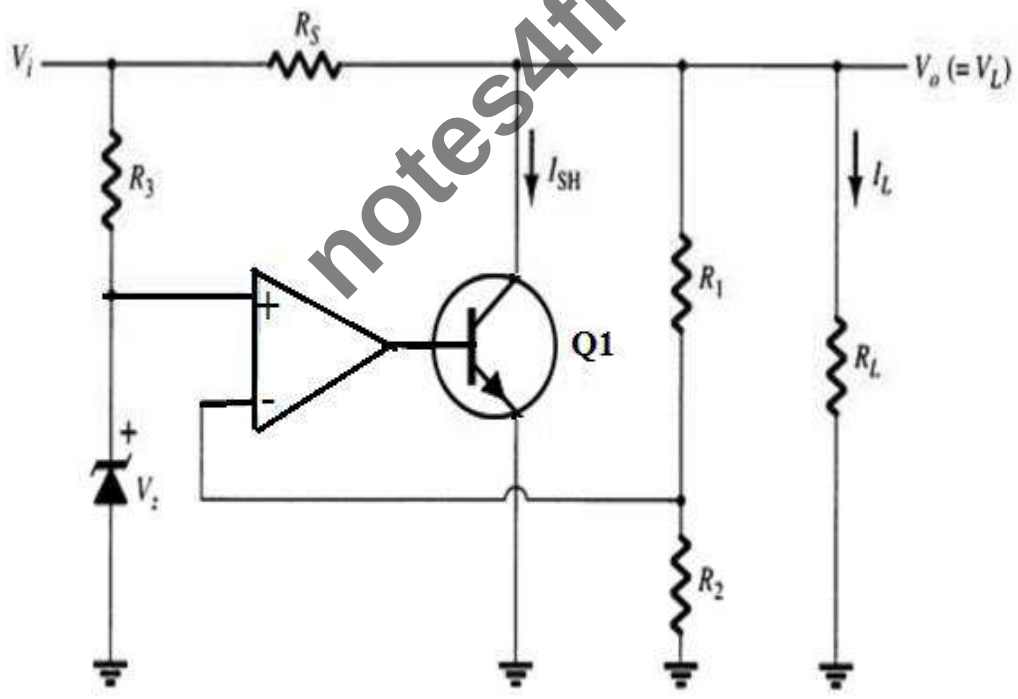


Figure 6.10 Shunt Voltage Regulator using op-amp

6.4 Switching Regulators

Switching regulators make use of power electronics devices to provide a constant and efficient dc supply. Basically, a switching regulator passes voltage to the load in pulses, which are then filtered to provide a smooth dc voltage. Block diagram of 3 terminal switching voltage regulators is shown in Figure 6.11.

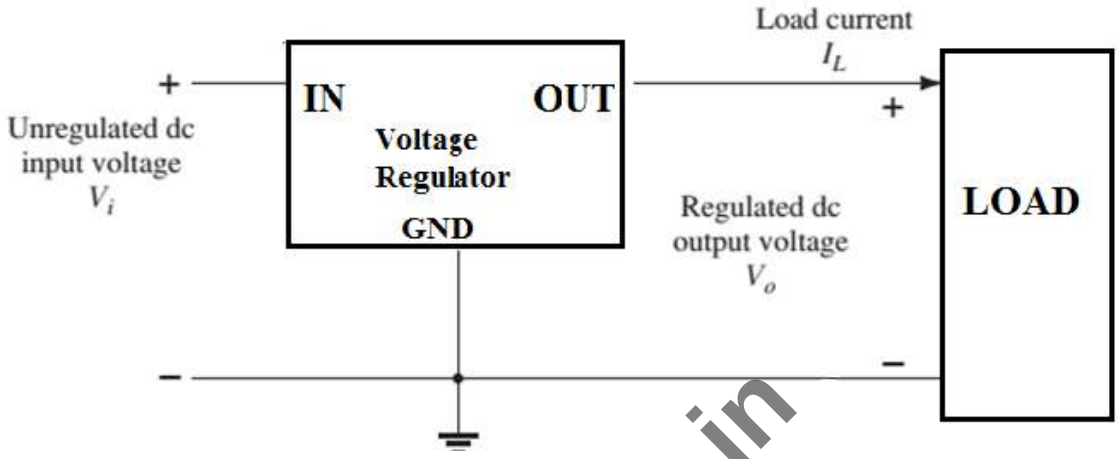


Figure 6.11 Block diagram of Switching Regulators