Module 1

Semiconductor Diodes & Applications

p-n junction diode, equivalent circuit of diode, Zener Diode, Zener diode as a voltage regulator, Rectification - Halfwave rectifier, Full wave rectifier, Bridge rectifier, Capacitor filter circuit [2.2, 2.3 2.4 of Text 1)

photodiode, LED, photo Coupler. (2.7.4, 2.7.5 & 2.7.6 of Text 1)

78XX series & 7805 Fixed IC Voltage Regulator (8.4.4 & 8.4.5 of Text 1).

(RBT Levels L1, L2 & L3)

Semiconductor Diodes :-

Diode approximation :-

The Diode approximations are

(i) Ideal diode approximation

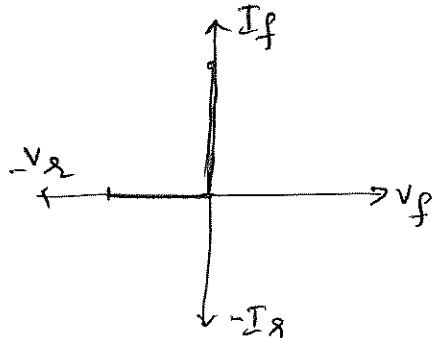
(ii) Second approximation

(iii) Linear piecewise approximation or Third approximation.

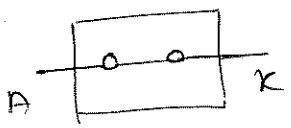
Ideal Diode Approximation

An equivalent circuit is defined as a combinational network of passive elements, voltage source etc. It is used to replace the active device for the purpose of mathematical & Analytical Analysis.

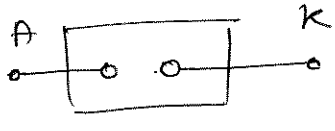
In ideal diode equivalent circuit, the diode is as switch. When diode is forward biased. it is treated as short circuit, with no resistance being offered, i.e $R = 0\ \Omega$. But when it is reverse biased treated as open circuit. Ideal characteristics are shown below. When reverse biased Resistance is infinity.



Ideal characteristics



Forward Biased. Closed circuit

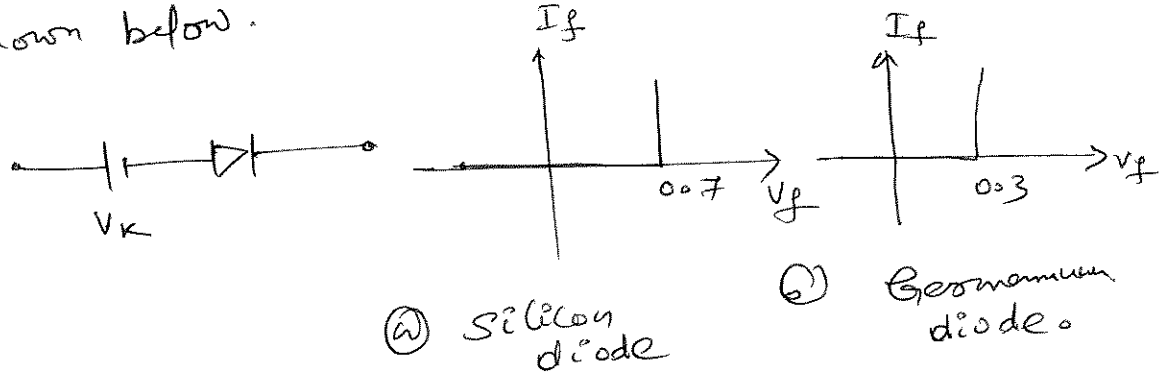


Reverse Biased. open circuit

Second approximation

It is also called as modified equivalent circuit. Practically no diode is ideal. Hence for analysing some circuit more accurate approximation is required. & it's called second approximation.

To an ideal equivalent circuit, add the cut in (or knee) voltage V_K (for Si Diode = 0.7 V, Ge Diode = 0.3 V). This will shift the characteristics towards right by an amount equal to V_K. modified equivalent circuit is shown below.

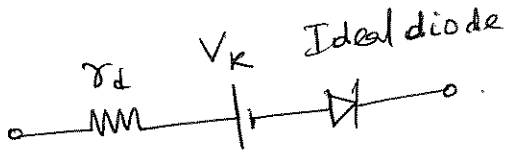


(a) Silicon diode (b) Germanium diode.

Fig (2) second approximation.

Piecewise linear equivalent (approximation) circuit.

The approximation of characteristics with the help of pieces of straight line is called linear piecewise approximation. To the modified equivalent circuit, a forward resistance of r_d is added as shown in figure. Due to addition of r_d the vertical straight characteristics of modified equivalent line will bend towards right resulting in a slope as shown in figure below. when diode is forward biased. The current starts flowing only after V_K (volts). The current then increases linearly with voltage having a slope of $\frac{1}{r_d}$ when diode is reverse biased the diode acts as open circuit offering infinite resistance.



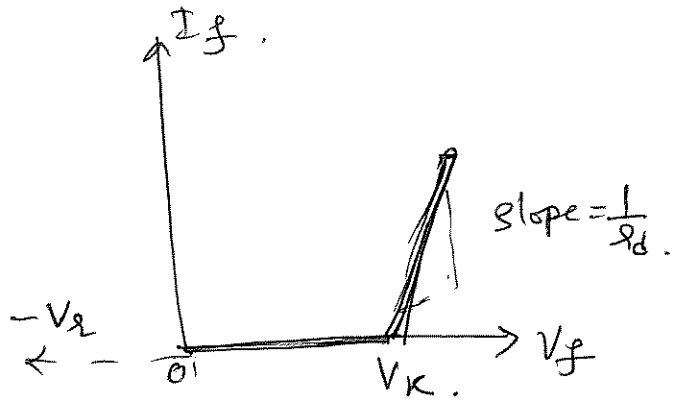


Figure (3). Piecewise linear model $\frac{1}{r_d} I_R$.

Semiconductor Diodes & Applications.

Pn-Junction Diode;-

Pn junctions (Diodes) are semiconductor devices which conduct only in one direction.

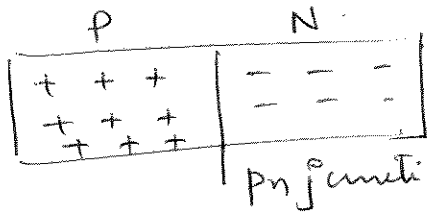
The pn junction ~~can be formed~~ is defined as the junction formed by attaching a p-type & an N-type semiconductor. once the pn junction is formed, the charge carriers are subjected to movement across the pn junction. This process is Transport phenomenon.

Transport phenomenon is defined as the process of movement of charge carriers across the p-n junction in the absence of any external electric field.

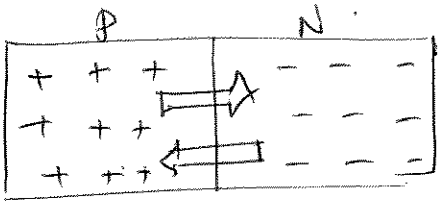
Diffusion process:- It can be defined as the process of movement of majority charge carriers across the junction when there is no external voltage applied.

Due to diffusion process, the majority charge carriers cross the junction & then meets a charge of opposite polarity on the other side of the pn-junction & the charge gets neutralized. The process of charge cancellation is called recombination.

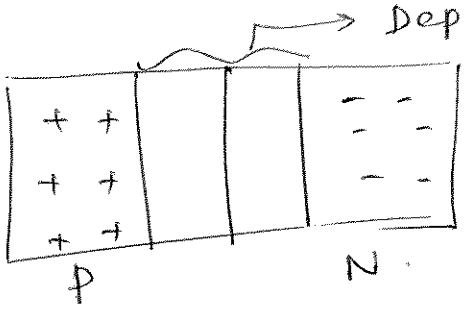
Due to Recombination process on either side of junction a region exists without any charge carriers is called depletion region. This region contains neither electrons nor holes.



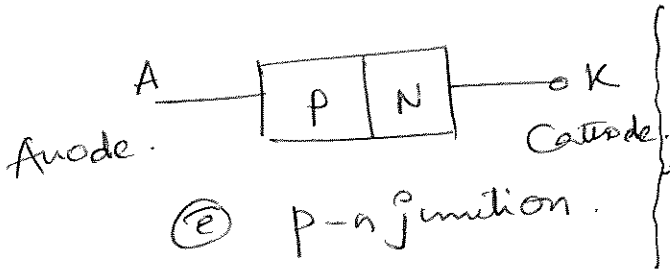
(a) pn-junction.



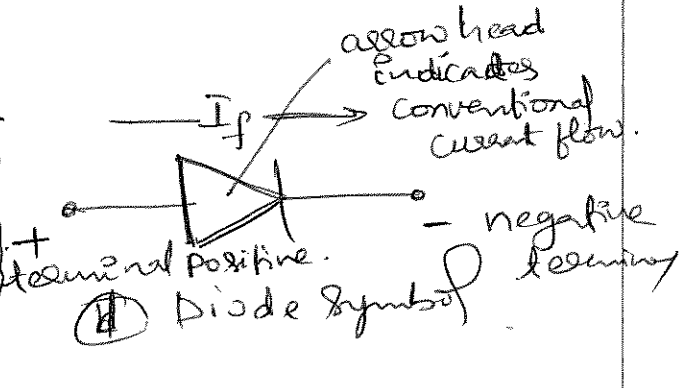
(b) Diffusion.



(c) Depletion region.



(e) p-n junction.



(d) Diode Symbol

Diode terminals :-

The device formed by the formation of the pn junction is called a diode. The diode has two terminals. They are Anode, Cathode.

A p-type material is called anode. & n-type is called Cathode.

Biasing of pn junction Diode

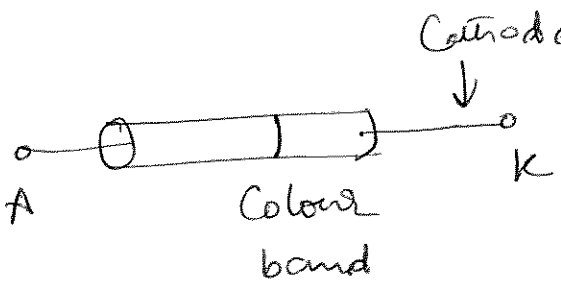
- Applying external D.C voltage to any electronic device is called biasing.
- p-n junction allows current flow only in one direction, under biased condition.
- Depending upon the polarity of the d.c voltage externally applied to it, the biasing is classified as Forward biasing & Reverse biasing.

Explain the Types of Diodes.

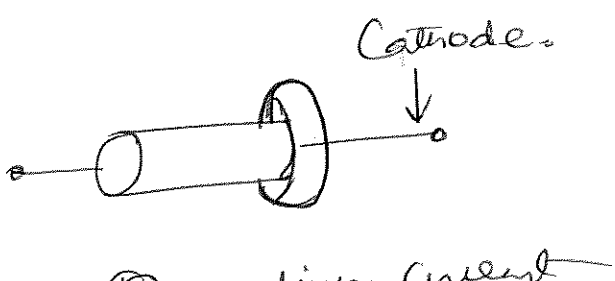
The diodes classified based on

(1) Forward current carrying capacity
(2) Reverse voltage withstanding capacity.

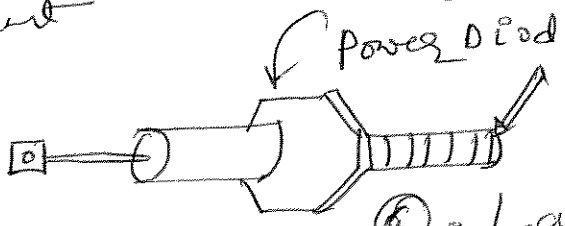
Sl.no.	Diode	Forward current Capacity	Reverse voltage Capacity.
1.	Low current	upto 100mA	upto 75V
2.	medium Current	upto 400mA	upto 200V
3.	large current	Few amperes	several 100volts.



(a) Low current



(b) medium current



(c). Large current.

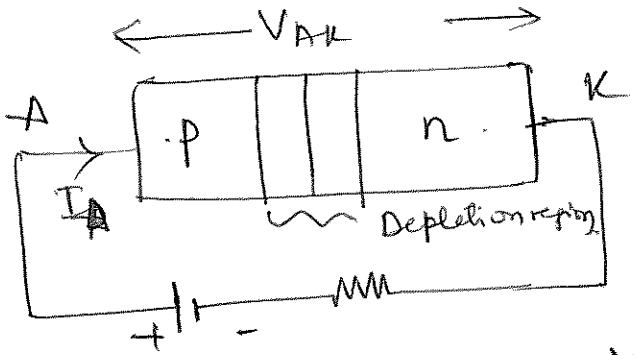
- Low and medium current diodes are connected in circuit by soldering their leads to the connecting terminal. The heat generated by these diodes is not very high & easily carried away by convection to the surroundings.

- The heat generated in case of high current diodes is very high and hence these diodes are stud mounted and provided with head sinks made of metals like copper or aluminium. The heat sinks provide large surface area so that heat can be easily transferred to the surroundings.

Characteristics and parameters.

Forward and Reverse characteristics :-

- If Anode (p-side) is connected to +ve terminal of external voltage source (battery) and cathode to negative terminal of external voltage source. Then Diode is said to be forward biased.



@ Diode under forward biased condition.

The holes of p type semiconductor move towards the junction. And the electrons in the n-type semiconductor are pushed towards the junction because of the external supply voltage. These movement of charge carriers contribute flow of current and diode is known as conducting.

- The width of depletion region decreases due to movement of majority charge carriers towards the junction.
- The minimum voltage required for the majority charge carriers to cross the junction is called barrier potential.

for Si diode barrier potential is 0.7 Volts.

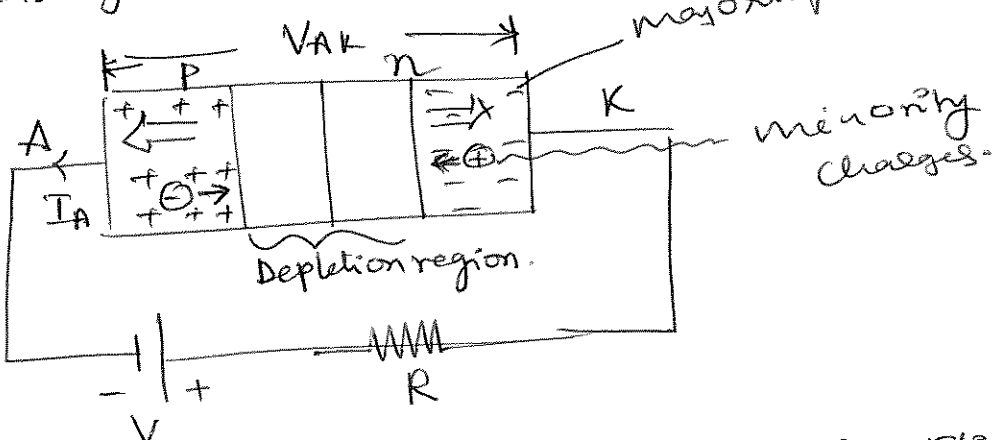
Ge diode " " is 0.3 Volts

- As voltage V_{AK} increases beyond barrier potential more number of charge carriers are pushed across junction & hence the current through the diode increases exponentially. as shown in V-I curve (1)

Reverse characteristics.

The diode is said to be reverse biased when the anode voltage is negative with respect to cathode. i,e Anode connected negative terminal of power supply & Cathode to positive terminal of the power supply.

V_{AK} is the voltage across the diode & I_A is the current through the diode.



(b) Diode under reverse biased Condition.

The majority charge carriers from both sides are pulled away from the junction. This is because of force exerted by the external voltage on the charge carriers.

Since majority charges moves away from junction they doesn't contribute to the flow of current & diode is said to be not Conducting.

- Even though the small number of minority charge carriers are pushed towards the pn-junction by the external voltage.

The movement of minority charges results in the current through the diode.

Since the minority charges are small in number, the current through the diode is very small & is called reverse saturation current.

Since current is small, it is neglected and the diode is said to be in OFF Condition.

- The variation of current is known below. reverse biasing increases the depletion region width. when a reverse voltage increases beyond specific value, the pn junction breaks down & current decrease drastically (or increases in reverse direction).

The reverse voltage at which the p-n junction breaks down is called reverse breakdown voltage or peak Inverse voltage. (PIV).

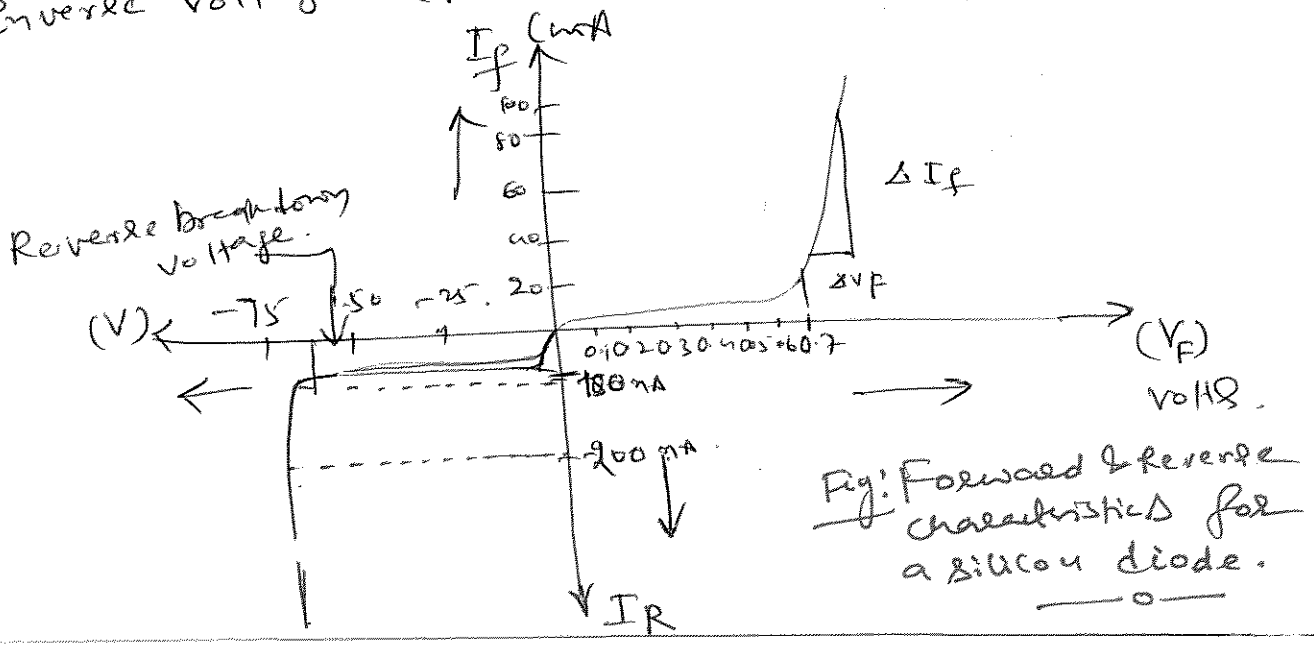
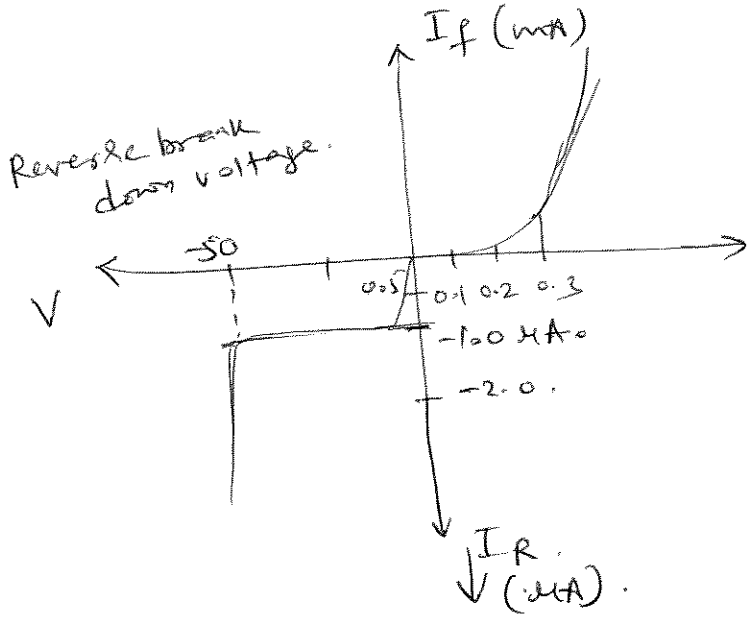


Fig: Forward & reverse characteristics for a silicon diode.



Typical forward & Reverse Characteristics curve for germanium Diode.

Diode parameters :- >

① **Barrier potential** :- It is defined as the minimum voltage under the forward biased condition, at which the diode starts conducting. It is also called cut-in voltage or knee voltage.

② **Forward voltage drop (V_F)**. It is defined as the voltage drop across the diode, when the diode is forward biased. The typical value $V_F = 0.7$ V silicon, $V_F = 0.3$ V germanium.

③ **Forward Resistance (R_f)**.
It is defined as the resistance of the diode when the diode is forward biased. For ideal diode $R_f = 0\,\Omega$. For pratical diode R_f = few ohms (very low).

④ **Reverse saturation current**
It is defined as the current through the diode when the diode is under the reverse biased condition.

- **Peak Inverse voltage (PIV)** – It is defined as the reverse voltage at which the p-n junction breaks down & the diode starts conducting heavily. Once p-n junction breaks down, the device gets damaged.
It is called as PIV rating of Diode.

Diode Equations / Relationship

The diode relationship refers to diode current & its dependance on the voltage across diode.

The relationship between diode current & diode voltage is called diode current equation.

The equation is.

$$I = I_0\left[e^{\frac{V}{\eta V_T}} - 1\right]$$

Where:

$I \rightarrow$ current flowing through the diode.

$I_0 \rightarrow$ reverse saturation current of the diode.

$V \rightarrow$ voltage applied across the diode.

$V = +ve$ for forward biasing

$V = -ve$ for reverse biasing.

$\eta \rightarrow$ Constant. it value $\eta = 1$ or 2.

V_T = voltage equivalent of Temperature.

$= \frac{KT}{q}$ where $K \rightarrow$ Boltzman Constant.

$= 1.38 \times 10^{-23}$ J/K.

$T \rightarrow$ Temperature in °K.

$T = 273 +$ temperature in °C.

q — magnitude of elatronic charge $= 1.6 \times 10^{-19}$ Columbs.

$$V_T = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}} * (273 + t°C) = (8.625 \times 10^{-5})(273 + t°C)$$

$$\boxed{V_T = \frac{273 + t°C}{11,600}}$$

for $t°C = 27$ $V_T = 0.026$

$$\boxed{V_T = 26 \text{ mV at } 27°}$$

Nature of V-I characteristics from Equation of Diode

Consider a diode equation

$$I = I_0\left(e^{V/\eta V_T} - 1\right).$$

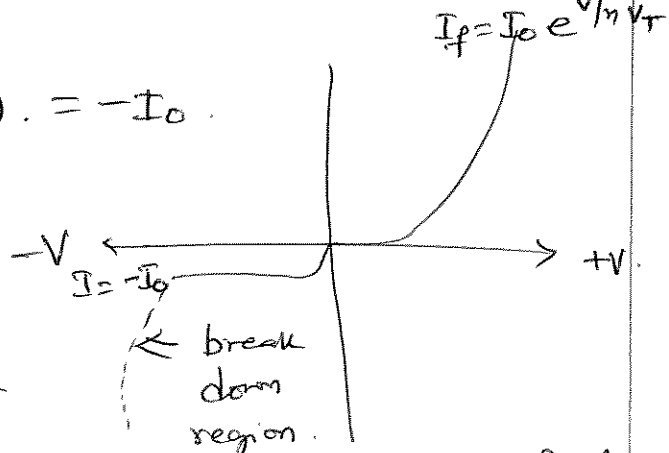
Now for a forward biased condition, the bias voltage V is considered positive & hence exponational index has positive sign. Due to this $1 << e^{V/\eta V_T}$. hence neglecting 1.

$$I_f = I_0 e^{V/\eta V_T}$$

It shows that once bias voltage exceeds cut-in voltage, the forward current increases exponationally.

In reverse biased condition, the bias voltage V is treated negative & due to this exponential index has negative sign. so $e^{-V/\eta V_T} << 1$. hence neglecting exponential term. we get

$$I_R = I_0(-1). = -I_0$$



V-I characteristics of p-n junction Diode

(1). A silicon diode operates at low values of current. The diode is under forward biased condition. The reverse saturation current of diode is 10nA. The voltage across the diode is 0.5V. Find the current through the diode

given:- $I_0 = 10nA$ $V = 0.5V$ $t = 25^\circ C$ $\eta = 2$ (Si diode at low currents)

$$V_T = \frac{t^\circ + 273}{11600} = 25.68 \times 10^{-3} V$$
$$= 0.02568 V$$

Find $I = ?$

$$I = I_0 \left[e^{V/\eta V_T} - 1 \right]$$
$$= 10 \times 10^{-9} \left[e^{\frac{0.5}{2(0.02568)}} - 1 \right]$$
$$= 0.169 \times 10^{-3} A = 0.169 mA$$

(2). A germanium diode operates at room temperature of 22°C with a forward current of 40mA. The forward voltage across diode is 0.25V. Find the reverse saturation current of the diode.

given. $t = 22°C$.

$I = 40 \times 10^{-3} A$. for germanium diode $\eta = 1$.

$V = 0.25V$.

$I_0 = ?$

$$I = I_0 \left[e^{V/\eta V_T} - 1 \right]$$

$$V_T = \frac{273+22}{11600} = 0.025$$

$$I_0 = \frac{I}{e^{V/\eta V_T} - 1} = \frac{40 \times 10^{-3}}{\left[e^{0.25/0.025} - 1 \right]}$$

$$= \frac{40 \times 10^{-3}}{22025} =$$

$$\boxed{I_0 = 1.816 \approx 182\ \mu A}$$

(3) In an application the germanium diode carries a current of 57mA under forward biased condition. The diode operates at a temperature of 100°C. The reverse saturation current of the diode is 5μA. Find the voltage across the diode.

given:- $\eta = 1$ (ge) $t = 100°C$

$I_0 = 5\mu A$.

$I = 57\mu A = 0.057A$.

$V = ?$

$$V_T = \frac{273+100}{11600} = 0.032$$

$$I = I_0 \left[e^{\frac{V}{\eta V_T}} - 1 \right]$$

$$\frac{I}{I_0} = \left[e^{\frac{V}{\eta V_T}} - 1 \right]$$

$$\frac{I}{I_0} + 1 = e^{\frac{V}{\eta V_T}}$$

$$\log_e \left[\frac{I}{I_0} + 1 \right] = \frac{V}{\eta V_T}$$

$$\log_e \left[\frac{0.057}{5 \times 10^{-6}} + 1 \right] = \frac{V}{0.032}$$

$$\ln \left[11,401 \right] = \frac{V}{0.032}$$

$$\boxed{V = 0.299V}$$

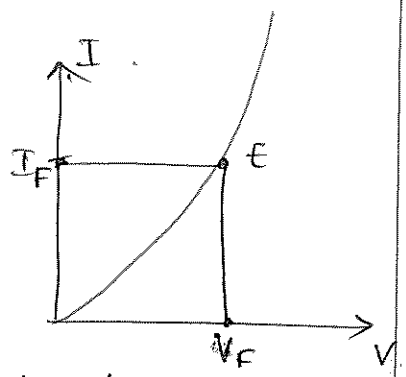
Static and Dynamic resistance.

Static resistance:-

It is also called as DC resistance is defined as a ratio of DC voltage across the diode to the resulting DC forward current through it.

$$R_{dc} = \frac{\text{forward DC voltage}}{\text{forward DC current}} \text{ in } \Omega = \frac{V_F}{I_F}$$

R_{dc} – Varies from 40Ω – 70Ω.



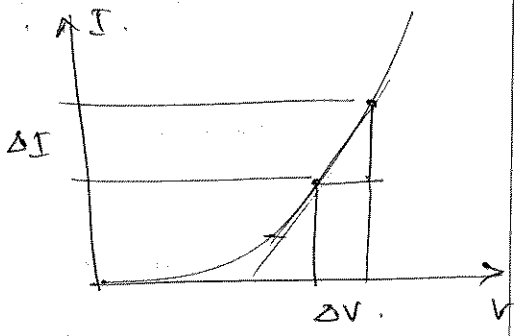
Dynamic forward resistance

When an alternating voltage is applied to diode, then the resistance offered by the diode under forward bias is called dynamic or AC forward resistance

It is defined as ratio of change in forward AC voltage to the change in diode current.

$$R_d = \frac{\Delta V}{\Delta I} = \frac{1}{\text{slope of tangent}}$$

$$\text{slope of tangent} = \frac{\Delta I}{\Delta V}$$



W.K.T the current through the diode is given by

$$I = I_0 \left[e^{\frac{V}{\eta V_T}} - 1 \right]$$

$$I = I_0 e^{V/\eta V_T} \rightarrow (2)$$

$e^{V/\eta V_T}$ is very large

Differentiating eqn (2) with respect to V.

$$\frac{dI}{dV} = \frac{d}{dV}\left\{ I_0 e^{\frac{V}{\eta V_T}} \right\} = I_0 \frac{d}{dV}\left\{ e^{\frac{V}{\eta V_T}} \right\}$$

$$\frac{dI}{dV} = I_0 e^{V/\eta V_T} \cdot \frac{1}{\eta V_T}$$

$$\frac{dI}{dV} = I \cdot \frac{1}{\eta V_T}$$

$$\frac{dV}{dI} = \frac{\eta V_T}{I} \longrightarrow (3).$$

$\eta = 1$ and temperature $t = 27^\circ C$.

$$V_T = \frac{t^\circ C + 273}{11600} = \frac{300K}{11600} = 0.026.$$

$$\boxed{r_d = \frac{0.026}{I} = \frac{26mV}{I_F}}$$

* A silicon diode operates at low values of current. The diode is under forward biased condition. The reverse saturation current of the diode is 10nA. The voltage across the diode is 0.5V. Find the current through the diode, Static & dynamic resistance of the diode.

Consider $t^\circ = 25^\circ C$.

given Data :- $I_0 = 10\,nA$. $I = ?$

$V = 0.5V$.

$\eta = 2$ (Si. diode at low currents).

$$V_T = \frac{t^\circ C + 273}{11600}$$

$$= \frac{25 + 273}{11600}$$

$$= 0.0256.$$

$$I = I_0 \left[e^{V/\eta V_0} - 1 \right)$$

$$= 10 \times 10^{-9} \left[e^{\frac{0.5}{2 \times 0.0256}} - 1 \right]$$

$$= 10 \times 10^{-9} \left[e^{9.765} - 1 \right]$$

$$= 1.743 * 10^{-4}.$$

$$\boxed{I = 0.1743\,mA} \simeq 0.17\,mA.$$

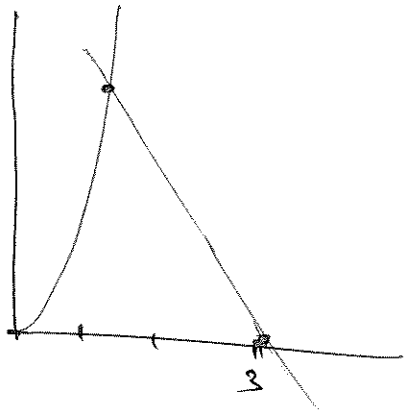
Static resistance $R_f = \frac{V}{I} = \frac{0.5}{0.17m} = 2.9\,K\Omega$

Dynamic resistance $r_d = \frac{0.026}{I} = 0.15K\Omega$.

$V_f = V_{in} - I_f R_L$

$I_f = 25mA \quad I_Q = 25mA.$

$I_f = 0 \quad V_f = V_{in} = 3V.$ is point B.



$Slope = \frac{\Delta I_f}{\Delta V_f}.$

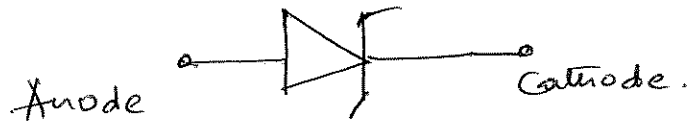
$\Delta I_f = 10mA \quad \Delta V_f = 0.9V.$

$Slope = \frac{10 \times 10^{-3}}{0.9} = 0.0111$

$R_L = \frac{1}{Slope} = 90\Omega.$

Zener Diode:-

Zener Diodes are constructed by heavily doped N & P type semiconductors. The symbol shown below.



(a) Zener diode

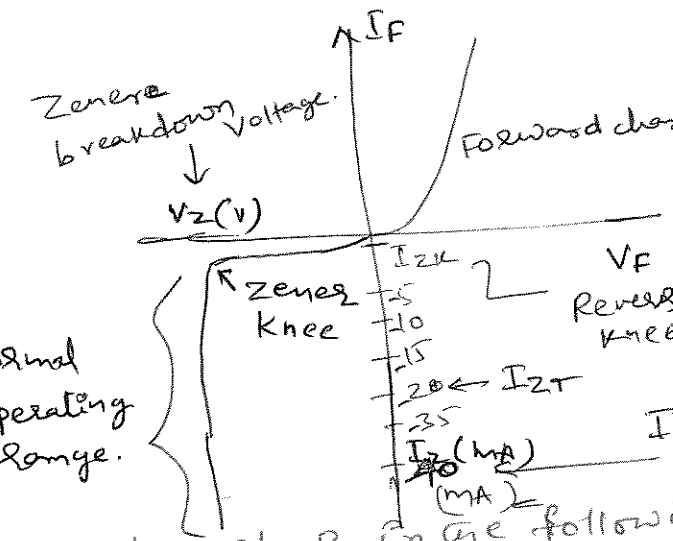
Operation:-

- In the forward bias direction, the zener diode behaves like an ordinary diode
- In Reverse bias Condition, no current flows unhill the breakdown voltage is reached.
- The zener diode undergoes a process of breakdown when the reverse voltage increase to a speific value called zener voltage, then diode starts conducting simultaneously current increases in zener diode.
- After breakdown, the voltage across the zener diode will remain constant & the current controlled by external resistance.

Breakdown voltage of zener 1.4 to 200V
power rating from 1W to 50W

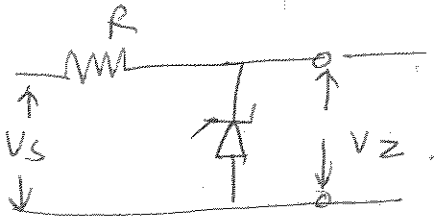
V_Z depends on Doping.

V - I characteristics of zener diode



I_{ZT} - Test current for measuring the V_Z

① Find the value of R in the following ckt with zener diode of voltage rating of 4.7 V. The power rating of zener diode is 400 mW. $V_S = V_{in} = 12$ V.



given:- $V_Z = 4.7$ V $P_Z = 400$mW

$V_S = 12$ V.

find. $R_S = ?$

$$P_Z = V_Z I_Z$$

$$I_Z = \frac{P_Z}{V_Z} = \frac{400\,m}{4.7} = 85\,mA.$$

To Find R. apply ohm's law.

$$R = \frac{V_S - V_Z}{I_Z} = \frac{12 - 4.7}{85 \times 10^{-3}} = 85.8\,\Omega \approx 85\,\Omega.$$

② A zener diode has voltage rating of 5V, & the current rating of 20 mA. Find the static resistance of the zener diode. If the voltage across the zener diode changes by 0.5V, the current through the zener diode is found to vary by 10 mA. Find the dynamic resistance of the zener diode.

given $V_Z = 5$ V $I_Z = 20$m. change in $V_Z = 0.5$ V

change in $I_Z = 10$mA.

$$\text{Static resistance} = \frac{V_Z}{I_Z} = \frac{5}{20 \times 10^{-3}} = 250\,\Omega.$$

$$\text{dynamic resistance } r_d = \frac{\text{change in } V_Z}{\text{change in } I_Z} = \frac{0.5}{10\,m} = 50\,\Omega$$

Zener diode as a Voltage regulator

Voltage regulators are the devices used to maintain constant voltage across a load despite of fluctuations in the input voltage and load currents.

The zener diode in its reverse bias region is widely used as a voltage regulator as it continuous to operate till the magnitude of current becomes less than $I_{Z(min)}$.

The typical voltage regulator is shown in figure (1).

The zener diode of breakdown voltage V_Z is connected to the supply voltage in reverse direction.

For all the values of current within the breakdown region the voltage across the diode will remain fixed at V_Z, giving a constant supply across its load.

The resistance R_S controls the current flowing in the circuit.

Case (i). When no load is connected ($I_L = 0$).

When there is no load resistance R_L, then $I_L = 0$. The current flowing in the circuit entirely passes through zener diode.

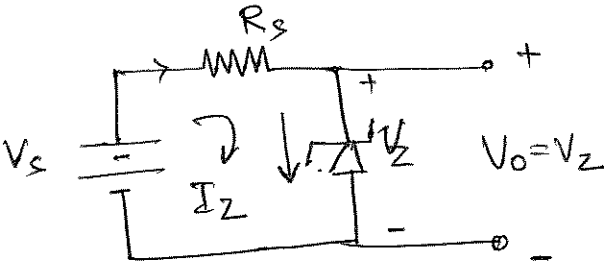
The diode dissipates maximum power. Series resistor is selected carefully to maintain the power dissipation with in the range of maximum power dissipating capability of the diode.

Apply KVL to the circuit.

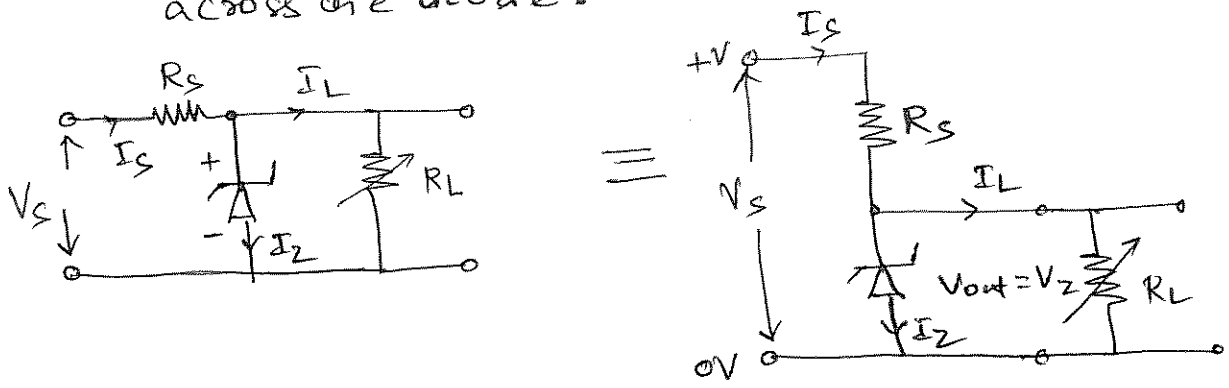
$$V_S - I_Z R_S - V_Z = 0.$$

The current I_Z flowing in the Resistor is given by

$$I_Z = \frac{V_S - V_Z}{R_S}, \quad R_S = \frac{V_S - V_Z}{I_Z}.$$



Case ②. When load resistance R_L is connected across the diode.



Zener diode as a voltage regulator.

Here, since the load is parallel to zener diode, the output voltage will be equal to V_Z.

The zener current must always be above $I_{Z(min)}$ [current for which the stabilization of voltage is effective].

The higher limit of current allowed to flow in the circuit depends upon the power dissipating capability of the components used.

Apply KVL to the above circuit.

$$I_Z + I_L = \frac{V_S - V_Z}{R_S}$$

$$I_S = I_Z + I_L$$

The voltage regulation can be done through two techniques.

1 line regulation.

2. Load regulation.

Line Regulation :- In this case, series resistance and load resistance are kept constant and it is assumed that all the variations in voltage arise due to fluctuations in input power supply.

The regulated output voltage is achieved for input voltage above certain minimum level. The percentage of regulation is given by

$$\frac{\Delta V_o}{\Delta V_{IN}} \times 100$$

where V_o is the output voltage, V_{IN} is the input voltage, and ΔV_o is the change in output voltage for a particular change in input voltage ΔV_{IN}.

2. Load Regulation :-

Here, the input voltage is fixed while the load resistance is varied. The constant output voltage is obtained as long as the load resistance is maintained above a minimum value. The percentage of regulation is given by.

$$\left(\frac{V_{NL} - V_{FL}}{V_{NL}}\right) \times 100$$

where V_{NL} is the voltage across the zener diode when no load is applied ($R_L = 0$).

V_{FL} Full Load voltage across the zener diode when R_L value is maximum.

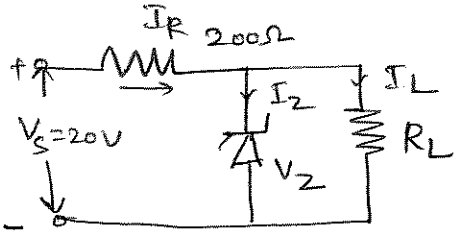
3. Series resistance Also varies, & it is given by

$$R_{min} = \frac{V_{i(min)} - V_Z}{I_{L(max)} + I_{Z(min)}}$$

$$R_{max} = \frac{V_{i(max)} - V_Z}{I_{L(min)} + I_{Z(max)}}.$$

$$R_{min} < R < R_{max}.$$

The circuit of figure has a zener diode connected across the load.



(a) For $R_L = 180\Omega$, determine all currents and voltages

(b). Repeat part (a) for $R_L = 450\Omega$

(c). Find the value of R_L for the zener to draw maximum power

$V_Z = 10V$, $R_Z = 0$.

$P_{Z(max)} = 350mW$

(d). Find the minimum value of R_L for the zener to be just in on-state.

Solution:-

(a). as R_L is small, Assume zener diode not conduct i.e $I_Z = 0$.

$$I_R = I_Z + I_L = \frac{V_S - V_Z}{R_S + R_L}.$$

$$I_R = I_Z = \frac{20 - 0}{200 + 180} = 52.6\,mA.$$

$$V_Z = V_L = V_S - I_R * R_S = 20 - (52.6 \times m \times 200) = 9.48 < 10V.$$

(b). $R_L = 450\Omega$.

Assume it at the zener conducts.

$$V_L = V_Z = 10V$$

$$I_L = \frac{V_Z}{R_L} = 0.0222 = 22.2mA.$$

$$I_R = \frac{V_S - V_Z}{R_S} = \frac{20-10}{200} = 50mA, \quad I_Z = I_R - I_L = 27.8\,mA.$$

$$P_Z = I_Z * V_Z = 27.8m * 10 = 278\,mW \leq 350mW \text{ rating}$$

(c). when zener draws maximum power

$$I_Z = \frac{P_Z}{V_Z} = \frac{350m}{10} = 35mA. \qquad I_R = \frac{V_S - V_Z}{R_S} = \frac{20-10}{200} = 50mA$$

$$I_L = I_R - I_Z = 50 - 35 = 15mA. \qquad R_L = \frac{V_Z}{I_L} = \frac{10}{15m} = 667\Omega.$$

(d). $I_Z = 0$ (just on state)

$I_R = 50mA = I_L$

$V_L = V_Z = 10V$ $\qquad R_{L(min)} = \frac{V_O}{I_R} = \frac{10}{50m} = 200\Omega.$

(1) Design a zener diode voltage Regulator to meet the following specifications.

Unregulated dc output voltage $V_i = 8-12\,V$.

Regulated dc output voltage $V_o = 5\,V$.

minimum zener current ; $I_{zmin} = 5\,mA$

maximum zener current , $I_{zmax} = 80\,mA$

Load current : $0-20\,mA$.

Given Data :-

$V_{imin} = 8\,V$ $V_{imax} = 12\,V$ $V_o = 5\,V$.

$I_{Lmin} = 0\,mA$ $I_{Lmax} = 20\,mA$. $I_{zmin} = 5\,mA$

$I_{zmax} = 80\,mA$. $V_z = 5\,V$. $= V_o$.

Select a zener diode with a reverse breakdown voltage of 5V.

$$R_L = \frac{V_z}{I_L} = \frac{V_o}{I_{Lmax}} = \frac{5V}{20mA}.$$

$$\boxed{R_{Lmin} = 250\,\Omega}$$

$$\frac{V_{imin} - V_z}{I_{zmin} + I_{Lmax}} > R$$

$$\frac{8-5}{5mA + 20mA} > R.$$

$$120 > R.$$

$$\boxed{R < 120\,\Omega} \longrightarrow (1)$$

$$\frac{V_{imax} - V_z}{I_{zmax} + I_{Lmin}} \leq R$$

$$= \frac{12-5}{(80mA + 0)} < R. \qquad \boxed{R > 87.5\,\Omega} \longrightarrow (2)$$

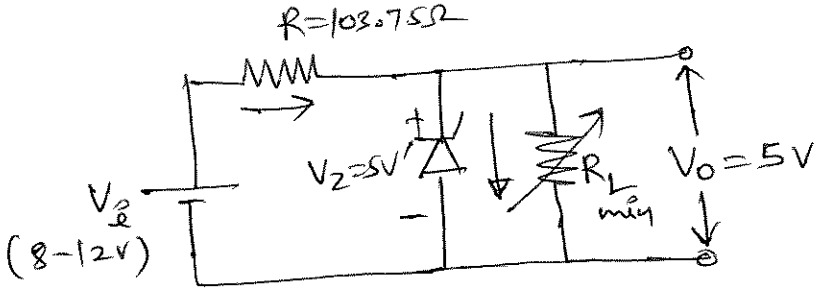
Combining the results of eqn ① & ②

$$87.5\Omega \leq R < 120\Omega$$

Let us take average.

$$R = \frac{87.5 + 120}{2}$$

$$R = 103.75\Omega$$



$R_{L\,min} = 250\Omega$.

Zener diode voltage regulator.

② Design a zener diode voltage regulator to meet the following requirements.

Unregulated dc input voltage V_i = 13 – 17V.

load current, I_L = 10mA.

Regulated output voltage V_o = 10V.

minimum zener current = $I_{Z\,min}$ = 5mA.

maximum power dissipation in zener $P_{Z\,max}$ = 500mW.

given: $V_{i\,min}$ = 13V.

$V_{i\,max}$ = 17V.

$I_L = I_{L\,max}$ = 10mA

$I_{L\,min}$ = 0 (not given)

V_o = 10V

$I_{Z\,min}$ = 5mA.

$$P_{Zmax} = P_D = V_Z I_{Zmax}.$$

$$I_{Zmax} = \frac{P_D}{V_Z} = \frac{500 \times 10^{-3}}{10} = 50\,mA.$$

$$\frac{V_{imin} - V_o}{I_{Zmin} + I_{Lmax}} > R.$$

$$\frac{13 - 10}{5m + 10mA} \geq R$$

$$200 > R$$

$$\boxed{R \leq 200\,\Omega}$$

$$\frac{V_{imax} - V_o}{I_{Zmax} + I_{Lmin}} < R.$$

$$\frac{17 - 10}{50m + 0} < R$$

$$140 < R$$

$$\boxed{R > 140\,\Omega}$$

Jhen $$R = \frac{140 + 200}{2} = 170\,\Omega.$$

$$R_L = \frac{V_o}{I_L}$$

$$R_{Lmin} = \frac{V_o}{I_{Lmax}} = \frac{10}{10 \times 10^{-3}} = 1000\,\Omega.$$

$$\boxed{R_{Lmin} = 1000\,\Omega}$$

① . A 9V reference source is to be designed using a series connected zener diode and a resistor connected to a 30V supply. Select suitable components and calculates the circuit current when supply voltage drops to 27V choose $I_Z = 20mV$.

Given data:- $V_S = 30V$. $\quad R_S = \frac{V_S - V_Z}{I_Z}$

$$R_S = \frac{30 - 9.1}{20mA}$$

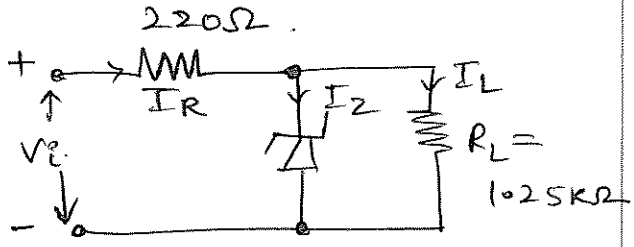
$$= 1.05K\Omega$$

$$P = (I_Z)^2 * R_S = (20\times10^{-3})^2 * 1K\Omega$$

$$= 0.4W.$$

when $V_S = 27V$, $\quad I_Z = \frac{V_S - V_Z}{R_S} = \frac{27 - 9.1}{1K\Omega} = 17.9mA.$

② Determine the range of V_i in which zener diode of figure conducts.



$V_Z = 20V$

$P_Z(max) = 1200mW$

(i) V_Z just in Conducting state.

$V_Z = 20V$, $I_Z = 0$.

$$I_R = I_L = \frac{20}{1.25K} = \frac{V_Z}{R_L} = 16mA.$$

$$V_i = 20 + (220 \times 16\times10^{-3}) = 23.52V.$$

$$= V_Z + (I_R * R)$$

(b). $\quad I_Z = I_{Z(max)} = \frac{P_{Z(max)}}{V_Z} = \frac{1200m}{20} = 60mA.$

$I_L = 16mA.$

$I_R = I_Z + I_R = 76mA.$

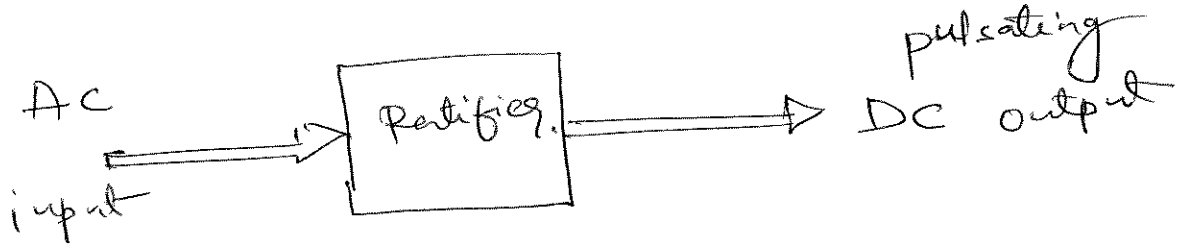
$$V_i = V_Z + (R * I_{R\,max})$$

$$= 20 + (220 * 76mA) = 36.72V.$$

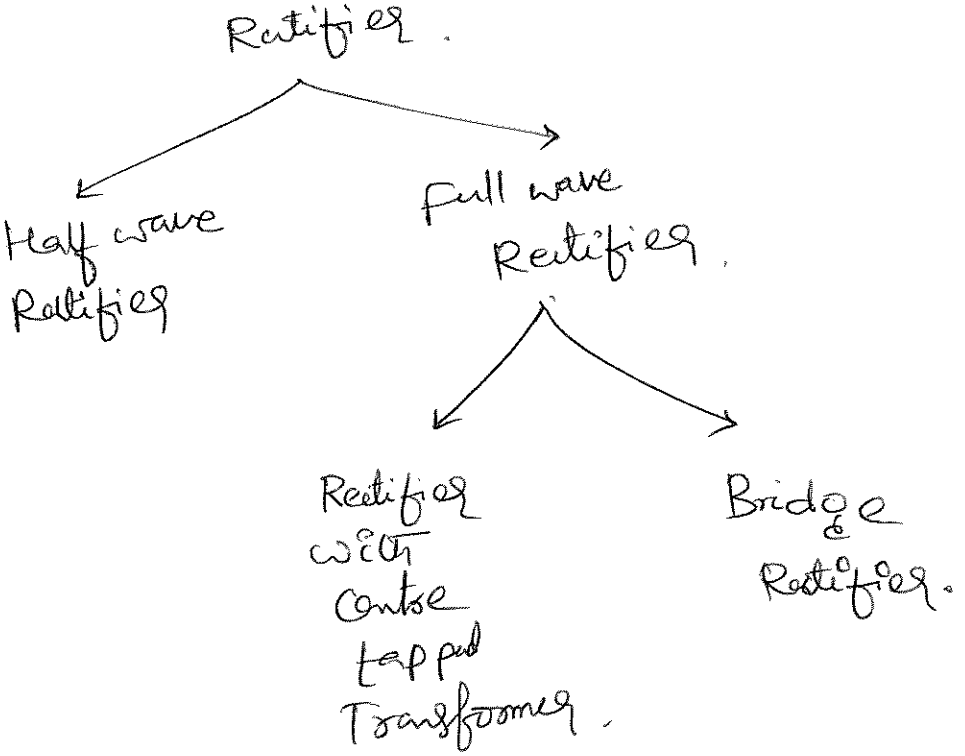
For input voltage from 23.52V to 36.72V, V_L will remain constant at 20V.

Rectifiers.

A rectifier is defined as an electronic circuit that converts alternating current (AC), which periodically reverses direction into a direct current (DC) which flows in only one direction. This process is known as rectification.

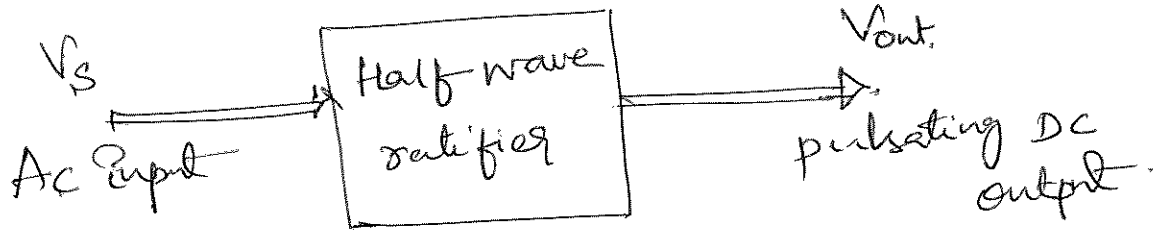


Classification of rectifier.



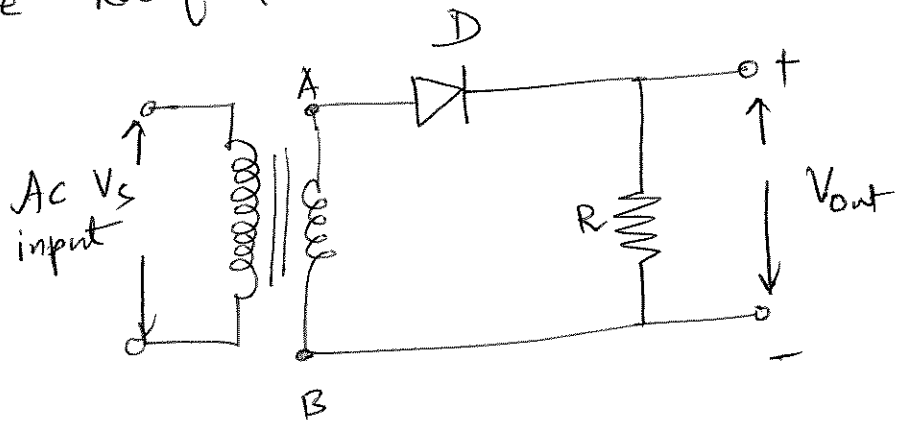
Half wave Rectifier :—

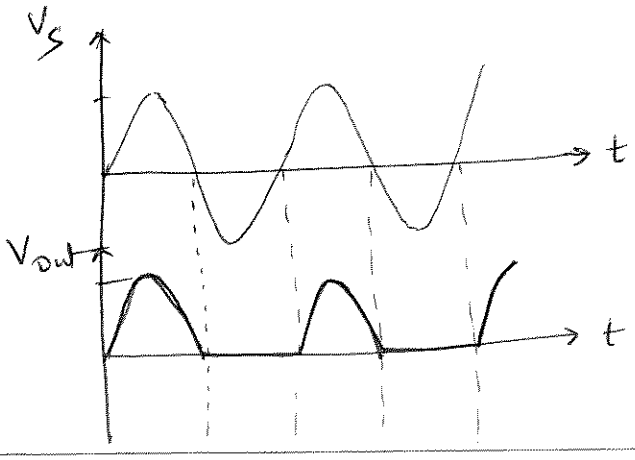
Half wave rectifier is a circuit which provides an output only during one half cycle of the input and zero output for the other half cycle.



The half wave rectifier using one diode is shown below.

The transformer is used to either step-up or step down, the ac input voltages. A diode in series with the transfomer and load is used in half wave Rectifier.



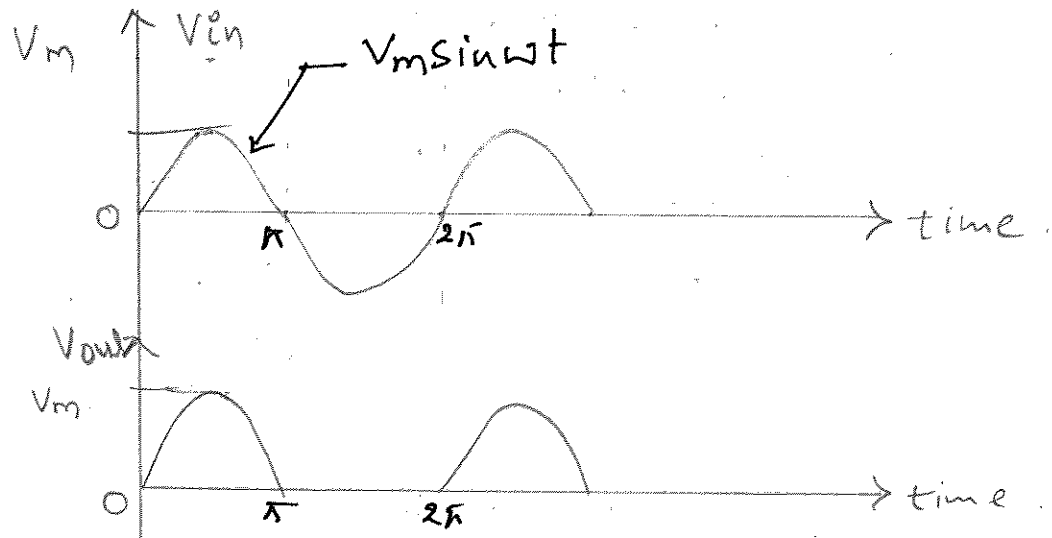


Working. During positive half cycle of the input signal (a c), the Diode Anode terminal becomes positive with respect to the other end. The Diode D is forward biased and acts as short circuit, Thus current flows in the circuit.

$$V_D = I_L R_L$$

During negative half cycle of the AC input. The diode Anode terminal becomes negative with respect to end B. The diode D is reverse biased and acts as open circuit thus no current flows.

$$V_D = 0 \text{ volt.}$$



Analysis of half wave rectifier

we use peformane paramter.

- DC output voltage. (V_{DC})
- RMS output voltage (V_{rms})
- Ripple factor (γ)
- Efficiency: (η)
- DC output ureant (I_{dc})
- Rms output ureant (I_{rms})
- peak Inverse voltage. (PIV).
- ac power (P_{ac})
- DC power (P_{DC})

To find an expression for dc output voltage

Dc output voltage is also known as the average value of the output voltage.

$$V_{DC} = \frac{\text{area under one cycle}}{\text{period of one cycle}}$$

$$\begin{cases} V_o = V_m \sin\omega t & \text{for } 0 \text{ to } \pi \\ V_o = 0 & \text{for } \pi \text{ to } 2\pi \end{cases}$$

V_{DC} is defined as the ratio of area enclosed under one cycle of the output waveform to the period of one cycle.

$$V_{DC} = \frac{\text{area under one cycle}}{\text{period of one cycle}}$$

$$V_{DC} = \frac{\int_0^{2\pi} V_o \, d\omega t}{2\pi} = \frac{\int_0^{\pi} V_m \sin\omega t \cdot d\omega t}{2\pi}$$

$$= \left[\frac{-V_m \cos\omega t}{2\pi} \right]_0^{\pi}$$

$$V_{DC} = \frac{V_m}{2\pi} \left[-\cos\pi + \cos 0 \right]$$

$$= \frac{V_m}{2\pi} \left[-(-1) + 1 \right] = \frac{2V_m}{2\pi} = \frac{V_m}{\pi}$$

$$\boxed{V_{DC} = \frac{V_m}{\pi}} = \boxed{V_{av} = \frac{V_m}{\pi}}$$

Similarly.

$$I_{DC} = \frac{I_m}{\pi} \text{ or } I_{av} = \frac{I_m}{\pi}$$

$$I_{DC} = \frac{V_{dc}}{R_L} = \frac{V_m}{\pi} * \frac{1}{R_L} = \frac{1}{\pi} \frac{I_m}{R_L} * R_L = \frac{I_m}{\pi}$$

To find an expression for RMS output voltage.

The rms voltage is also called effective voltage. It is found as square root of the ratio of area enclosed under one cycle of the squared output waveform to the period.

Here one cycle is from 0 to 2π.

$$V_{rms} = \sqrt{\frac{\int_0^{2\pi} V_o^2 \cdot d\omega t}{2\pi}} = \sqrt{\frac{\int_0^{\pi} V_o^2 \, d\omega t}{2\pi}}$$

(root mean square)

$$V_{rms} = \sqrt{\frac{\int_0^{\pi} V_m^2 \sin^2 \omega t \cdot d\omega t}{2\pi}} = \sqrt{\frac{V_m^2}{2\pi}} \sqrt{\int_0^{\pi} \left[\frac{1-\cos 2\omega t}{2}\right] d\omega t}$$

$$\sin^2 \omega t = \frac{1-\cos 2\theta}{2}$$

$$= \sqrt{\frac{V_m^2}{4\pi}} \sqrt{\left[\omega t - \frac{\sin 2\omega t}{2}\right]_0^{\pi}}$$

$$= \sqrt{\frac{V_m^2}{4\pi}} \sqrt{\pi - \frac{\sin 2\pi}{2}}$$

$$= \sqrt{\frac{V_m^2}{4\pi}} \cdot 2\sqrt{\pi}$$

$$\boxed{V_{rms} = \frac{V_m}{2}}$$

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m}{2R_L} = \frac{I_m R_L}{2 R_L} = \frac{I_m}{2}$$

$$P_{dc} = I_{dc}^2 * R_L$$

$$= \left(\frac{I_m}{\pi}\right)^2 * R_L = \frac{I_m^2}{\pi^2} * R_L$$

$$P_{dc} = \frac{1}{\pi^2} \frac{V_m^2}{R_L^2} * R_L$$

$$= \frac{V_m^2}{\pi^2 R_L}.$$

$$P_{ac} = I_{rms}^2 * R_L$$

$$= \left(\frac{I_m}{2}\right)^2 * R_L = \frac{1}{4} * \frac{V_m^2}{R_L^2} * R_L = \frac{V_m^2}{4R_L}.$$

① Ripple factor.

It is defined as the measure of ac component in the output of the rectifier.

$$\text{Ripple factor} = \gamma = \frac{\text{rms Value of ac Component.}}{\text{dc Component of output}}$$

V_{ac} → rms value of ac component in the rectifier output.

V_{DC} → is the DC value of Rectifier output.

V_{rms} → rms value of the Combined waveforms.

$$\text{The } V_{rms} = \sqrt{V_{ac}^2 + V_{dc}^2}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\gamma = \frac{V_{ac}}{V_{dc}} = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}}$$

$$= \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

let $V_{rms} = \frac{V_m}{2}$ $\quad V_{dc} = \frac{V_m}{\pi}$

$$= \sqrt{\left(\frac{\frac{V_m}{2}}{\frac{V_m}{\pi}}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$$

$$\boxed{\gamma = 1.21} \quad \text{i.e. } 121\%$$

Efficiency :-

Efficiency is defined as the ratio of dc power delivered to the load to the total input power to the rectifier.

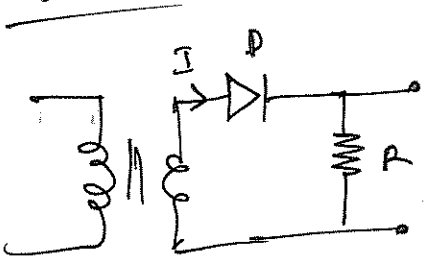
$$\eta = \frac{\text{dc output power.}}{\text{Total input power.}}$$

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{\frac{V_m^2}{\pi^2 * R_L}}{\frac{V_m^2}{4R_L}} = \frac{4}{\pi^2} = 40.5\%$$

$$\boxed{\eta = 0.405}$$

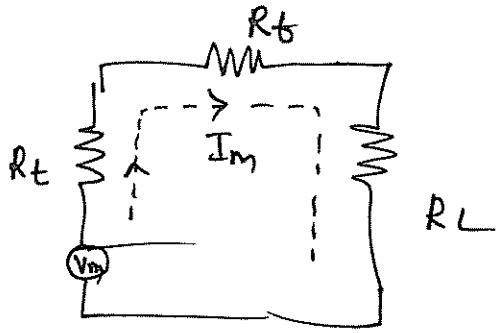
OR

Equivalent circuit of Half wave rectifier



Half wave rectifier.

$\equiv$



Equivalent circuit of Half wave rectifier

From circuit.

$$P_{dc} = I_{dc}^2 R_L .$$

$$P_{ac} = I_{rms}^2 (R_f + R_t + R_L).$$

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_f + R_t + R_L)}$$

$$I_{dc} = \frac{I_m}{\pi}$$

$$I_{dc} = \frac{I_m}{2}$$

$$\eta = \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{I_m}{2}\right)^2 (R_f + R_t + R_L)}$$

$$\boxed{\eta = \frac{4}{\pi^2} \frac{R_L}{(R_f + R_t + R_L)}}$$

$R_f = 0$

$R_t = 0.$

$$= 0.405 . \frac{R_L}{R_L}$$

$$\boxed{\eta = 0.405.}$$

An half wave rectifier supplies power to a load of 500Ω. The input voltage to the circuit is 100V. (peak value). Find the rms & average value of the load current, rms & average value of the load voltage ripple factor, efficiency of rectifier. given forward resistance of the diode to be 10Ω.

given. Data :- $V_m = 100V$ $R_L = 500\Omega$ $R_f = 10\Omega$

$I_{DC} = ?$ $I_{rms} = ?$ $V_{DC} = ?$ $V_{rms} = ?$ Ripple factor = ?

$\eta = ?$

We know :- $I_m = \frac{V_m}{R_f + R_t + R_L} = \frac{100}{(10+0+500)} = 0.196\ A.$

$$I_{DC} = \frac{I_m}{\pi} = \frac{0.196}{\pi} = 0.062\ A$$

$$I_{rms} = \frac{I_m}{2} = \frac{0.196}{2} = 0.098\ A$$

$$V_{DC} = I_{DC} * R_L$$

$$= 0.062 * 500$$

$$= 31V.$$

$$V_{rms} = I_{rms} * R_L$$

$$= 0.098 * 500 = 49V.$$

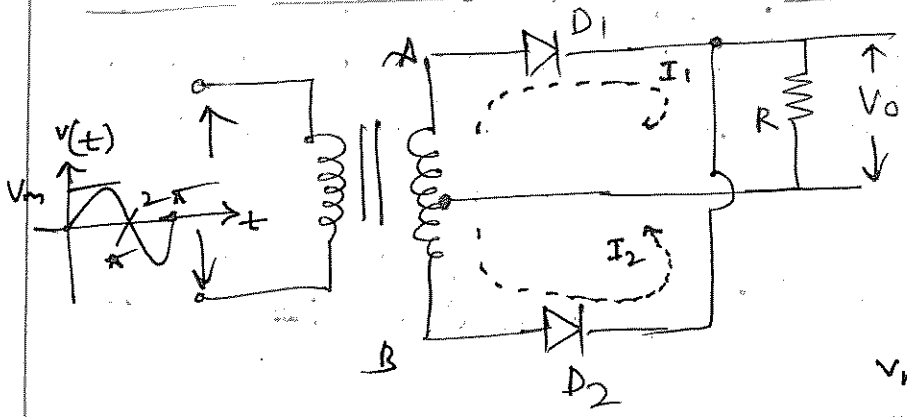
ripple factor = 1.21.

$$\text{Efficiency} = \eta = 0.405 \left(\frac{R_L}{R_f + R_t + R_L} \right)$$

$$= 0.405 \left(\frac{500}{10+0+500} \right) = 0.397$$

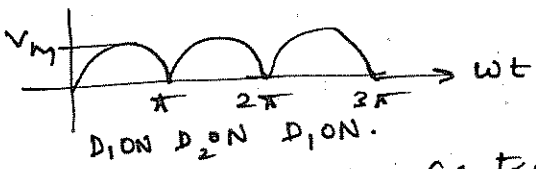
Full wave Rectifiers :-

Full wave rectifier with Centre tapped transformer.



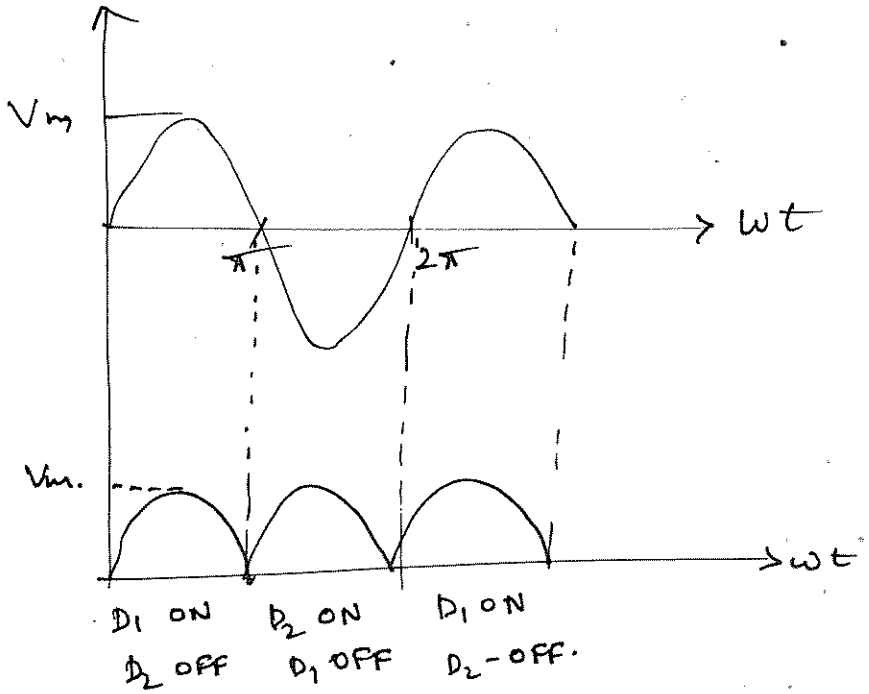
Current flows when D_1 Conducts

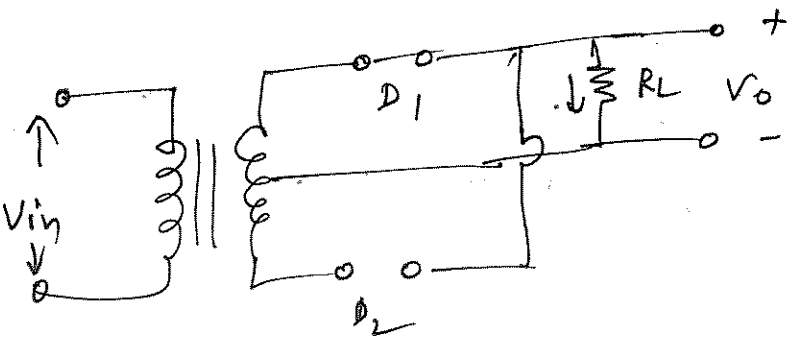
Current flows when D_2 conducts.



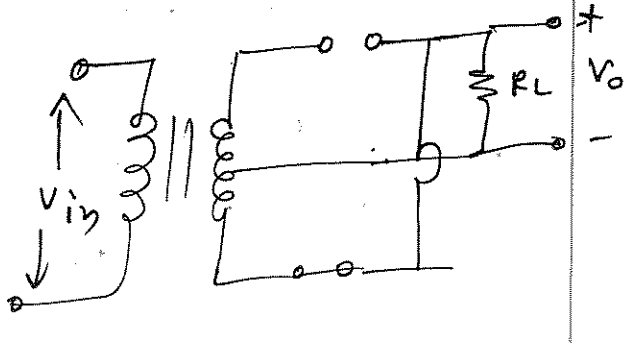
The full wave rectifier using two diodes and a Centre tapped transformer is shown in fig ①.

The Transformer is used to either step-up or step down the ac input voltage. Two diodes are connected on the secondary side of the Transformer as shown in fig ② along with the load.





(a) During +ve half cycle



(b) During negative cycle.

Operation:- During +ve half cycle of the ac input voltage end A becomes positive with respect to end B The diode D_1 is forward biased & conducts, diode D_2 is reverse biased and acts as open circuit and will not Conduct as shown fig(2).

Thus Diode D_1 supplies the load current. The Conventional current flow is through diode D_1, load resistor R_L.

During -ve half cycle of the AC input voltage end A becomes -ve with respect to end B, the diode D_2 is forward biased and conducts while diode D_1 is reverse biased and acts as open circuit and will not Conduct. The Diode D_2 supplies the load current the Conventional current is through diode D_2, Load resistor R_L.

Therefore for both the half cycles the current flows through load in the same direction. Hence we get two half cycles for one input signal.

Analysis of the full wave rectifier;-

The performance parameters are

(1) DC output Voltage
(2) RMS output Voltage
(2) Ripple factor
(4) Efficiency.

Dc output voltage;-

The dc output voltage can also be called the average Value of the output voltage.

The dc output voltage is defined as the ratio of area enclosed under one cycle of the output waveform. one cycle is from 0 to π.

let the output voltage of the rectifier be expressed as $V_o = V_m \sin\omega t$.

$$V_{DC} = \frac{\text{area under one cycle}}{\text{period of one cycle.}}$$

$$V_{DC} = \frac{\int_0^{\pi} V_o \cdot d\omega t}{\pi} = \frac{\int_0^{\pi} V_m \sin\omega t}{\pi}$$

$$V_{DC} = \left[-\frac{V_m \cos\omega t}{\pi} \right]_0^{\pi}$$

$$V_{DC} = \frac{V_m}{\pi} \cdot \left[-\cos\pi + \cos 0 \right]$$

$$= \frac{V_m}{\pi} \left[-(-1) + 1 \right] = \frac{2V_m}{\pi}.$$

$$\boxed{V_{DC} = \frac{2V_m}{\pi}}$$

Expression for RMS output voltage

RMS voltage is also called effective voltage. The RMS value of a continuous-time waveform is the square root of the arithmetic mean (average) of the squares of the original values.

. let the output of the rectifier is $V_o = V_m \sin\omega t$. The RMS output voltage is found as square root of the ratio of area enclosed under one cycle of the squared output waveform to the period of one cycle.

In above waveform, one cycle is from 0 to π.

$$V_{RMS} = \sqrt{\frac{\text{area enclosed under one cycle of the squared output waveform}}{\text{period of one cycle}}}$$

$$= \sqrt{\frac{\int_0^{\pi} V_o^2 \cdot d\omega t}{\pi}} = \sqrt{\frac{\int_0^{\pi} V_m^2 \sin^2 \omega t \cdot d\omega t}{\pi}}$$

$$= \sqrt{\frac{V_m^2}{\pi}} \sqrt{\int_0^{\pi} \left[\frac{1 - \cos 2\omega t}{2}\right] \cdot d\omega t}$$

$$= \sqrt{\frac{V_m^2}{2\pi}} \sqrt{\left[\omega t - \frac{\sin 2\omega t}{2}\right]_0^{\pi}}$$

$$= \sqrt{\frac{V_m^2}{2\pi}} \sqrt{\pi - \frac{\sin 2\pi}{2}}$$

$$V_{RMS} = \sqrt{\frac{V_m^2}{2\pi}} \cdot \sqrt{\pi}$$

$$\boxed{V_{RMS} = \frac{V_m}{\sqrt{2}}}$$

Ripple factor :-

Ripple factor is measure of ac component in the output of the rectifier.

Mathematically, the ripple factor found as the ratio of rms value of ac component to dc value in the output of the rectifier.

$$\text{Ripple factor} = \gamma = \frac{\text{rms value ac component}}{\text{dc component}}$$

let V_{ac} is the rms value of ac component in the o/p Rectifier

V_{DC} is the dc value of the output of the rectifier.

V_{rms} is the rms value of the combined waveform.

The rms voltage can be.

$$V_{rms} = \sqrt{V_{ac}^2 + V_{DC}^2}$$

$$V_{ac} = \sqrt{V_{Rms}^2 - V_{DC}^2}$$

Ripple factor $= \gamma = \frac{V_{ac}}{V_{dc}}$

$$\gamma = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{DC}}$$

$$= \sqrt{\left[\frac{V_{rms}}{V_{dc}}\right]^2 - 1} \qquad = \sqrt{\left[\frac{\frac{V_m}{\sqrt{2}}}{\frac{2V_m}{\pi}}\right]^2 - 1}$$

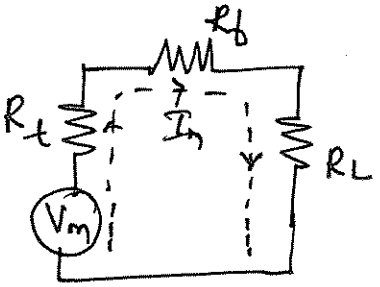
here $V_{rms} = \frac{V_m}{\sqrt{2}}$ $\qquad = \sqrt{\left(\frac{\pi}{\sqrt{2}}\right)^2 - 1} = 0.483.$

$V_{dc} = 2\frac{V_m}{\pi}$

Efficiency :- It is defined as the ratio of dc power delivered to the load to the total ~~input~~ input power to the rectifier.

$$\eta = \frac{\text{dc output power}}{\text{total input power}}.$$

$$\eta = \frac{P_{dc}}{P_i}.$$



In the circuit V_m is peak value of secondary voltage.

I_m is the peak value of current through the circuit.

By applying Ohm's law peak current I_m can be expressed as follows.

peak load current $I_m = \frac{V_m}{R_f + R_t + R_L}$

Here I_{dc} is the dc load current

$$P_{dc} = I_{dc}^2 R_L$$

Here $P_{ac} = I_{rms}^2 (R_f + R_t + R_L)$ ----

where R_f – resistance of the forward biased diode

R_t – is the resistance of secondary winding of the transformer.

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_f + R_t + R_L)}.$$

$$= \frac{\left[\frac{2I_m}{\pi}\right]^2 R_L}{\left[\frac{I_m}{\sqrt{2}}\right]^2 (R_f + R_t + R_L)}.$$

$I_{dc} = \frac{2I_m}{\pi}$

$I_{rms} = \frac{I_m}{\sqrt{2}}$

$$= \frac{8}{\pi^2} \left[\frac{R_L}{R_f + R_t + R_L}\right]$$

$$= 0.81 \frac{R_L}{R_f + R_t + R_L}$$

We get maximum efficiency when $R_f = 0$ & $R_t = 0$,

$$\boxed{\eta = 0.81}$$

Note:- $I_{DC} = \frac{2I_m}{\pi}$ $I_{rms} = \frac{I_m}{\sqrt{2}}$ $V_{DC} = \frac{2 \cdot V_m}{\pi}$

$V_{rms} = \frac{V_m}{\sqrt{2}}$ $V_{DC} = I_{DC} \cdot R_L$.

$V_{Rms} = I_{Rms} \cdot R_L$.

peak Load current $I_m = \frac{V_m}{R_f + R_t + R_L}$

$\eta = 0.81 \cdot \frac{R_L}{(R_f + R_t + R_L)}$ $\eta = 0.483$.

A full wave rectifier (centre taped rectifier) with a centre tapped secondary supplies power to a load of 500Ω. The input voltage to the circuit is 100V (peak value). Find the rms & average value of the load current, rms & average value of load voltage, ripple factor & Efficiency of the rectifier. Consider the forward resistance of the diode to be 10Ω.

given data:- $V_m = 100V$, $R_L = 500\Omega$, $R_f = 10\Omega$.

Find $I_{DC} = ?$ $I_{rms} = ?$ $V_{DC} = ?$, $V_{rms} = ?$

Ripple factor = ? $\eta = ?$

Ans:- $I_m = \frac{V_m}{(R_f + R_t + R_L)} = \frac{100}{(10+0+500)} = 0.196A.$

$I_{DC} = 2\frac{I_m}{\pi} = 2 * \frac{0.196}{\pi} = 0.124\,A.$

$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{0.196}{\sqrt{2}} = 0.1386\,A.$

$V_D = I_{DC} * R_L = 0.124 * 500.$

$= 62V.$

$V_{rms} = I_{rms} * R_L$

$= 0.1386 \times 500.$

$= 69.3V.$

Ripple factor $= 0.483.$

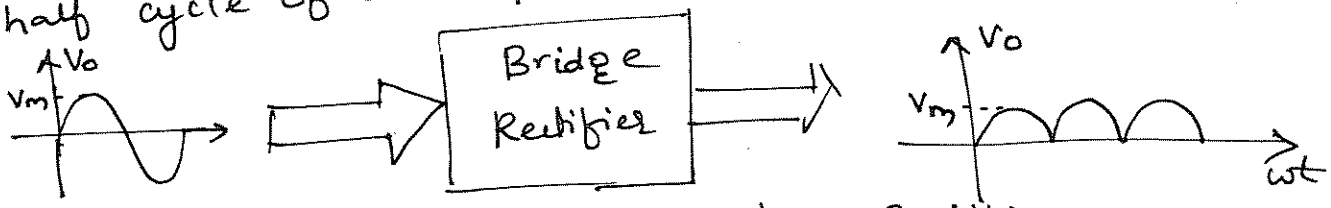
Efficiency $= \eta = 0.81 * \frac{R_L}{(R_f + R_t + R_L)}$

$= 0.81 * \frac{500}{(10+0+500)}.$

$\boxed{\eta = 0.7941}$

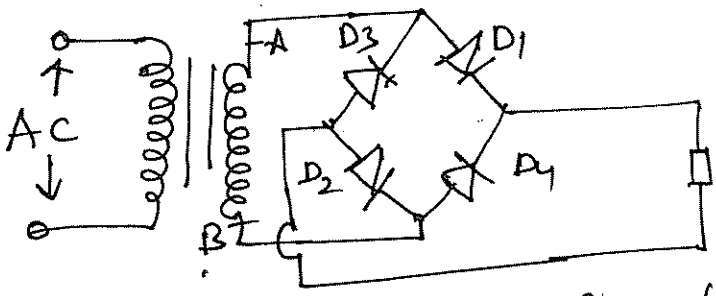
Bridge Rectifier :-

It is a circuit which provides output during both half cycle of the input.



Block diagram of Bridge Rectifier.

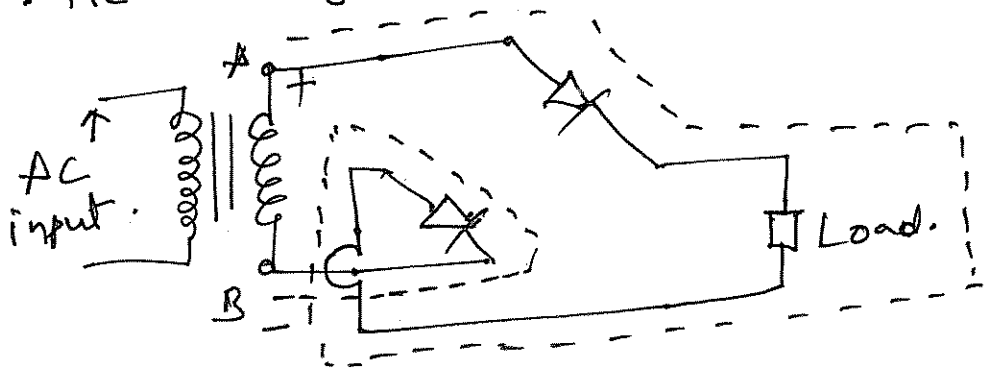
The bridge Rectifier using the four diodes and a transformer is shown. The Transformer in the given is used to either step-up or step-down the ac input voltages. Four diodes are connected to the secondary windings of the transformer.



circuit diagram of bridge Rectifier.

Working :-

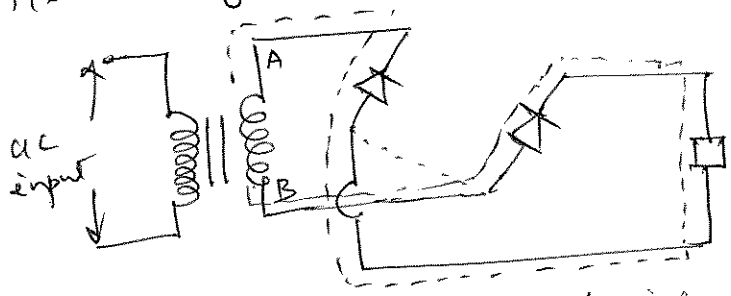
During the positive half cycle of the input signal let the terminal A becomes positive & the terminal B becomes negative. The diode D_1 & D_2 are forward biased & D_3 & D_4 are reverse biased. The current flows through the diode D_1, D_2 and the load. Hence we get the voltage across the load.



bridge Rectifier during positive half cycle.

During negative half cycle of the input signal, the terminal A becomes negative & the Terminal B becomes positive. D_3 & D_4 Forward biased.
D_2 & D_1 Reverse biased.

The current flows through the diode D_3, D_4 & the load Hence we get the voltage across the load.



Bridge Rectifier during negative half cycle.

Note: Since two diodes conduct during any of the half cycle. For efficiency & peak current Calculations $2R_f$ will be used.

In analysis bridge rectifier is same as that of full wave Rectifier with centre tapped transformer.

Formulae

DC output current $I_{DC} = \frac{2I_m}{\pi}$

rms output Current $I_{rms} = \frac{I_m}{\sqrt{2}}$

No load DC output voltage $V_{DC} = \frac{2V_m}{\pi}$

No load Rms output voltage $V_{rms} = \frac{V_m}{\sqrt{2}}$

When the resistance of transformer & Diode is considered then $V_{DC} = I_{DC} * R_L$ & $V_{rms} = I_{rms} \times R_L$

peak load current $I_m = \frac{V_m}{(2R_f + R_L + R_L)}$

ripple factor (γ) = 0.483.

efficiency = $\eta = 0.81 \frac{R_L}{2R_f + R_L + R_L}$

A Full wave Rectifier with a Centre tapped secondary transformer supplies power 5W to a load of 100Ω. Find the input voltage to the circuit. The Transformer has a secondary resistance of 25Ω. Consider $R_f = 20\Omega$.

Soln:

given.

$R_L = 100\Omega$

$R_f = 20\Omega$

$R_t = 25\Omega$

$P = 5W$.

Find $V_m = ?$

We know that

$$\text{Output power} = I_{dc}^2 \times R_L$$

$$5 = I_{dc}^2 \times 100$$

$$I_{dc}^2 = 5/100$$

$$I_{dc} = \sqrt{5/100}$$

$$\boxed{I_{dc} = 0.2236A}$$

W.K.T. $I_{dc} = 2\frac{I_m}{\pi} \Rightarrow I_m = \frac{I_{dc} * \pi}{2}$.

$$= \frac{0.2236 * \pi}{2}$$

$$\boxed{I_m = 0.35135A}$$

peak load current $I_m = \frac{V_m}{(R_f + R_t + R_L)}$

$$V_m = I_m(R_f + R_t + R_L)$$

$$= 0.35135\,(20 + 100 + 25)$$

$$= 0.35135 \times 145$$

$$\boxed{V_m = 50.94V}$$

(1) A Bridge Rectifier has Input voltage of 100sinωt. The diode resistance is 50Ω & the load resistance is 950Ω. Find the dc output voltage. ripple factor, & efficiency.

given:- $V_m = 100$, $R_f = 50\Omega$ $R_t = 0$ $R_L = 950\Omega$

Find. V_{DC}, V_{RMS}, Ripple factor, $\eta = ?$

$$I_m = \frac{V_m}{2R_f + R_t + R_L} = \frac{100}{1000} = 0.1A.$$

Find I_{DC}:

$$I_{DC} = \frac{2I_M}{\pi} = \frac{0.2}{\pi} = 0.06366\ A.$$

$$I_{RMS} = \frac{0.1}{\sqrt{2}} = 0.071\ A.$$

$$V_{DC} = I_{DC} \cdot R_L = 0.0636 * 950.$$
$$= 60.42V.$$

$$V_{RMS} = I_{RMS} * R_L$$
$$= 0.071 \times 950 = 67.45V.$$

ripple factor $= 0.483$.

$$\eta = 0.81 * \frac{R_L}{(2R_f + R_t + R_L)} = 0.81 * \frac{950}{1000} = 0.77.$$

Filters:- Half wave rectifier with a capacitor filter

A filter is a circuit that removes the ac component present in the output of a rectifier.

Consider a half wave rectifier with a capacitor C connected across the Load. as shown below.

Half wave rectifier with Capacitor filter.

The output of the rectifier is the input to the filter. When diode reverse biased or forward biased. Depending on that filter works.

When $V_i > V_c$.

The diode is in forward bias condition & Conducts current through the load resistor R_L. Hence the current produces an output voltage across the Load resistor R_L, which has the similar output to that of half wave rectifier.

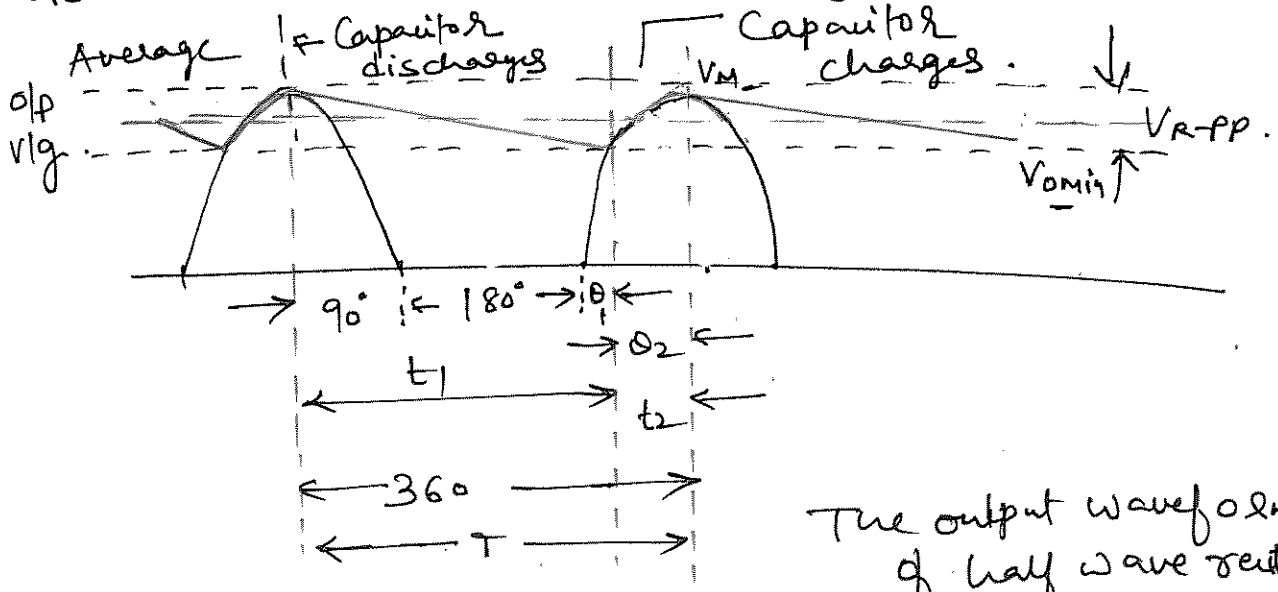
. At the same time the Capacitor is charged. At the end quarter cycle, when the input voltage reaches the maximum value, capacitor also charges to the maximum input value.

When input voltage falls below peak value.

$V_i < V_c$.

- The Diode reverse biased. Anode voltage less than Capacitor (Cathode) voltage. ∴ No current flows through the Diode.
- The capacitor which has been already charged starts discharging through the Load resistor.

. As capacitor discharges, the capacitor voltage & hence the output voltage magnitude decreases.



The output waveform of half wave rectifier with capacitor filter.

Full wave rectifier with a capacitor filter

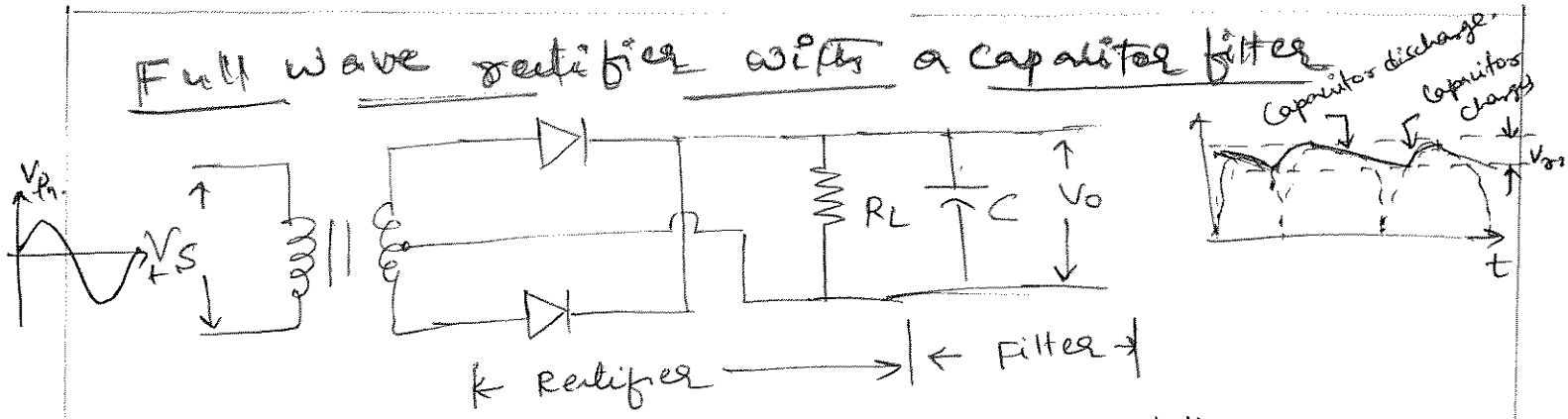


Fig: Fullwave rectifier with capacitor filter.

Case ①: $V_{in} > V_c$

When Diode is forward biased & conducts current through the Load resistor R_L. Hence the current produces an output voltage across the Load resistor R_L, which has the same shape as the initial input.

. During this time, the capacitor is charged. When the input voltage reaches the maximum value, the capacitor charged to the maximum value of the input voltage.

Case ② $V_{in} < V_p$. when the input voltage falls below the peak value.

The diode is reverse biased since anode voltage (input voltage) becomes less than the diode cathode voltage (capacitor voltage). ∴ no current through the diode.

During reverse biasing of Diode, the capacitor starts discharging through the Load resistor.

- The discharge current of the capacitor produces voltage across the load resistor; hence we get the output voltage.

The.

A Full wave Rectifier with a centre tapped secondary transformer supplies power 5W to a load of 100Ω. Find the input voltage to the circuit. The transformer has a secondary resistance of 25Ω. Take the $R_f = 20\Omega$.

Soln:- given $R_L = 100\Omega$ $R_f = 20\Omega$ $R_t = 25\Omega$.

$P = 5W$

Find V_m.

We know that

output power $= I_{dc}^2 * R_L$

$$5 = I_{dc}^2 * 100.$$

$$I_{dc}^2 = \frac{5}{100}$$

$$I_{dc} = \sqrt{\frac{5}{100}} = 0.2236\,A.$$

$$\frac{2I_m}{\pi} = I_{dc} \Rightarrow I_m = \frac{I_{dc} * \pi}{2}$$

$$= \frac{0.2236 * \pi}{2}$$

$$I_m = 0.35135A.$$

peak load current $I_m = \frac{V_m}{R_f + R_t + R_L}$

$$V_m = I_m(R_f + R_t + R_L)$$

$$= 0.35155 * 145.$$

$$\boxed{V_m = 50.94V}$$

Problems on Full Wave Rectifier

A Full wave rectifier with a centre tapped transformer secondary supplies power to a load of 100Ω. The input voltage to the circuit is 10V (rms value) through a transformer having a secondary resistance of 25Ω. Find Dc & rms output voltages, ripple factor output power, input power & efficiency of the rectifier forward resistance of the diode to be 10Ω.

given: $V_m = 10 * \sqrt{2}$ $\quad R_L = 100\Omega$, $R_f = 10\Omega$, $R_t = 25\Omega$.

$= 14.14$

Find: $I_{dc} = ?$ $I_{rms} = ?$ $V_{dc} = ?$ $V_{rms} = ?$ $\eta = ?$ P_{in}, P_{out}

Soln

W.K.T the peak load current $I_m = \frac{V_m}{R_t + R_f + R_L} = \frac{14.14}{100 + 10 + 25}$

$= 0.1047\ A$

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2 * 0.1047}{\pi} = 0.0666\ A$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{0.1047}{\sqrt{2}} = 0.0740\ A$$

$V_{DC} = I_{dc} * R_L = 0.0666 * 100 = 6.66\ V$

$V_{rms} = I_{rms} * R_L = 0.0740 * 100 = 7.4\ V$

$P_{out} = I_{DC}^2 R_L = (0.0667)^2 * 100 = 0.444\ W.$

$P_{in} = I_{rms}^2 (R_L + R_f + R_t) = (0.0740)^2 * (135) = 0.739\ W.$

Ripple factor (γ) $= 0.483$

$$\eta = 0.812 * \frac{R_L}{R_L + R_f + R_t}$$

$$= 0.812 * \frac{100}{135} = 0.6014$$

$\% \eta = 60.14$

A full wave Rectifier is supplied power through a step down transformer with a primary input voltage of 250V. The turns-ratio of the transformer is 10. The load resistance is 1KΩ. The resistance of the secondary winding of the transformer is 12Ω. & that of diode is 13Ω. Calculate the dc & rms value of the output voltage. Find Regulation.

given $V_p = 250\,V$ turns ratio = 10, $R_L = 1K\Omega$, $R_t = 12\Omega$, $R_f = 13\Omega$

Find, V_{dc}, V_{rms}, Regulation.

Solution:- Secondary voltage $= \frac{V_p}{\text{turn-ratio}} = \frac{250}{10} = 25V$.

$$V_m = \sqrt{2}\, V_s = \sqrt{2} \times 25$$
$$= 35.35\,V$$

peak load current $I_m = \frac{V_m}{R_f + R_L + R_t} = \frac{35.35}{1025} = 0.0345A$

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2 * 0.0345}{\pi} = 0.022A$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{0.0345}{\sqrt{2}} = 0.02439A$$

$$V_{dc} = I_{dc} * R_L = 0.022 * 1000 = 21.95V = 22V$$

$$V_{rms} = I_{rms} \times R_L = 0.02439 * 1000 = 24.39 = 25V$$

$$\text{Regulation} = \frac{R_t + R_f}{R_L} = \frac{25}{1000} = 0.025$$

Problem on half wave rectifier :-

(2) A half wave rectifier is supplied power through a step down transformer with a primary input voltage of 250V. The primary to secondary turns ratio of the transformer is 10. The Load resistance is 1kΩ. The resistance of the secondary winding of the transformer is 12Ω & that of diode is 13Ω. Calculate dc & rms value of the output voltage. Also Find the Regulation.

Soln :- $V_p = 250V$. turns ratio = 10. $R_L = 1k\Omega$ $R_t = 12\Omega$ $R_f = 13\Omega$

$V_s = \frac{V_p}{\text{turns ratio}} = \frac{\text{Primary i/p voltage}}{\text{turns ratio}}$

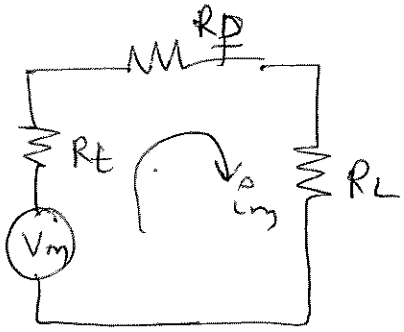
$= \frac{250}{10}$

$= 25.$

$V_{dc} = ?$

$V_{rms} = ?$

Regulation = ?



$V_m = \sqrt{2} * V_s$

$= 35.35\ V$

The peak Load current

$I_m = \frac{V_m}{(R_f + R_t + R_L)} = \frac{35.35}{1025}$

$= 0.0345\ A.$

$I_{dc} = \frac{I_m}{\pi} = \frac{0.0345}{\pi} = 0.0109\ A$ $V_{dc} = I_{dc} \times R_L = 10.97\ V.$

$I_{rms} = \frac{I_m}{2} = 0.0172\ A.$ $V_{rms} = I_{rms} \times R_L = 17.2\ V.$

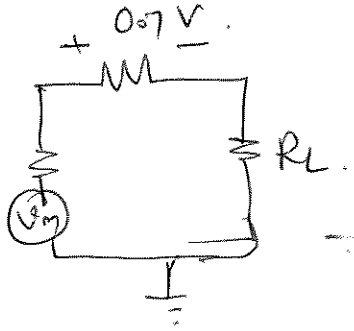
$\text{Regulation} = \frac{I_{dc}(R_f + R_L)}{V_{dc}} = \frac{0.0109 \times (25)}{10.97}$

$= 0.0248.$

% Regulation = 2.48%

(3). A diode in a half wave rectifier has $V_F = 0.7V$. The Load resistance is 600Ω. & the ac input voltage is 25V (rms). Determine dc & rms output voltage.

given:- $V_f = 0.7$ $R_L = 600\Omega$, $V_s = 25V$ V_{dc}?, V_{rms}?



$V_m = \sqrt{2} * V_s$

$= \sqrt{2} \times 25$

$V_m = 35.35V$

$I_m = \frac{V_m - V_F}{R_f + R_t + R_L}$

$= \frac{35.35 - 0.7}{(600+0+0)}$

$I_m = 0.0588A$

$R_f = 0$

$R_t = 0$

$V_{dc} = \frac{I_m}{\pi} = 0.0187A = \frac{0.058}{\pi} = 0.0187A$

$I_{rms} = \frac{I_m}{2} = 0.0294A = \frac{0.058}{2} = 0.0294$

$V_{DC} = I_{DC} * R_L = 0.018 * 600 = 10.8V$

$V_{Rms} = I_{rms} \times R_L = 0.029 \times 600 = 17.4V$

Photo Diode:-

Light definition and units.

According to the quantum theory, light is in the form of photons and each photon delivers an energy packet to the surface on which it falls.

$$W = hf \text{ joules.}$$

where, h = planck's constant 6.624×10^{-34} Joules seconds

f = frequency of light waves in Hz.

Another important information is that light also behaves as travelling wave.

The frequency of light is directly related to its wavelength, as

$$f = V/\lambda$$

where

V = velocity of light (3×10^8 m/s)

λ = Wavelength in meters, A° or μm.

1 angstrom (A°) = 10^{-10} m

1 micrometer (μm) = 10^{-6} m

Intensity of light is measured in units of luminous flux incident on unit area.

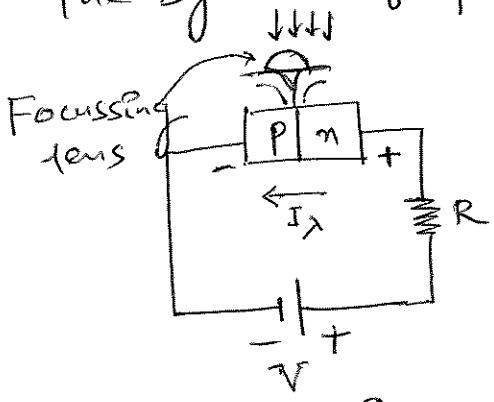
Unit of luminous flux are lumens.

$$1 \text{ lm} = 1.496 \times 10^{-10} \text{ W}$$

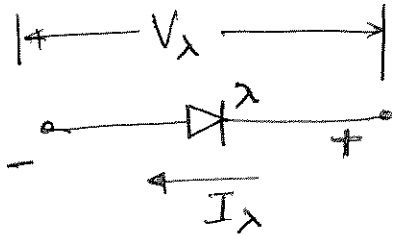
Intensity of light can be measured with the following pratical unit. 1 lm/ft^2, called foot-candle (fc = 1.609×10^{-9} W/m^2

A photodiode is a PN junction (silicon/ germanium) operates in reverse-bias region as shown in figure 1(a)

The symbol of photodiode is also shown in figure 1(b)



1(a). photo diode in reverse bias condition.



1(b) Symbol

A light is made to impinge on the junction (pn), the light photons impart energy to the valence electrons causing more electron-hole pairs to be released.

As a result, the concentration of minority carriers increases and current I_λ also increases.

The reverse saturation current I_λ is limited by the availability of thermally generated minority carrier.

The VI characteristics for various values of light intensity (fc) are draw in figure 2.

The dark current characteristic corresponding to no-light impingement ($I_\lambda = I_s$).

Here for the certain V_λ (say 20V), I_λ increases almost linearly with fc.

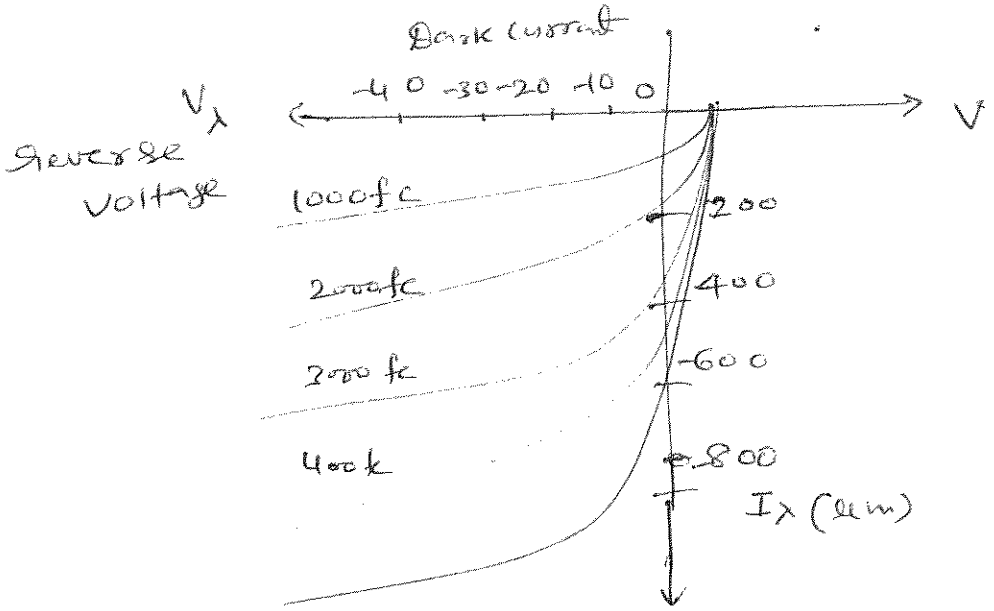


Fig (2). VI Characteristics of photo diode

Generally Ge photo diode has more overlaps Compared to Si, which spans the range of light frequency to which the human eye is sensitive.

Ge is, therefore, more suitable for infra-red (IR) light sources like lasers.

Light Emitting Diode (LED)

In a forward biased PN Junction diode recombination of electrons & holes takes place at the junction and within the body of the crystal, extrinsic at the location of a crystal defect.

The free electrons will be captured by holes, the electron goes into a new state & its kinetic energy is given off as heat & as light photons.

In silicon diode, most of the energy is given off as heat but in other materials such as gallium arsenide (GaAs) or Gallium phosphide (GaP) sufficient number of photons (light) are generated so as to create a visible source.

This process of light emission in PN Junctions of such materials is shown in fig (3) & it is called as electroluminescence.

The metal contact of P-material is made small to permit the emergence of maximum number of photons so that in an LED, the light lumens generated per watt of electric power is quite high.

Intensity of light increases almost linearly with forward current, depending on the material used.

The voltage levels of LEDs are 1.7V & to 3.3V. It is compitable with solid-state circuits. The response time is short few ns (nanoseconds) and light contrast is good.

LED emit light in red green. orange or blue color.

Applications

used in Display applications.

(1) 8 segment display of numbers 0 to 9.

(2) LED TV's.

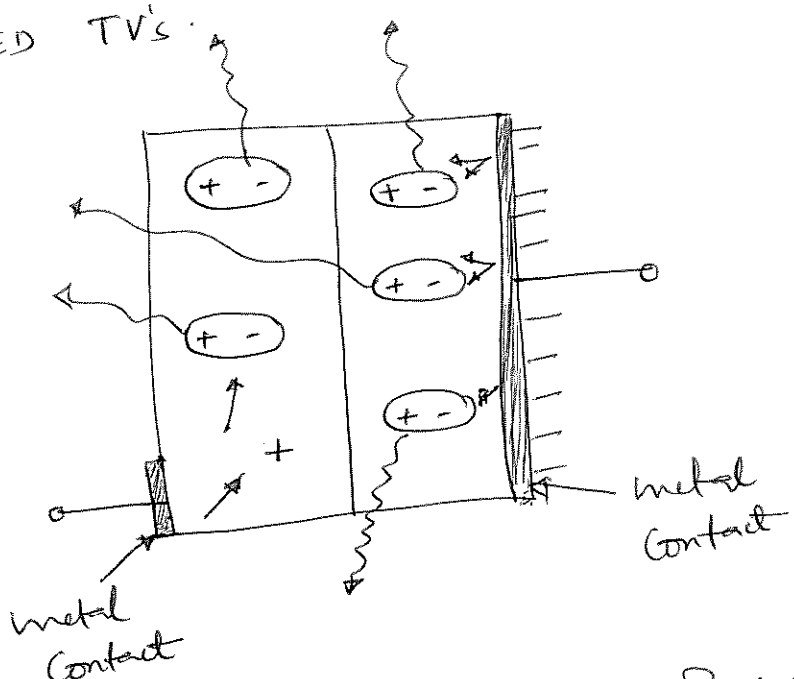


Figure (3). Light emission in pN Junction

For a photodiode, determine I_λ if $V_\lambda = 30V$ and intensity of light is $3.22 \times 10^{-6} w/m^2$. Given $I_\lambda = 300 \mu A$ for 30V in figure (2).

light intensity in fc

$$f_c = \frac{3.22 \times 10^{-6}}{1.609 \times 10^{-9}}$$

$$= 2000.$$

Photo Coupler

It is a package of an LED and photodiode whereas circuits are electrically isolated as in figure (4). The LED is forward biased & the photodiode is reverse biased. The output is available across R_2.

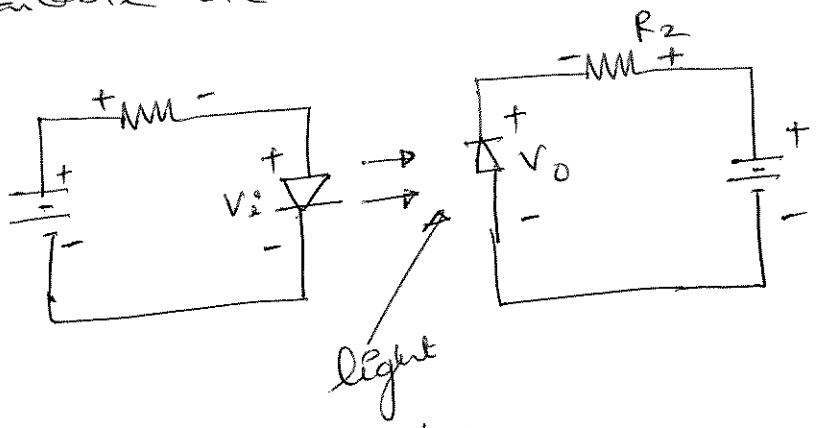


Figure (4) photo coupler

Advantage of photo coupler is electrical isolation between two circuits.

It is employed to couple circuits whose voltage level may differ by several thousand volts.

78XX Series & 7805 Fixed IC Voltage Regulator

We learnt in previous topic that Zener diode can be used as voltage regulator. Similarly we have Integrated circuits are also called as monolithic linear regulators namely

LM 7800 series
LM 7805 Fixed Regulator

LM7800 series

The LM78XX series (where XX = 05, 06, 08, 10, 12, 15 18 or 24) is a typical three terminal voltage Regulators.

The 7805 produces an output of +5V
7806 produces +6V
7808 produces +8V & so on upto
& 7824 produces an output of +24V

The Functional block diagram of 78xx series voltage regulator is shown in figure 5.

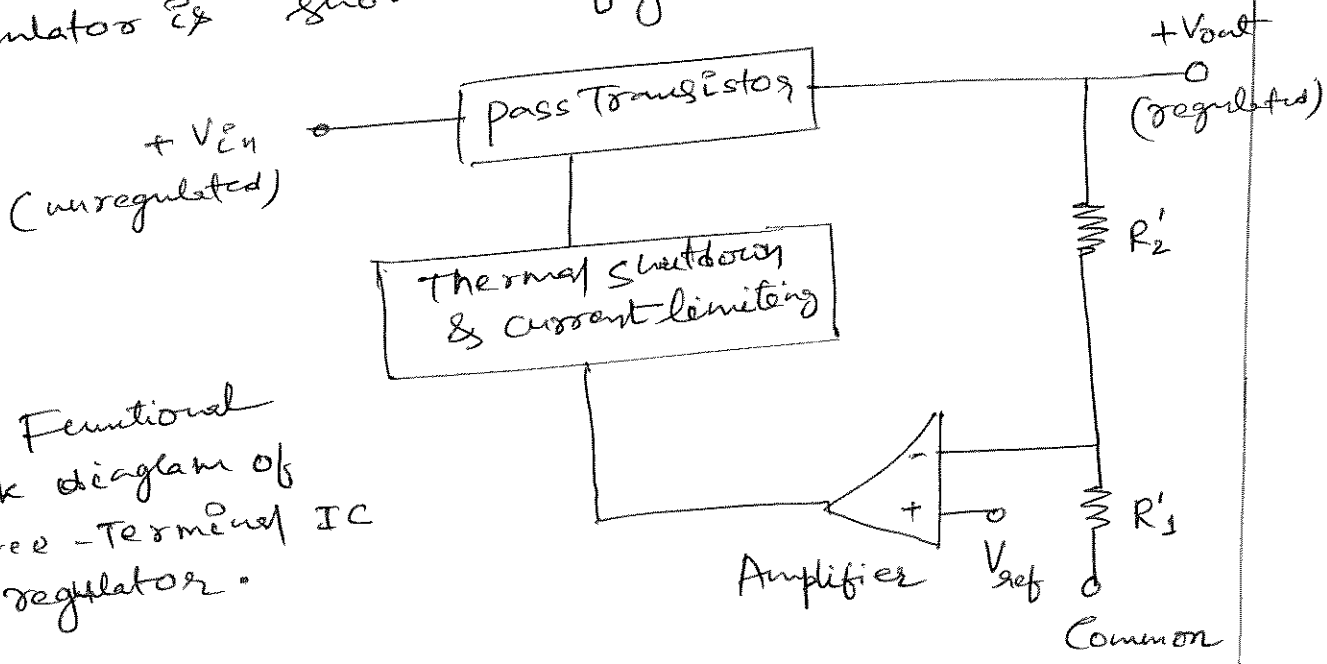


Fig 5. Functional block diagram of Three-Terminal IC regulator.

IC regulators are series regulator because they are more efficient than the shunt regulator.

IC regulator will have three pins

1. Unregulated input voltage pin
2. regulated output voltage pin
3. Ground.

Available in plastic or metal packages, these are popular because they are inexpensive & easy to use.

The output voltage of IC regulator may be

fixed positive
fixed negative or
adjustable.

A built in reference voltage V_{ref} drives the non-inverting input of an amplifier.

A voltage divider circuit consisting of R_1' and R_2' samples the output voltage and returns a feedback voltage to the inverting input of a high gain amplifier.

The output voltage is given by

$$V_{out} = \frac{R_1' + R_2'}{R_1'} V_{ref}.$$

The reference voltage is similar to zener voltage.

The primes attached to R_1' & R_2' indicate that these resistors are inside the IC itself, rather than being external resistors, rather than being external resistors.

These resistors are factory-trimmed to get the different output voltages (5 to 15V) in the 78xx series.

The tolerance of the output voltage is ±4 percent.

The LM78xx includes a pass transistor, it can handle 1A of load current, provided that adequate heat sinking is used.

Thermal shutdown & current limiting circuit included. Thermal shutdown means that the chip will shut itself off when the internal temperature becomes too high, around 175°C.

This is a precaution against excessive power dissipation, which depends on the ambient temperature type of heat sinking & other variables.

Because of thermal shutdown & current limiting, devices in the 78xx series are almost indestructible.

LM7805 Fixed IC Regulator

LM7805 is a fixed voltage Regulator IC. It has three pins pin 1 is the input, pin 2 is the output and pin 3 is grounded.

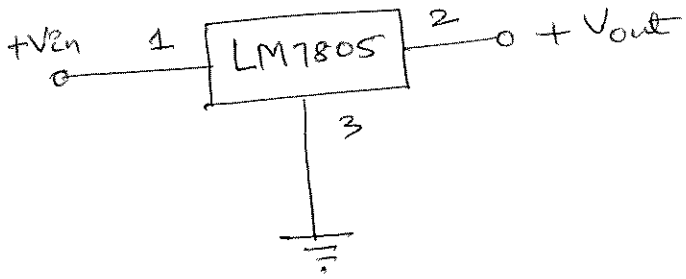
LM7805 has an output voltage of +5V and a maximum load current over 1A.

The typical load regulation is 10 mV for a load current between 5 mA & 1.5 A.

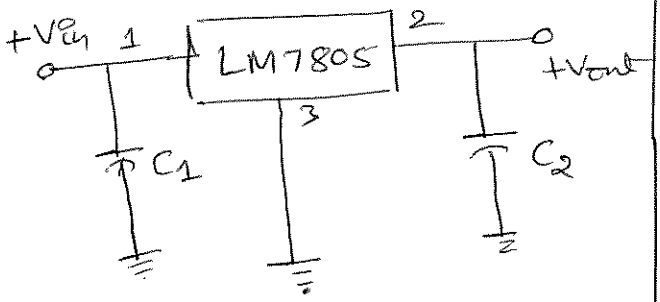
The typical line regulation is 3 mV for an input voltage of 7 to 25 V.

LM 7805 has a ripple rejection of 80dB, which means that it will reduce the input ripple by a factor of 10,000.

LM7805 is a very stiff voltage source to all loads within its current rating with output resistance of 0.01Ω.



(a) using a 7805 as Voltage Regulator.



(b) Input Capacitor prevents oscillations and output Capacitor improves frequency response

When an IC is more than 6 from the filter capacitor of the unregulated power supply, oscillations will be produced because of the inductance of the connecting wires. Hence to avoid oscillations bypass Capacitor C_1 is used near p1. The value suggested by manufacture in data sheet will be 0.22μF for 78xx series IC.

A bypass Capacitor C_2 is sometimes used on pin 2 to improve the transient responses of the regulated output voltage. The C_2 output Capacitor value is 0.1μF.

78XX series Regulator has a drop-out voltage of 2 to 3 V depending on the output voltage. It means that input voltage is 2 to 3 V greater than that of output voltage.

otherwise, the chip stop regulating. Also there is a maximum input voltage because of excessive power dissipation.

For instance, the LM7805 will regulate over an input range of approximately 8 to 20 V.

The data sheet for the 78xx series gives the minimum and maximum input voltages for the other preset output voltages.

A half wave

Module - 2

FET and SCR:

Introduction JFET:

Construction & operation, JFET Drain characteristics and parameters, JEFT Transfer Characteristic. Square law expression for I_D, Input resistance MOSFET: Depletion and Enhancement type MOSFET - Construction, operation, characteristics & Symbols, refer 7.1, 7.2 7.4 7.5 of Text 2)
CMOS (4.5 of Text 1)

Silicon Controlled Rectifier (SCR).

Two - transistor Model
Switching action, characteristics
phase Control application.
[refer 3.4 upto 3.4.5 of Text 1]

RBT Levels: L1 L2 & L3.

JFET — Junction Field Effect Transistor.

Introduction :-

Field Effect Transistor (FET) are unipolar devices because, they operate only with one type of charge carrier, But Bipolar junction Transistor (BJT) are bipolar devices are uses both electron & hole current.

FET's.

JFET MOSFET

JFET — Junction field effect transistor
MOSFET — metal oxide semiconductor FET.

Field effect is a term which relates to the depletion region formed in the channel of a FET as a result of a voltage applied on one of its terminal (gate).

BJT is a current-Controlled device; i.e the base current Controls the amount of collector current.

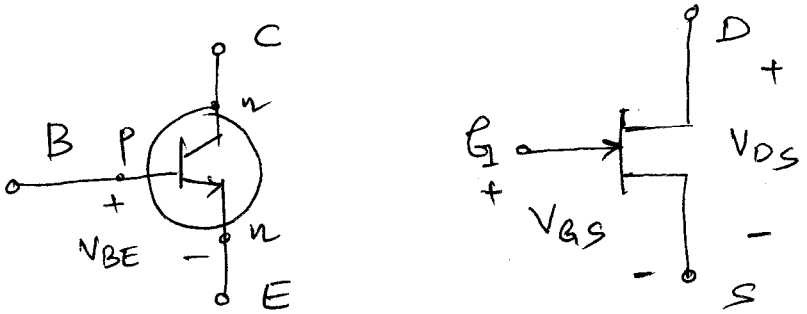
FET is a voltage-Controlled device, where the voltage between two of the terminal (gate and source) Controls the current through the device.

The BJT has few disadvantages such as it offers low input impedances & considerable noise level.

A major advantage of FET's is their very high input resistance. They are non-linear in nature, not widely used as amplifiers. but used where high input impedance is required.

- FETs used in Low-voltage switching applications because they are generally faster than BJT's when turned ON and OFF. IGBT used in high-voltage switching application.

JEFT:- It is a three terminal unipolar semiconductor device in which current conduction is by one type of carrier either electrons or holes. It is a voltage controlled device.



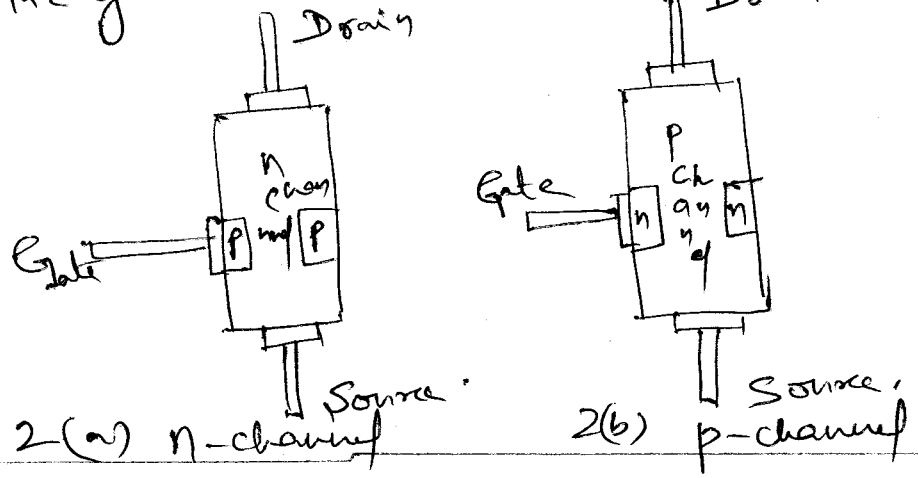
ⓐ BJT (npn).
Control current I_B
Control output I_C

ⓑ n-channel JFET
input voltage V_{GS}
controls output
current.

Basic structure:

Figure shows the basic structures of an n-channel and p-channel JFET are shown in fig. 2 (a) & 2 (b)

In n channel JFET wire leads are connected to each end of the n-channel; the drain is at the upper end, and the source is at the lower end. Two p-type regions are diffused in the n-type material to form a channel, and both p-type regions are connected to the gate lead. gate is connected to p-region.



2(a) n-channel
2(b) p-channel

Fig (2) Basic structure of n-channel & p channel JFET.

Basic operation:

→ Fig (3) shows Applying DC bias voltages applied to an n channel device.

→ V_{DD} provides a drain-to-source voltage and supplies current from drain to source.

→ V_{GG} sets the reverse bias voltage between the gate and the source.

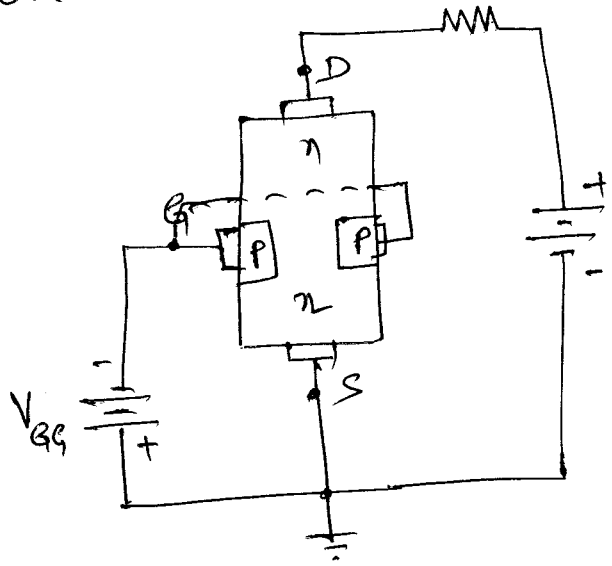


Fig (3).
A biased n-channel JFET

The JFET is always operated with the gate-source pn junction reverse-biased.

Reverse biasing of the gate-source junction with a negative gate voltage produces a depletion region along the pn-junction, which extends into the n-channel and thus increases its resistance by restricting the channel width.

The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current I_D.

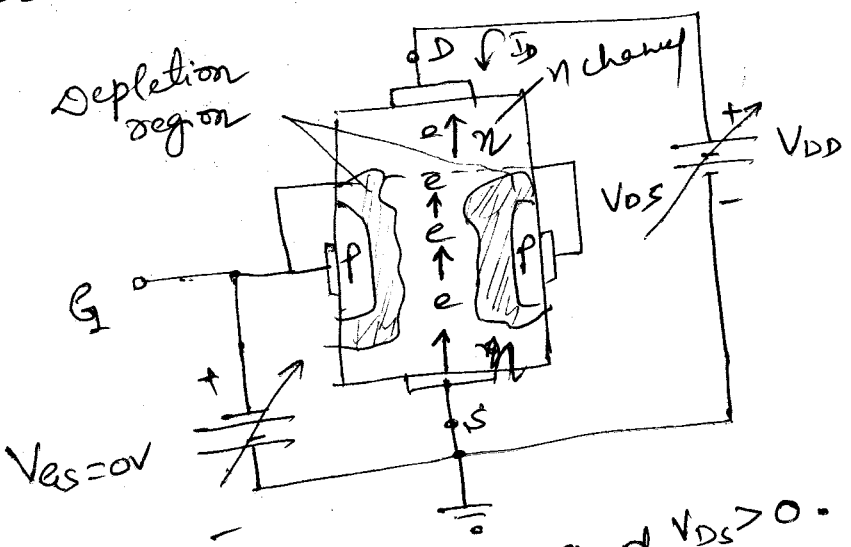
Case (1)

When $V_{GS}=0$, and V_{DS} is increased from zero. Under this condition voltage on the gate terminal is made zero and voltage between drain and source is applied as shown in figure.

The electrons (majority charge carriers) will start flowing from source to drain whereas conventional drain current I_D flows through the channel from drain to source.

The width defines the amount of electrons, flowing through channel. Since $V_{GS}=0$, we cannot control the flow of electrons from source to drain.

The electrons are drawn to the drain terminal establishing the conventional current I_D due to a small V_{DS} applied across drain-source terminals.



JFET at $V_{GS}=0$ V and $V_{DS}>0$.

Case (2): When V_{GS} is applied ($V_{GS}<0$).

When a reverse voltage V_{GS} is applied between gate and source. The reverse bias voltage across the gate source junction is increased.

As a result of this, the depletion regions are widened. Automatically this reduces the width of the conduction channel.

When the gate to source voltage V_{GS} is increased further, a stage is reached at which two depletion regions touch each other as shown in figure.

At this stage, the channel is completely blocked for the flow of electrons from source to drain and hence drain current becomes zero. The value of V_{GS} where $I_D = 0$ referred to as pinch off voltage V_p or $V_{GS(off)}$.

Note: From above explanation, it is clear that current from drain to source can be controlled by the application of potential on gate voltage. For this reason the device is called field effect (voltage controlled) transistor.

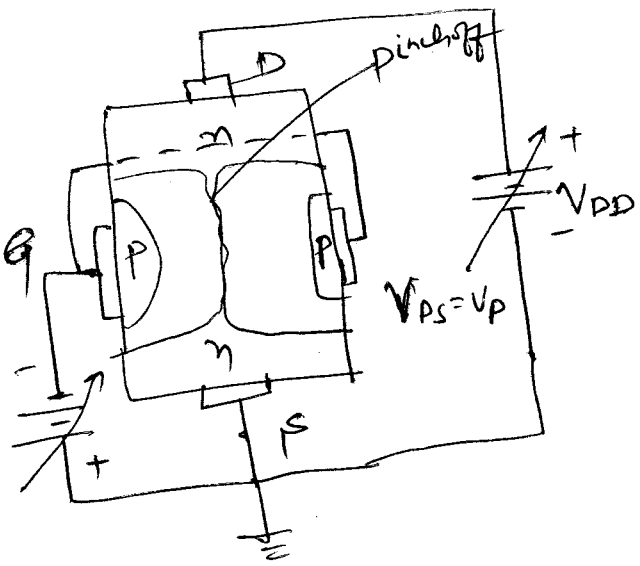


Fig. Pinch-off ($V_{GS} = 0V$, $V_{DS} = V_p$).

$V_{GS} < 0V$: V_{GS} is negative, i.e the gate terminal is made more negative than source. The level of V_{GS} that results in $I_D = 0mA$ is defined by $V_{GS} = V_p$, with V_p being negative voltage for n-channel devices

and a positive voltage for p-channel JFETs.

p-Channel Devices :-

The p-channel JFET is shown in figure is constructed in exactly the same manner as the n-channel device but with a reversal of the p- and n-type materials. The defined current directions and actual polarities of the voltages V_{GS} and V_{DS} are reversed.

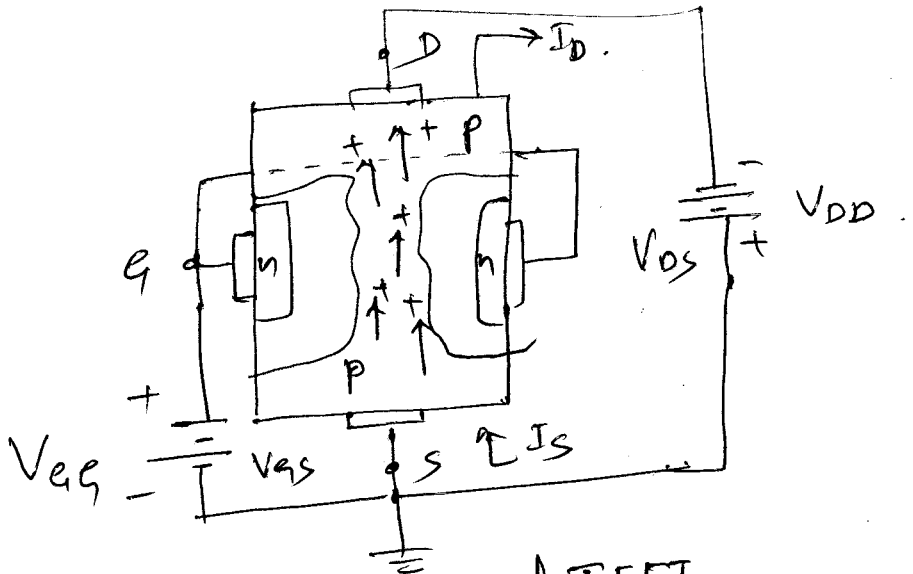
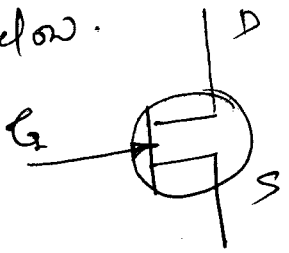


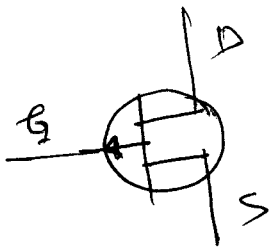
Fig. p-channel JFET.

JFET Symbols.

The ARROWS on the Gate point "in" for n channel JFET and "out" for p channel JFET are shown in figure below.



n-channel JFET



p-channel JFET.

Schematic Symbol.

JFET characteristics and parameters :-

JFET operates as a voltage Controlled, Constant Current device. There are two types of characteristic curve.

(1) Drain characteristics or V-I characteristics.

(2) Transfer characteristics

The set of curves which relate device current and voltage are known as characteristic curves.

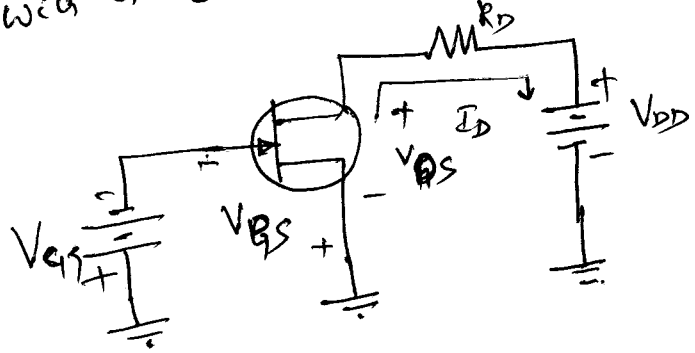
Drain characteristics :-

These curves give relationship between the drain current (I_D) and drain to source voltage (V_{DS}) for different value of gate-to-source voltage (V_{GS}).

Transfer characteristics :-

These curves give relationship between drain current (I_D) and gate to source voltage (V_{GS}) for constant, small positive potential (V_{DS}) applied to the drain to source terminal.

Here the n-channel JFET is Connected in Common source mode. Here we can use potentiometer to vary the voltages V_{GS} and V_{DS}. The voltages V_{DS} and V_{GS} may be measured by the voltmeters connected across the JFET terminals. The I_D can be measured by the milliammeter connected in series with the JFET and supply voltage V_{DD}.



JFET in Common source mode.

JFET Drain characteristics :-

The characteristics of JFET divided into three different regions, namely

(1) Ohmic region
(2) Saturation region.
(3) cut-off region

The voltage applied to the drain is termed as V_{DS} and the voltage to the gate is called as V_{GS}.

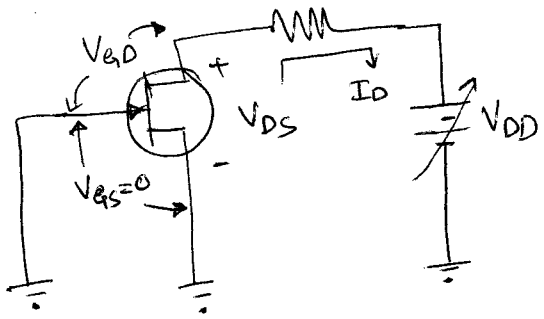
Drain characteristic is also called as output characteristics. Variation of output current I_D by varying the output voltage V_{DS} by keeping input voltage V_{GS} constant.

The circuit arrangement for Drain characteristics is shown in figure.

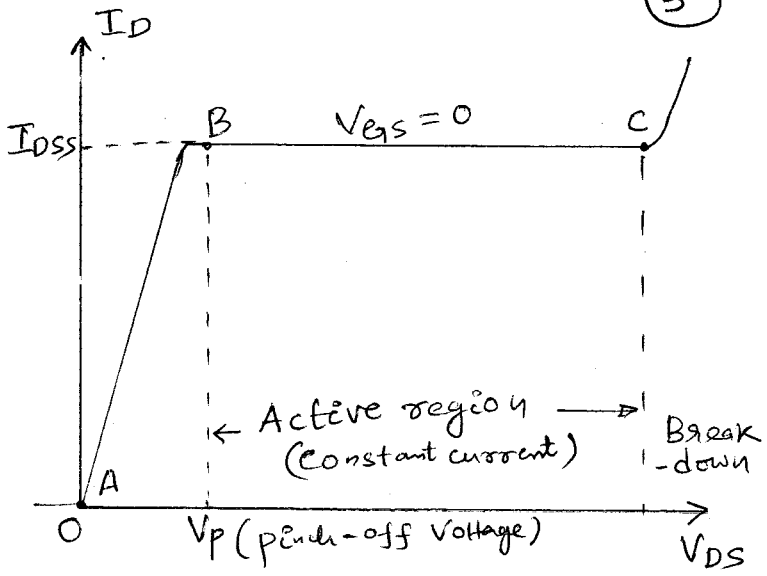
Consider the case when the gate-to-source voltage is zero ($V_{GS} = 0V$). As V_{DD} (and thus V_{DS}) is increased from 0V, I_D will increase proportionally, as shown in figure. (b) between points A and B. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the ohmic region because V_{DS} and I_D are related by ohm's law.

Ohmic region :- ($V_{DS} > 0$ and $V_{DS} < V_P$).

- Here channel depletion layer is very small and the JFET acts as a variable resistor.
- From point A to B, the drain current increases linearly with the increase in drain-to-source voltage, obeying ohm's law - Here N channel acts like a simple resistors hence this is a linear increase in drain current.



(a) JFET with $V_{GS}=0V$ and a variable V_{DS} (V_{DD}).



(b) Drain characteristic.

At point B in figure, the curve levels off and enters the active region or saturation region where I_D becomes essentially constant.

As V_{DS} increases from point B to point C. The reverse-bias voltage from gate to Drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping I_D constant.

Pinch-off voltage :-

For $V_{GS}=0V$, the value of V_{DS} at which I_D becomes essentially constant (point B on the curve) is the pinch-off voltage V_p. For a given JEFT, V_p has a fixed value.

I_{DSS} : Maximum Drain Current / (Drain-to-Source current with gate shorted).

After the pinch-off voltage, a continued increase in V_{DS} above the pinch-off voltage produces an almost constant drain current. This constant value of drain current is I_{DSS} and is always specified on JFET datasheets.

I_{DSS}: is the maximum drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, $V_{GS} = 0\,V$.

Breakdown:

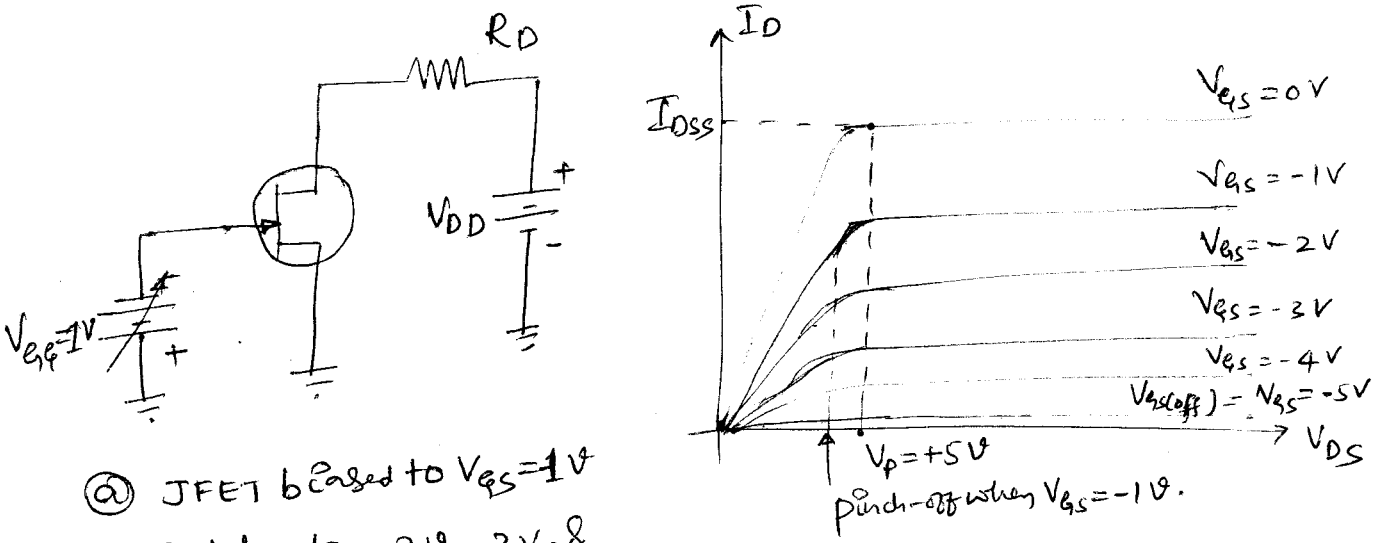
As shown in figure (b), breakdown occurs at point C when I_D begins to increase very rapidly with any further increase in V_{DS}.

Breakdown can result in irreversible damage to the device, so JFET are operated below breakdown & with in the active region (constant current) Between point B & C (in the graph). The breakdown point is shown with point C.

Now we connect a bias voltage, V_{GG} from gate to source as shown in figure (a). As V_{GS} is set to increasingly more negative values by adjusting V_{GG} a family of drain characteristic curve is obtained. as shown in figure (b)

In figure I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel.

We observe that, for each increase in V_{GS}, the JFET reaches pinch-off (where constant current begins) at values of V_{DS} less than V_p. The term pinch-off is not same as pinch off -voltage V_p.., The amount of drain current is controlled by V_{GS}, as shown in figure.



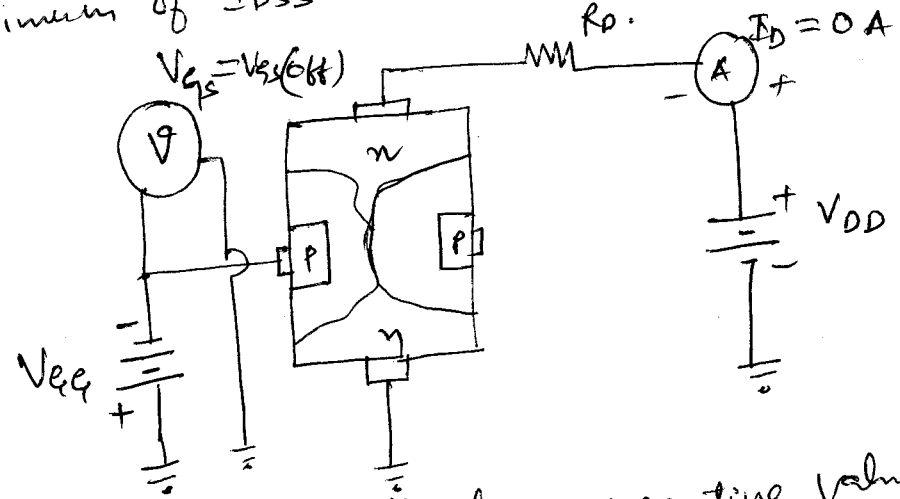
ⓐ JFET biased to V_{GS}=1V & later to -2V, -3V, & -4V and -5V.

ⓑ Family of drain characteristics curves.

Fig:- Drain characteristic curve with Applied V_{GS}.

Cutoff Voltage : $V_{GS(off)}$:-

The value of V_{GS} that makes I_D approximately zero is the cutoff voltage, $V_{GS(OFF)}$. as in figure ⓑ. the JFET must be operated between V_{GS}=0V and $V_{GS(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.



when V_{GS} has a sufficiently large negative value. I_D is reduced to zero. this cut off effect is caused by widening of the depletion region to a point where it completely closes the channel. as shown in figure.

Note:-

Pinch-off voltage and cutoff voltage:-

The pinch-off voltage V_p is the value of V_{DS} at which the drain current becomes constant and equal to I_{DSS} and is always measured at $V_{GS} = 0V$.

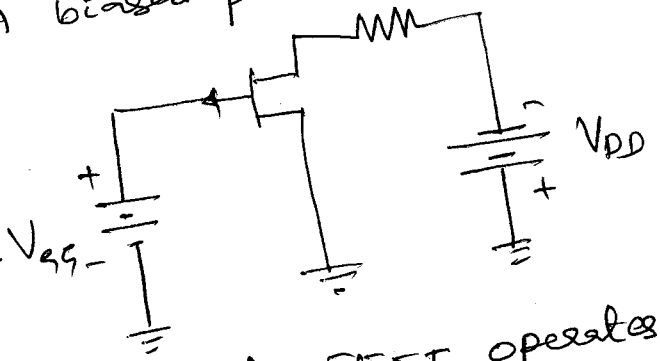
However the pinchoff occurs for V_{DS} values less than V_p when V_{GS} is non zero.

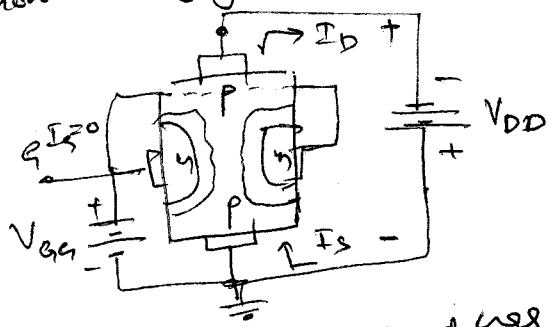
$V_{GS(off)}$ and V_p are always equal in magnitude but opposite in sign.

For Eg. if $V_{GS(off)} = -5V$. then $V_p = +5V$. as shown in figure.

Biasing of p-channel JFET:-

A biased p-channel JFET is shown in figure.





p channel JFET operates in the same way and has the similar characteristics as an N-channel JFET except that channel carriers are holes instead of electrons and the polarities of V_{GS} and V_{DD} are reversed as well as the direction of the output current I_D.

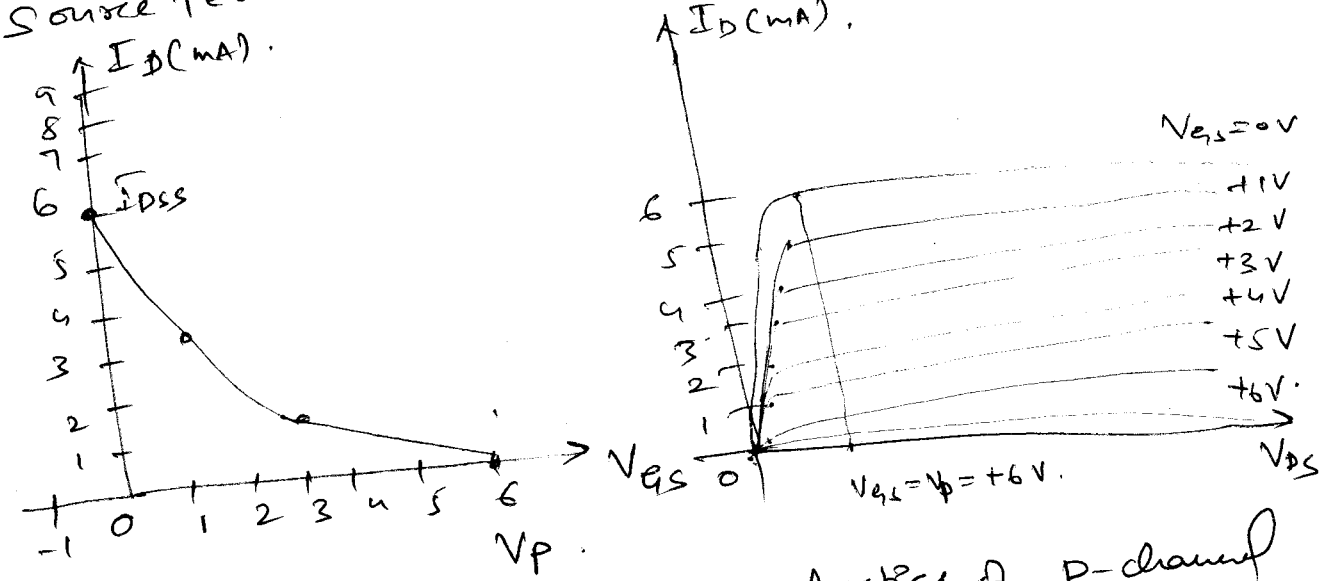
In p-type JFET holes acts as majority charge carriers, due to movement of these holes, current flow take place in transistor. p-channel JFET has three terminals with two n-type materials connected back to back as gate terminal & the p-type materials acts as source & drain ends.

As holes are majority charge carriers at $V_{GS}=0V$, the current flow is maximum when the positive V_{GS} is applied the current flow starts decreasing due to reverse bias at gate terminal and current flow is due to the negative V_{DS} across drain & source terminals.

Characteristics of p-channel JFET:-

From the drain characteristics it is clearly shown that at lower value of V_{GS} gain is maximum as the input voltage is (V_{GS}) increased gain automatically decreases as the channel gets shrinked.

At higher negative V_{DS} voltage the transistor starts to breakdown as the transistor fails to resist to the flow of current in the channel the breakdown is caused mainly because of higher positive voltage applied to source terminal.



Drain & Transfer characteristics of p-channel JFET.

Problem:-

(1) For the JFET in figure $V_{GS(off)} = -4V$ & $I_{DSS} = 12mA$ Determine the minimum value of V_{DD} required to put the device in the constant current region of operation when $V_{GS} = 0V$.

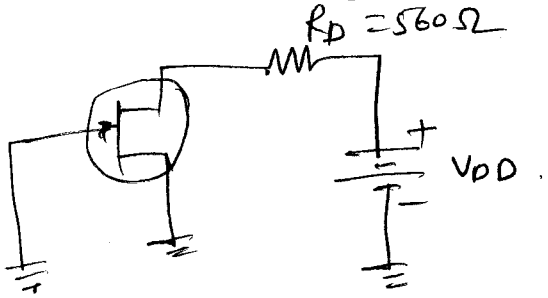


Figure:

Given:-

$V_{GS(off)} = -4V$

$I_{DSS} = 12mA$

$V_{DD} = ?$

$V_{GS} = 0V$.

Since $V_{GS(off)} = -4V$, then pinch-off voltage $V_p = +4V$.

The minimum value of V_{DS} for the JFET to be in its constant current region is

$$V_{DS} = V_p = 4V.$$

In constant current region with $V_{GS} = 0V$,

$$I_D = I_{DSS} = 12mA.$$

The drop across the drain resistor is

$$V_{RD} = I_D R_D = (12mA)(560\Omega) = 6.72V.$$

Apply Kirchhoff's law around the drain circuit.

$$V_{DD} = V_{DS} + V_{RD} = 4V + 6.72V$$
$$= 10.7V.$$

(2). In the above problem, if V_{DD} is increased to 15V. what is drain current?

Soln:- $V_{DD} = 15 = V_{DS} + V_{RD} = 4 + V_{RD}$.

$$V_{RD} = 15 - 4 = 11$$

$$I_D R_D = 11 \Rightarrow I_D = \frac{11}{560\Omega} = 0.0196A$$

or $\boxed{19.6mA. = I_D}$

JFET universal Transfer characteristics

Now, we know that a range of V_{GS} values from zero to $V_{GS(off)}$ controls the amount of drain current. For an n-channel JFET, $V_{GS(off)}$ is negative, and for p-channel JFET, $V_{GS(off)}$ is positive.

The Transfer characteristics for a JFET can be determined experimentally, keeping drain-source voltage, V_{DS} Constant and determining drain current, I_D for various values of gate-Source voltage V_{GS}.

→ It shows relationship between V_{GS} and I_D.
→ This curve is also known as transConductance curve.

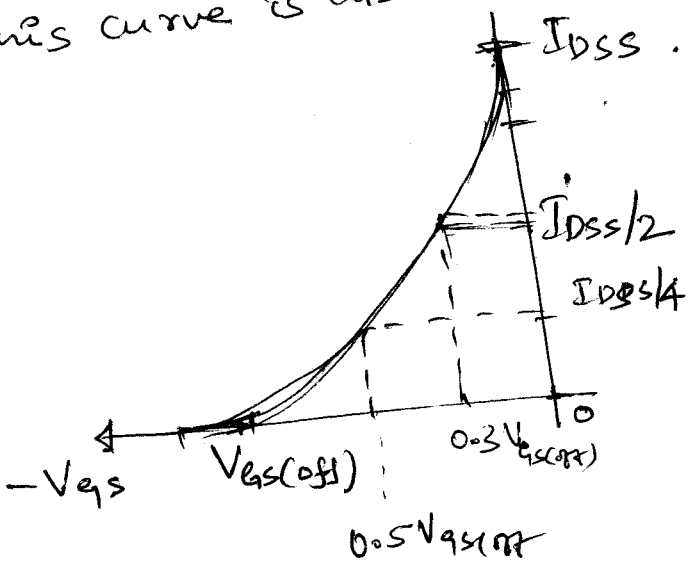


Fig → Transfer characteristic Curve (n-channel).

Observation :

→ Drain current decreases with the increase in negative gate-source bias.

→ Drain current, $I_D = I_{DSS}$ when $V_{GS} = 0$.

→ Drain current $I_D = 0$, when $V_{GS} = V_{GS(off)} = V_P$.

→ Drain current $I_D = I_{DSS}/4$ when $V_{GS} = 0.5\, V_{GS(off)}$

and $I_D = \frac{I_{DSS}}{2}$ when $V_{GS} = 0.3\, V_{GS(off)}$.

The Transfer characteristics curve can also be developed from drain characteristic curve.

This curve can be obtained by plotting values of I_D for the values of V_{GS} taken from the family of drain curves at pinch-off. as shown below in fig for a specific set of curves.

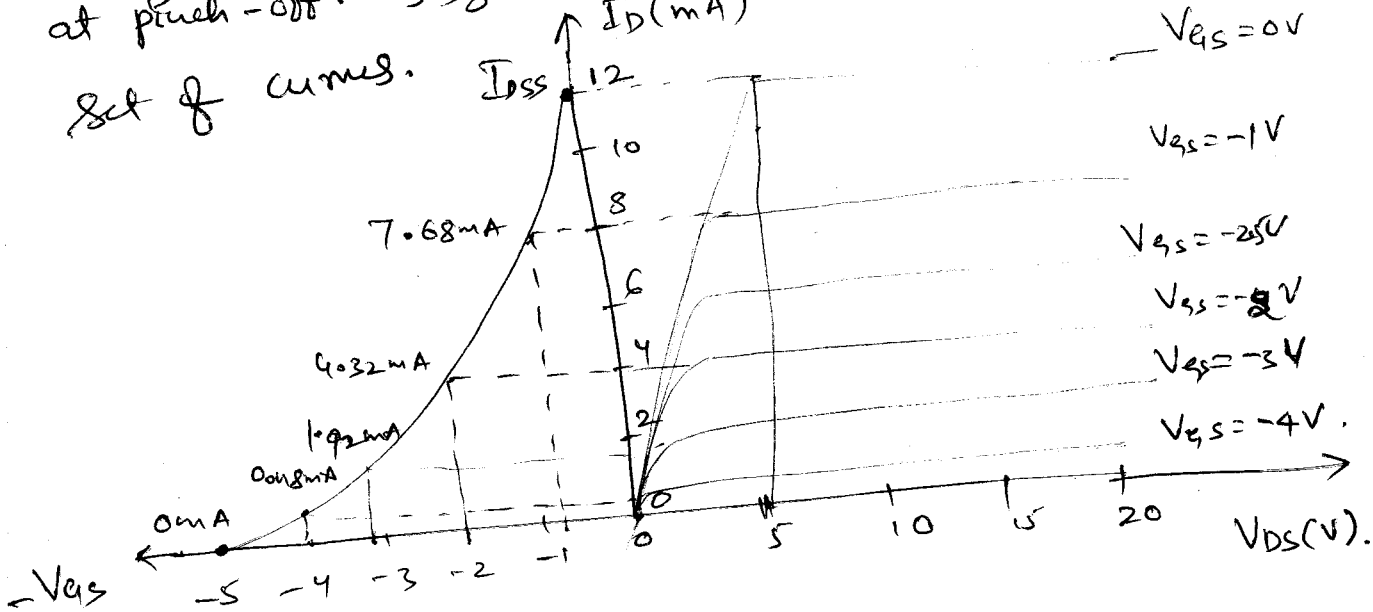


Fig:- Developing Transfer Characteristic curve from Drain characteristic.

The relationship between output drain current I_D and for any negative gate to source voltage V_{GS} in active region is given by Shockley equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Where,

V_{GS} = Applied gate-to source voltage.

I_{DSS} = Drain to source current for short circuit ($V_{GS}=0$) condition.

$V_{GS(off)}$ = Cut off voltage [-ve for n-channel].

V_{GS} = Gate-to source voltage.

Square Law Expression for I_D.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

observe the squared term in the equation, Because of its form, a parabolic relationship is known as a square law, and those JFET's and MOSFET's are called as square-law devices.

JFET Forward Transconductance

The Forward Transconductance (Transfer Conductance, g_m is the change in drain current (ΔI_D) for a given change in ~~drain current~~ Gate to source voltage (ΔV_{GS}) with drain-to-source voltage constant.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad \text{Siemens (S). or mho.}$$

$g_m = g_{fs} = Y_{fs}$ = forward transfer admitance.

important factor in determining the voltage gain of FET amplifier.

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

where

$$g_{mo} = \frac{2 I_{DSS}}{|V_{GS(off)}|}$$

Input resistance :-

JFET operates with its gate source junction reverse-biased, which makes the input resistance at gate very high. It is advantage for JFET.

$$R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right|$$

Where I_{GSS} → gate reverse current.

Input Capacitance Ciss

It is a result of the JFET operating with a reverse-biased pn junction.

A reverse biased pn junction acts as a capacitor whose capacitance depends on the amount of reverse voltage.

AC-Drain to Source Voltage

In Drain characteristics we know that, above pinch-off, the drain current is relatively constant over a range of drain-to-source voltages. Therefore, a large change in V_{DS} produces only a very small change in I_D. The ratio of these changes is the ac drain-to-source resistance of the device r_{ds}'.

$$r_{ds}' = \frac{\Delta V_{DS}}{\Delta I_D}$$

$$r_{ds}' = \frac{1}{g_{os}} = \frac{1}{Y_{os}} =$$

This parameter also specified by the term output conductance or output admittance Y_{os}.

P1 For the typical JFET characteristics curve, Calculate the ac drain-to-source resistance for a JEFT biased at the origin if $V_{GS} = -2\,V$. given $I_{DSS} = 2.5$ mA and $V_{GS(off)} = -4\,V$.

Solution:

The transconductance for $V_{GS} = 0\,V$

$$g_{mo} = \frac{2 I_{DSS}}{|(V_{GS(off)})|} = \frac{2(2.5mA)}{|-4.0|} = 1.25\,mS$$

g_m at $V_{GS} = -2\,V$

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

$$= 1.25mS\left[1 - \frac{-2\,V}{-4\,V}\right]$$

$$= 0.625\,mS$$

The ac drain-to-source resistance of the JFET is the reciprocal of the transconductance.

$$r_{ds}' = \frac{1}{g_m} = \frac{1}{0.625\,mS} = 1.6\,K\Omega.$$

P(2): For an N-channel JFET, $I_{DSS} = 8.7mA$, $V_P = 3\,V$ $V_{GS} = 1\,V$, Find the value of I_D.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$= 8.7mA\left[1 - \frac{-1\,V}{-3\,V}\right]^2 = 3.87mA.$$

P③: For an JFET, $I_{DSS} = 9mA$ and $V_p = -8V$, using these values, determine the drain current for $V_{GS} = 0V, -1$ and $-4V$.

Given Data: $I_{DSS} = 9mA$, $V_p = -8V$.

$I_D = ?$ for $V_{GS} = 0V, -1$ & $-4V$.

Drain current is given by

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

(i) For $V_{GS} = 0V$.

$$I_D = I_{DSS} = 9mA.$$

(ii) For $V_{GS} = -1V$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 = 9mA\left[1 - \frac{-1V}{-8V}\right]^2$$

$$= 9mA\left[1 - 0.125\right]^2$$

$$= 9mA\,(0.766) = \underline{6.89mA}.$$

(iii) For $V_{GS} = -4V$.

$$I_D = 9mA\left[1 - \frac{-4V}{-8V}\right]^2$$

$$= 9mA(1 - 0.5)^2 =$$

$$= 9mA * 0.25$$

$$I_D = 2.25mA.$$

P(4) For an 2N5459 JFET typical values of $I_{DSS} = 9mA$ and $V_{GS(off)} = -8V$ (maximum). Determine the drain current for $V_{GS} = 0$, & $-5V$.

Solution: given data; $I_{DSS} = 9mA$ $V_{GS(off)} = -8V$

Case ① For $V_{GS} = 0$.

$$I_D = I_{DSS} = 9mA.$$

Case ② For $V_{GS} = -5V$.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 9mA\left(1 - \frac{-5V}{-8V}\right)^2$$

$$= 9mA\,(1 - 0.625)^2$$

$$= 9mA\,(0.375)^2$$

$$\boxed{I_D = 1.265625\,mA}$$

P(5). A JFET is operated at Q-point $I_{DQ} = 4mA$ & $V_{GSQ} = -3V$. Determine I_{DSS} if $V_P = -6V$.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_{DSS} = \frac{I_D}{\left(1 - \frac{V_{GS}}{V_P}\right)^2} = \frac{4mA}{\left(1 - \frac{-3}{-6}\right)^2} = \frac{4mA}{0.25}$$

$$\boxed{I_{DSS} = 16mA}$$

P⑥: For an N-channel JFET, $I_{DSS} = 8\,mA$; $V_P = -5V$

Determine (i) I_D at $V_{GS} = -2V$ and $-3V$

(ii) V_{GS} at $I_D = 3\,mA$ and $5\,mA$.

Solution:-

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

(i) I_D at $V_{GS} = -2V$

$$I_D = I_{DSS}\left(1 - \frac{-2}{-5}\right)^2$$

$$= 8mA\left(1 - 0.4\right)^2$$

$$= 8mA * 0.36$$

$$= 2.88mA.$$

$V_{GS} = -3V$

$$I_D = 8mA\left(1 - \frac{-3}{-5}\right)^2$$

$$= 8mA\left(1 - 0.6\right)^2$$

$$= 8mA * 0.16$$

$$= 1.28mA$$

$$\boxed{I_D = 1.28mA}$$

(ii). For $I_D = 3mA$

$$3 = 8\left(1 - \frac{V_{GS}}{(-5)}\right)^2$$

$$3 = 8\left(1 + 0.2V_{GS}\right)^2$$

$$1 + 0.2V_{GS} = \sqrt{\frac{3}{8}}$$

$$1 + 0.2V_{GS} = \pm 0.6123$$

$$V_{GS} = -1.94V \text{ \& } -8.06V$$

$-8.06V$ is neglected as it is greater than V_P.

$$\therefore V_{GS} = -1.94V.$$

For $I_D = 5mA$.

$$5 = 8\left(1 - \frac{V_{GS}}{(-5)}\right)^2$$

$$5 = 8\left(1 + 0.2V_{GS}\right)^2$$

$$1 + 0.2V_{GS} = \pm 0.7905$$

$$V_{GS} = -1.05V \text{ \& } -8.95V$$

$-8.95V$ is neglected as it is greater than V_P

$$\therefore V_{GS} = -1.05V$$

(7) In the JFET ckt shown, determine, the minimum value of V_{DD} required to put the device in the pinch off region. given that at $V_p = -4V$. $I_{DSS} = 12mA$.

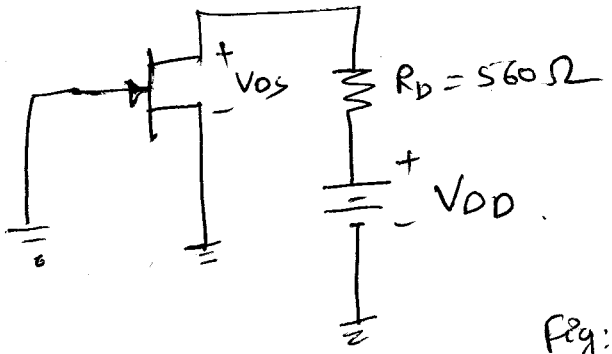


Fig:-

Solution:

In Fig.

We observed that $V_{GS} = 0V$

In pinch-off region with $V_{GS} = 0V$. we have.

$$I_D = I_{DSS} = 12mA.$$

The minimum value of V_{DS} for the JFET to be in its pinch-off region is $V_{DS} = V_p = 4V$.

Apply KVL to the output side

$$V_{DD} = I_D R_D + V_{DS}$$

$$= (12m)(560) + 4 = 10.72V.$$

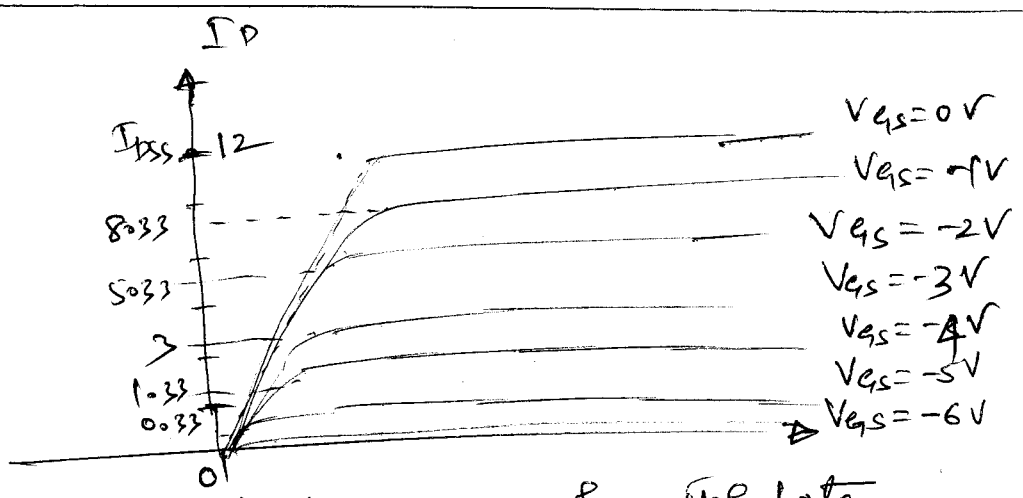
This is the minimum value of V_{DD} required to make $V_{DS} = V_p = 4V$, i.e to put the device in the pinch-off region.

(8): Find the transfer characteristics values of N-channel JFET. Given that $I_{DSS} = 12mA$ & $V_p = -6V$.

Soln:- we have $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

V_{GS} (V)	I_D (mA).
0	12
−1	8.33
−2	5.33
−3	3
−4	1.33
−5	0.33
−6	0

Then draw the graph.



Drain characteristic curve from the data calculated before.

(1) $V_{GS}=0V$. $\quad I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$

$= (12mA)\left(1-\frac{0}{-6}\right)^2$

$\boxed{I_D = 12mA}$

$V_{GS}=-1V$ $\quad I_D = (12mA)\left(1-\frac{-1}{-6}\right)^2$

$\boxed{I_D = 8.33mA}$

$-2V$ $\quad I_D = (12mA)\left(1-\frac{-2}{-6}\right)^2$

$\boxed{I_D = 5.33mA}$

$-3V$ $\quad I_D = (12mA)\left(1-\frac{-3}{-6}\right)^2$

$\boxed{I_D = 3mA}$

$-4V$. $\quad I_D = (12mA)\left(1-\frac{-4}{-6}\right)^2$

$\boxed{I_D = 1.33mA}$

$-5V$ $\quad I_D = (12mA)\left(1-\frac{-5}{-6}\right)^2$

$\boxed{I_D = 0.33mA}$

$-6V$ $\quad I_D = (12mA)\left(1-\frac{-6}{-6}\right)^2$

$\boxed{I_D = 0.mA}$.

MOSFET :

MOSFET stands for metal oxide semiconductor field effect transistor.

MOSFET has three terminal, Source, Gate & Drain.

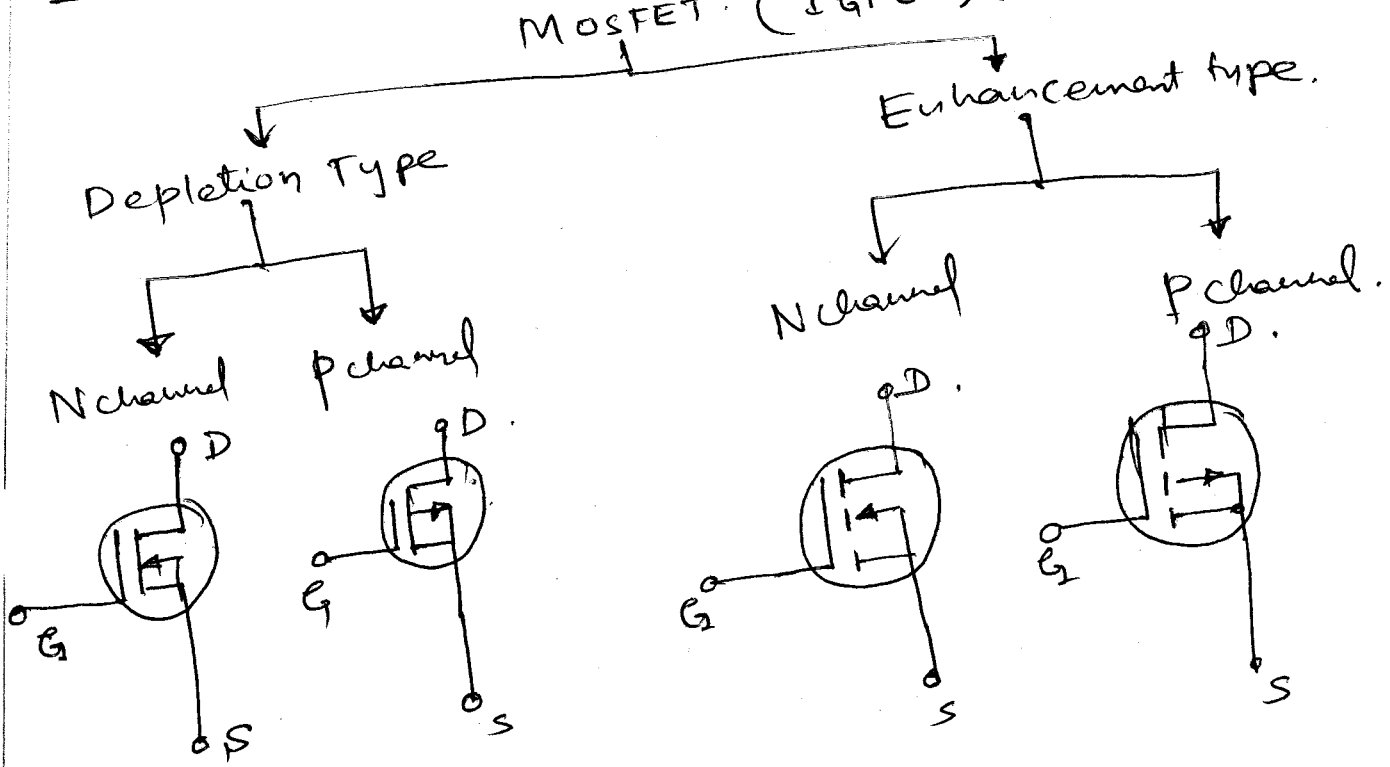
In MOSFET, the gate is insulated from the channel. But not in FET. Because of insulated gate, the gate current is even smaller than it is in a FET.

MOSFET is also called as insulated gate field effect transistor (IGFET). (or Insulated gate FETs).

MOSFET's are used in VLSI circuits such as microprocessors and semiconductor memories.

VLSI - Very large scale Integration.

Types of MOSFET



Basically two types

(1) Enhancement type MOSFET (normally-off).

(2) Depletion type MOSFET. (normally-ON).

Enhancement MOSFET

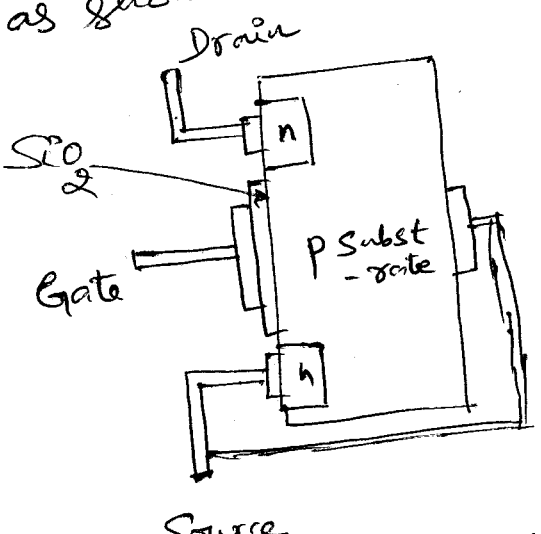
Construction:

The E-MOSFET operates only in the enhancement mode and has no depletion mode.

E-MOSFET has no structural channel.

Figure 1(a) shows the basic structure of the N-channel E-MOSFET.

In E-MOSFET, the substrate extends completely to the SiO_2 layer. For an n-channel device, a positive gate voltage above a threshold value induces a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer as shown in figure 1(b).



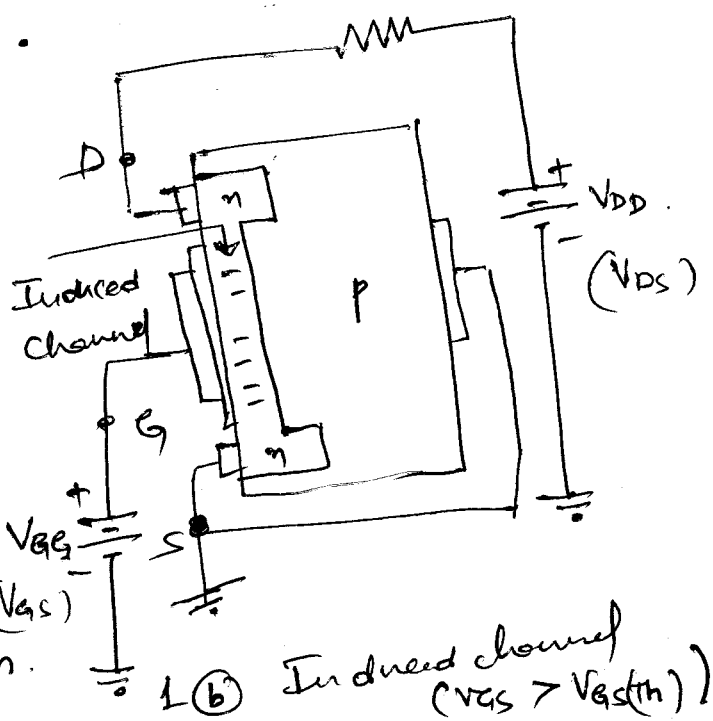


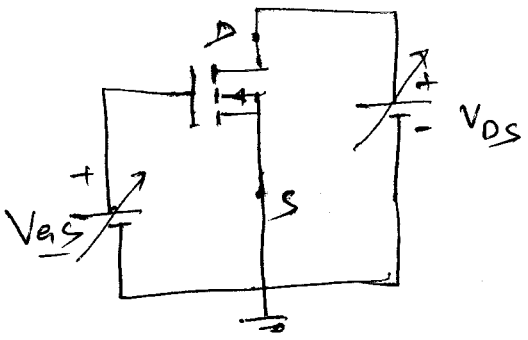
Fig. 1(a) Basic Construction. 1(b) Induced channel ($V_{GS} > V_{GS(th)}$)

The conductivity of the channel is enhanced by increasing the gate-to-source voltage, and thus pulling more electrons into the channel area.

Operation:-

Circuit Connection for E-MOSFET is shown in figure ③.

If some positive voltage is applied at the gate, it induces a negative charge in the p-type substrate adjacent to the silicon dioxide layer.



Fig③ Circuit connection

- The induced negative charge is produced by attracting the free electrons from the source.
- when the gate is positive enough, it can attract a number of free electrons and forms a thin layer, which stretches from source to drain.
- This layer of free electrons is called N-type inversion layer.
- The minimum gate-to-source voltage (V_{GS}) produces inversion layer is called as threshold voltage $V_{GS(TH)}$
- When $V_{GS} < V_{GS(TH)}$. $I_D = 0A$.
- when $V_{GS} > V_{GS(TH)}$. Inversion layer connects Drain & source we get I_D.

$$I_D = K\left(V_{GS} - V_{GS(TH)}\right)^2.$$

The relation ship between V_{DS} and V_{GS} is given by

$$V_{DS} = V_{GS(ON)} - V_{GS(TH)}.$$

Figure ④ shows the transconductance characteristics It is a graph of Input gate-to-source voltage (V_{GS}) and output drain current I_D.

For any gate voltage below the threshold value, there is no channel.

- E-MOSFET are called as "Normal-OFF state devices.
- The channel between Drain & Source is absent.
- The minimum voltage required to turn-ON MOSFET is called as "Threshold Voltage" $V_{GS(TH)}$.

The schematic symbol of n-channel & p-channel E-MOSFET's are shown in figure ②. The broken lines symbolize the absence of physical channel.

- An inward-pointing substrate arrow is for n-channel, & an outward pointing arrow for p channel.

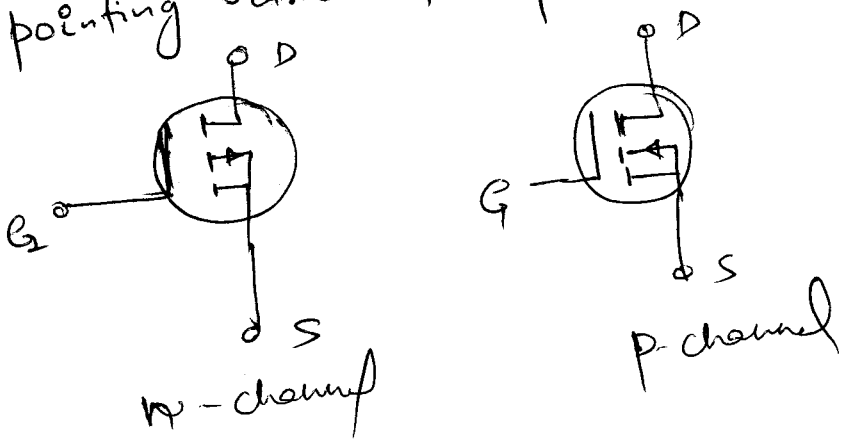


Fig ②. Symbol of E-MOSFET.

Here substrate is always shorted to source.

- For $V_{GS} > V_{GS(TH)}$, the drain current is given by the modified shockley equation.

$$I_D = K\left(V_{GS} - V_{TH}\right)^2$$

where $K = \text{Constant} = \dfrac{I_{D(ON)}}{\left(V_{GS(ON)} - V_{GS(TH)}\right)^2}$

V_{GS} = ON state gate-source voltage
$V_{GS(TH)}$ = Threshold Voltage of N-MOSFET.

- It is observed that, until $V_{GS} = V_{TH}$, there is no-drain current, EMOSFET operates in cut-off mode (open switch).

- When $V_{GS} > V_{TH}$, the channel is created and it becomes ON. This region of operation is called as Enhancement mode operation. i.e, as V_{GS} increases, output current I_D also increases depending upon the Drain current equation.

$$I_D = K \cdot (V_{GS} - V_{GS(TH)})^2.$$

Figure (5) shows the output characteristics of EMOSFET. It is a graph of output voltage (V_{DS}) and drain current (I_D) for a constant Gate-to Source voltage ($V_{GS} > V_{GS(TH)}$).

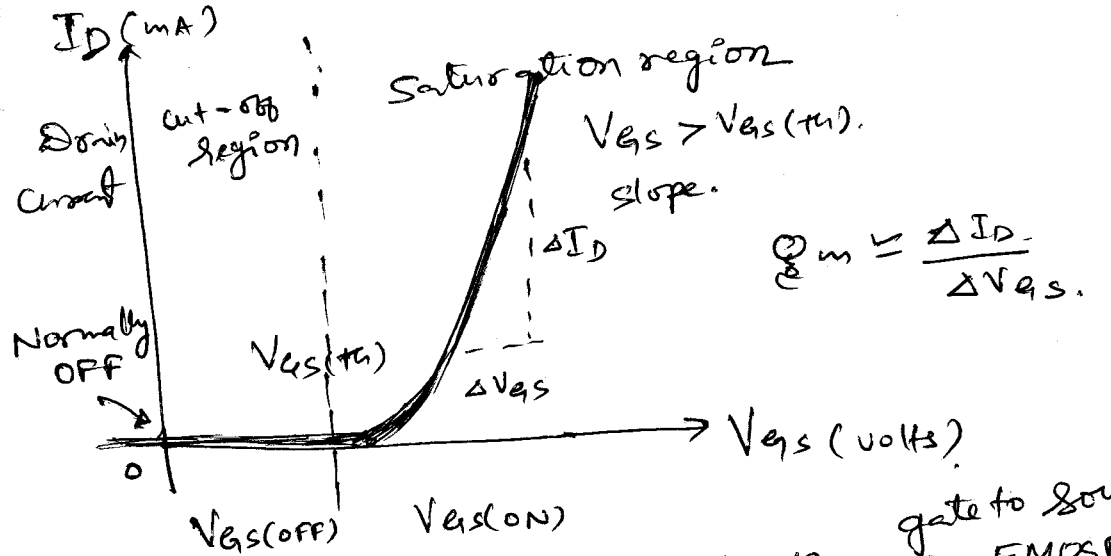


Fig (4). Transfer characteristics of gate to Source voltage of EMOSFET.

$V_{GS4} > V_{GS3} > V_{GS2} > V_{TH}$

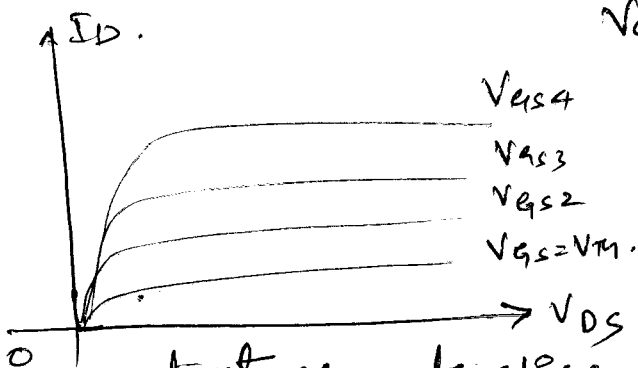


Fig (5): output characteristics.

p-channel EMOSFET

The construction of a p-channel EMOSFET is the reverse process of N-channel EMOSFET. i.e. here is now n-type substrate and p-doped regions under the drain and source connections.

- The terminals same as n-type EMOSFET. but all the voltage polarities & the current directions are reversed.

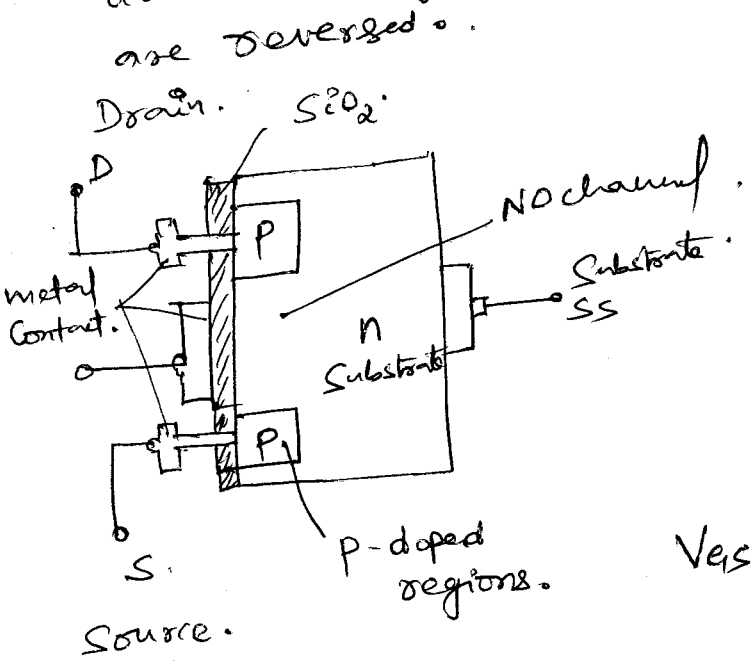


Fig 6(a) P-channel EMOSFET

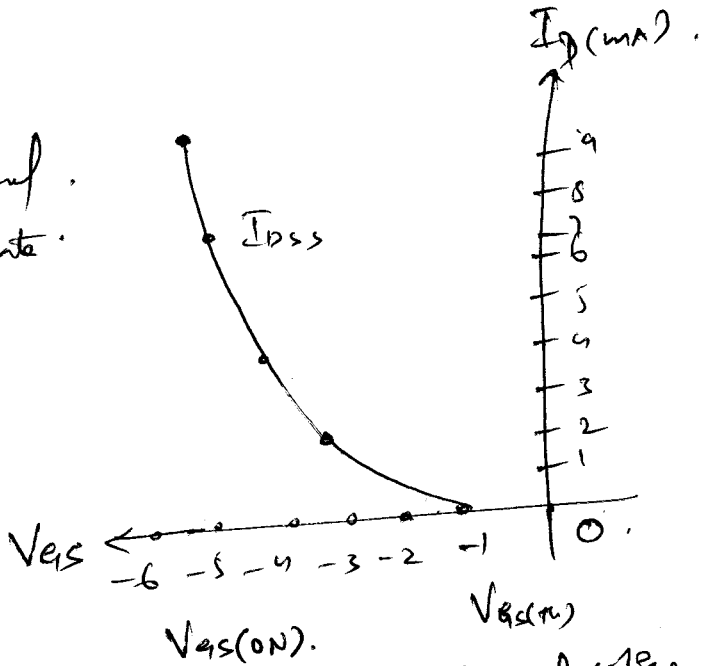


Fig (6b) Transfer characteristics

Construction of p-channel EMOSFET is shown in fig 6(a). Substrate and Source are shorted here. the Trans Conductance / Transfer characteristics are plotted in figure 6(b).

Depletion Type MOSFET : Constration.

- Another type of MOSFET is the depletion MOSFET.
- A physical channel is constructed between source & Drain.

Figure (7) shows the Basic structure of n-channel and p-channel DMOSFET.

→ The drain & source are diffused into the substrate material & then connected by a narrow channel adjacent to the insulated gate.

→ A DMOSFET N-channel device constration is explained below. A slab of p-type material is formed from a silicon base and referred to as the substrate.

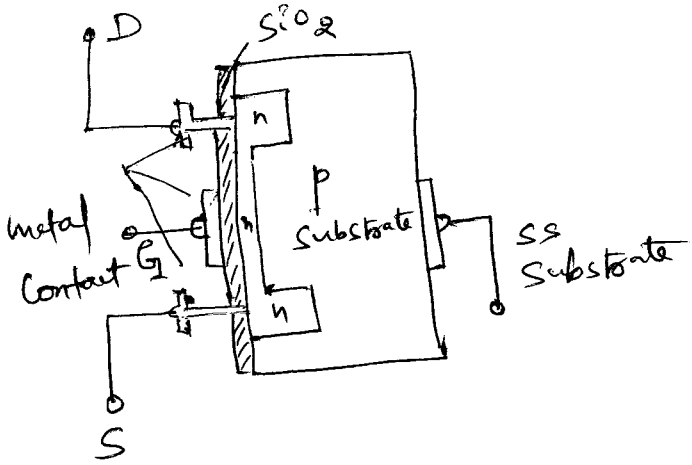
→ The source and Drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in figure (7) a

→ The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin SiO_2 layer.

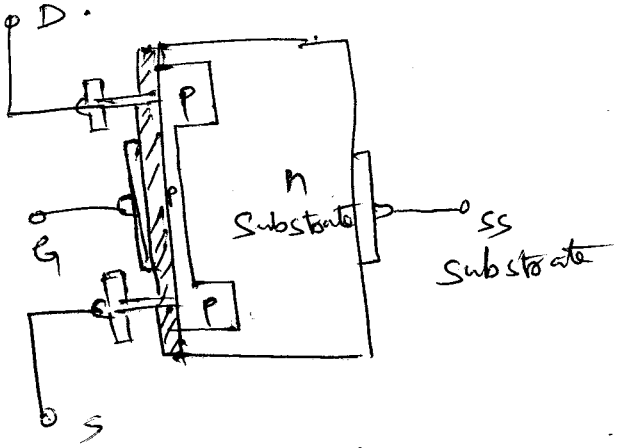
→ No electrical connection between the gate terminal and the channel of MOSFET.

→ SiO_2 layer in MOSFET accounts for very high desirable high input impedance of the device.

→ If entire structure acts as paralleled plate capacitors, then gate is one end and other by semiconductor channel. then plated is seperated by a dielectric (SiO_2) layer.



#(a) N-channel DMOSFET



#(b) p-channel DMOSFET

Operation :-

The DMOSFET can be operated in TWO modes.

(1) Depletion mode

(2) Enhancement mode.

It is also called as Depletion/Enhancement MOSFET.

- Since the gate is insulated from the channel, either a positive or negative gate voltage can be applied.
- When V_{GS} applied is negative N-channel MOSFET operates in depletion mode
- When V_{GS} applied is positive, then MOSFET operates in Enhancement mode.

→ They are generally operated in depletion mode

Depletion mode :-

The device operates in this mode, when gate voltage is zero or negative.

Fig 8 shows MOSFET with a negative gate to source voltage.

⇒ The negative voltage on gate, induces a positive charge in the channel.

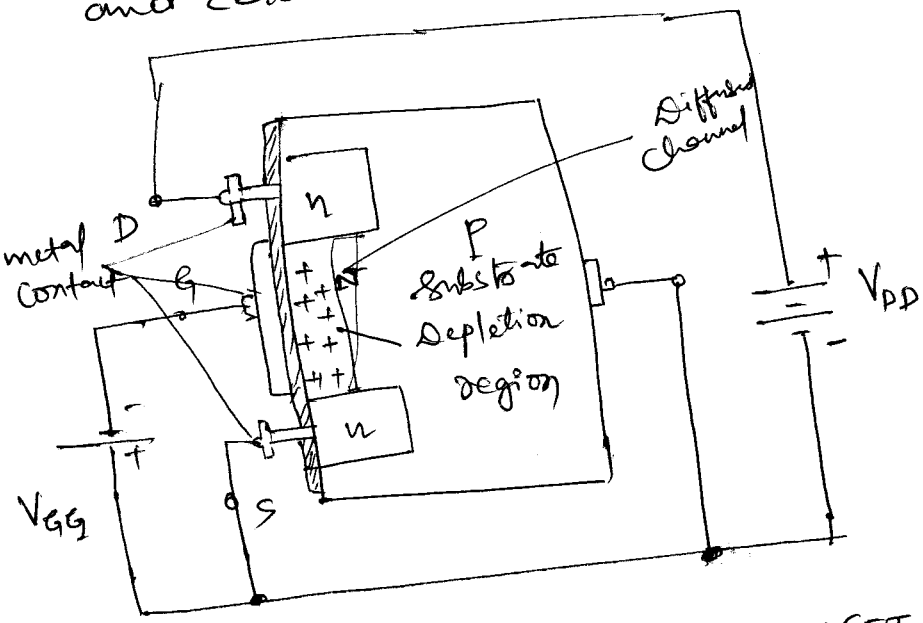
⇒ Because of this negative voltage, electrons in the vicinity of positive charge are repelled away in the channel.

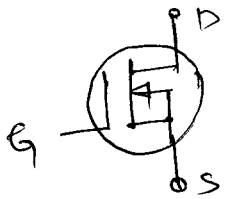
⇒ As a result of this, the channel is depleted of free electrons and Reduces the electrons resulting in the reduction of drain current I_D.

⇒ If $-V_{GS}$ increases means then I_D decreases.

⇒ At a sufficiently negative V_{GS} voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero.

⇒ Like n-channel JFET, the n-channel D-MOSFET conducts drain current for gate-to-source voltages between $V_{GS(off)}$ and zero.





Depletion MOSFET Symbol

Figure ⑧ Depletion type MOSFET. with $V_{GS} \leq 0$. & applied voltage V_{DD}.

Figure 8 N channel MOSFET of depletion type. It offers very high input resistance. (about 10^{10} to 10^{15}). Significant current flows for given V_{DS} at V_{GS} of 0 volt.

when gate (i.e one plate of capacitor) is made positive, the channel (i.e the other plate of capacitor) will have positive charge induced in it.

Figure (9) shows the drain characteristic for the N-channel depletion type MOSFET in the common source configuration. These curves are plotted for both negative and positive values of gate to source voltage (V_{GS}). The curves for $V_{GS} \leq 0$, MOSFET operates in the depletion mode. If $V_{GS} > 0$, the MOSFET operates in Enhancement mode.

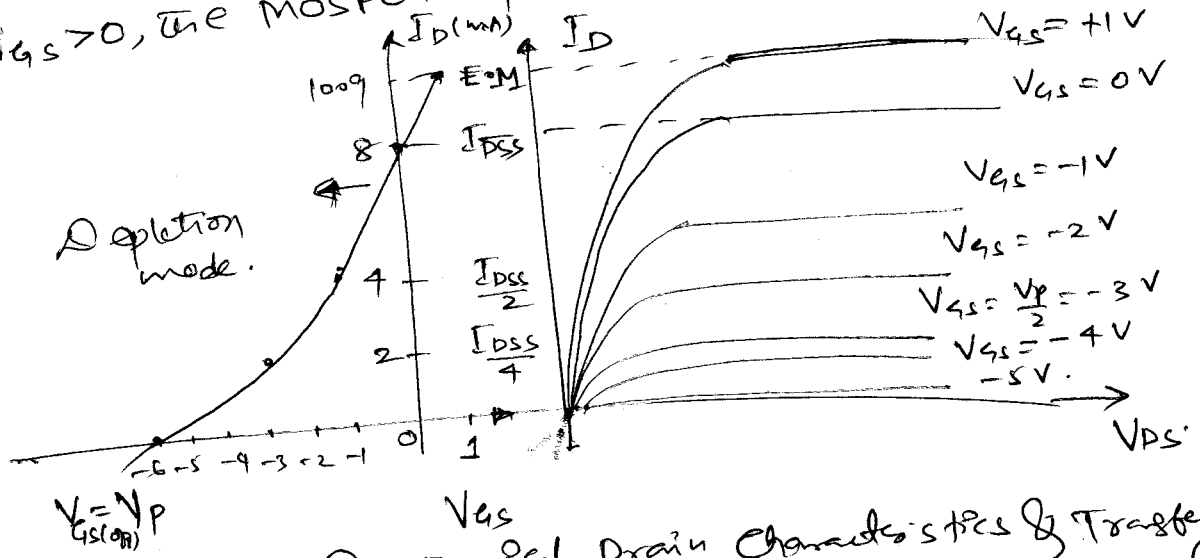
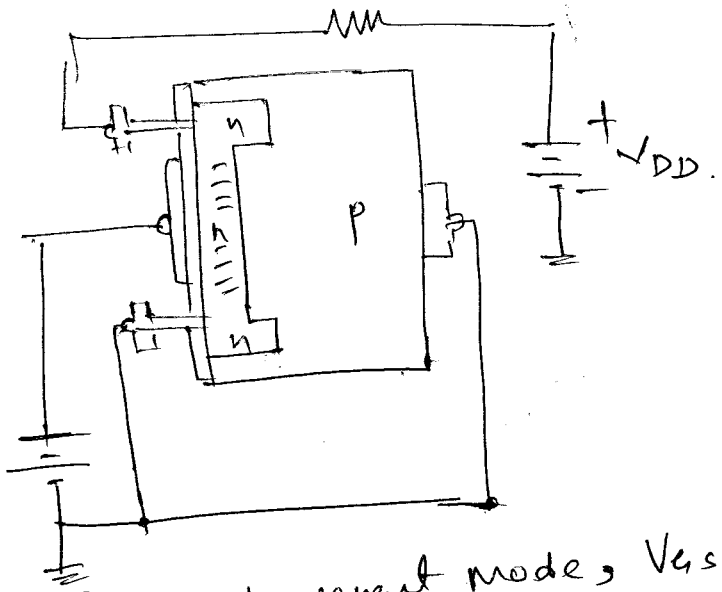


Figure (9). Typical Drain Characteristics & Transfer Characteristics for an n-channel depletion-type MOSFET.

Note:
EM-Enhancement mode

Enhancement mode:-

- MOSFET operates in this mode, when the gate voltage is positive as shown in figure (10).
- The positive gate voltage increases the number of free electrons passing through the channel. The greater the gate voltage, greater is the number of free electrons passing through the channel.



- This increases, ie enhances the conduction in the channel. Because of this fact, positive gate operation is called Enhancement.

Fig (10). Enhancement mode, V_{GS} positive.

As V_{GS} is made greater than zero ($V_{GS} > 0$), the current increases from I_{DSS} & becomes more positive constituting the positive drain current I_D. as shown in figure (9).

The depletion-MOSFET can conduct even if the V_{GS} is zero. Because of this it is also called as Normally ON MOSFET.

The Drain current is given by.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

where.

I_{DSS} →

V_{GS} →

$V_{GS(TH)}$ →

P(1): Draw the transfer and drain characteristics for an n-channel depletion-type MOSFET for the ranges of values $V_{GS} = -6V$ to $+1V$ with $I_{DSS} = 8mA$

Soln:- For depletion mode of operation, the drain current =

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

when $V_{GS} = -6$, $I_D = 8m\left(1 - \frac{-6}{-6}\right)^2 \cdot 1 = 0$.

$V_{GS} = -5$, $I_D = 8\times10^{-3}\left(1 - \frac{-5}{-6}\right)^2 = 0.2mA$

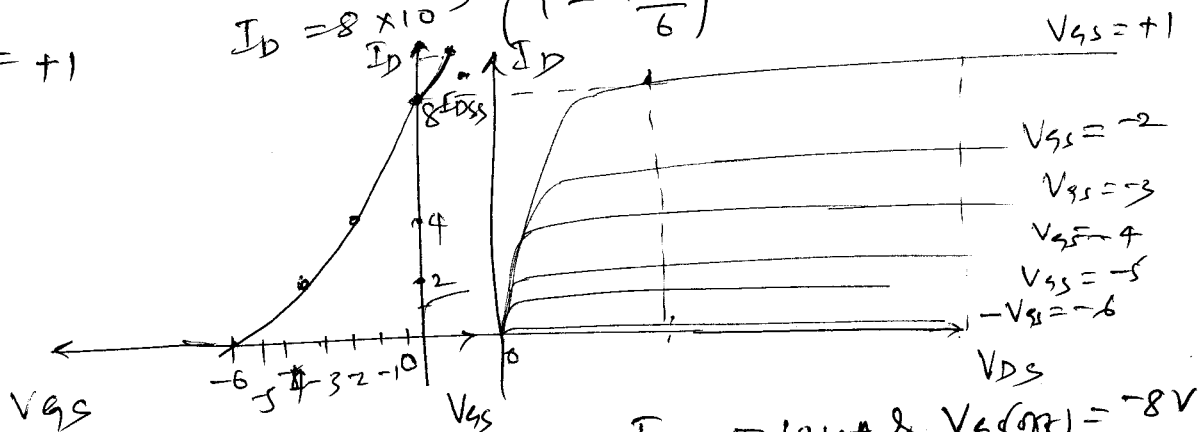
$V_{GS} = -4$, $I_D = 8\times10^{-3}\left(1 - \frac{-4}{-6}\right)^2 = 0.88mA$.

$V_{GS} = -3$ $I_D = 8\times10^{-3}\left(1 - \frac{-3}{-6}\right)^2 = 2mA$

$V_{GS} = -2$ $I_D = 8\times10^{-3}\left(1 - \frac{-2}{-6}\right)^2 = 3.55mA$

$V_{GS} = -1$ $I_D = 8\times10^{-3}\left(1 - \frac{-1}{-6}\right)^2 = 5.55mA$

$V_{GS} = +1$ $I_D = 8\times10^{-3}\left(1 - \frac{+1}{6}\right)^2 = 10.9mA$.



P(2). For an certain D-MOSFET, $I_{DSS} = 10mA$ & $V_{GS(off)} = -8V$

(a) Is it an n-channel or a p-channel

(b) Calculate the I_D at $V_{GS} = -3V$

(c) Calculate the I_D at $V_{GS} = -3V$.

Soln: (a) The device has a negative $V_{GS(off)}$, therefore, it is an n-channel MOSFET.

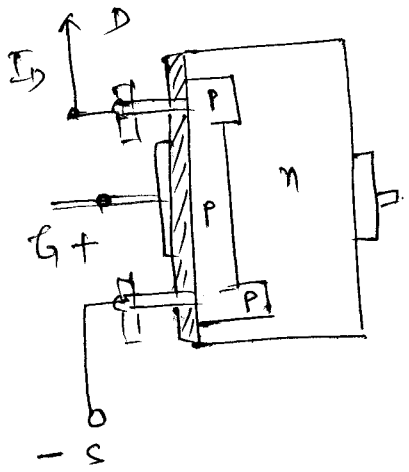
(b) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = 10mA\left(1 - \frac{-3V}{-8V}\right)^2 = 3.91mA$

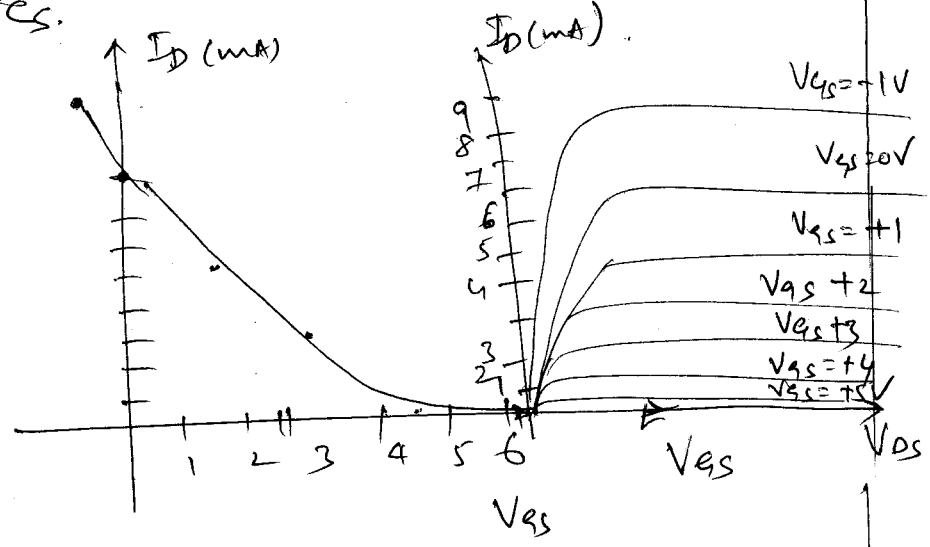
(c) $I_D = (10mA)\left(1 - \frac{+3}{-8}\right)^2 = 18.9mA$.

P-channel Depletion type MOSFET

The construction is exactly reverse of N-channel DMOSFET. Here n-type substrate and a p-type channel. The construction shown below.

P channel Depletion type MOSFET & typical Drain ~~and~~ transfer characteristics.





Comparision:-

Transfer characteristics

$V_{GS} = V_P = +6V$. Drain characteristics

Sl No.	FET	MOSFET	BJT.
1.	unipolar transistor	unipolar transistor	Bipolar transistor.
2.	High input impedance.	Comparatively higher than FET	Low input impedance.
3.	It is three terminal semiconductor device has Gate, source & Drain terminal	It has three terminal, Gate, source & Drain	It is also three terminal semiconductor device has, Base emitter & Collector.
4.	Gate must be reverse biased for proper operation	MOSFET may be Connected in Enhancement mode. that means that the device is not restricted to operating with its gate reverse biased.	Input Limit must be Connected in forward biased
5.	Voltage driven device	voltage driven device	Current driven device
6.	Noise level is small	. Noise level is small	Comparatively more Noise than a FET.

CMOS Circuits

CMOS is a full form of complementary metal oxide semiconductor. CMOS is constructed using complementary & symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (CMOSFETs) for logic functions.

Here the two gates are connected to form the input terminal and two drains are connected to form the output terminal as shown in figure 1(a). The CMOS circuit offers two advantages:

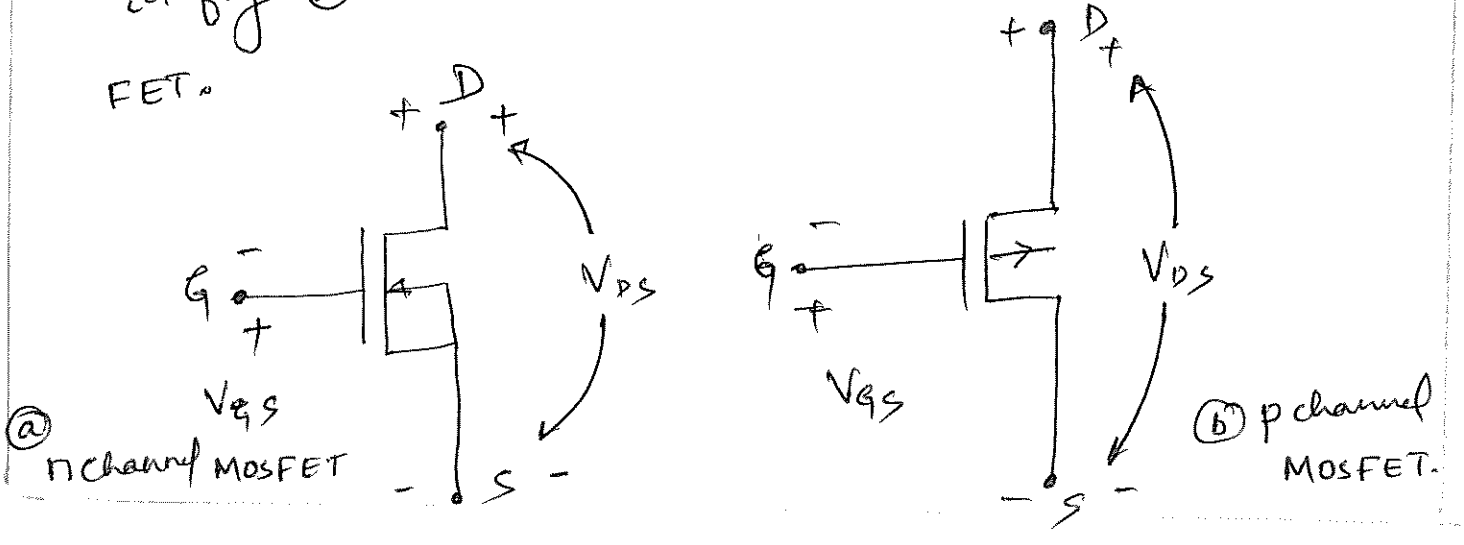
1. The drain current is very low and flows mainly during transistion from one state to the other (ON/OFF).

2. The power drawn in steady state is extremely small.

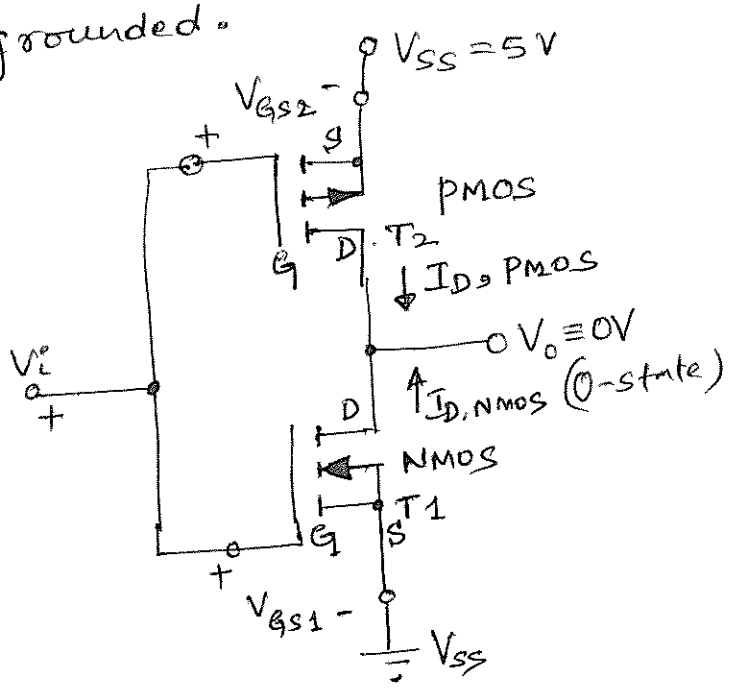
These two advantages, gained great popularity in digital circuits. Also used in Analog Circuit.

CMOS Application in Digital circuit :-

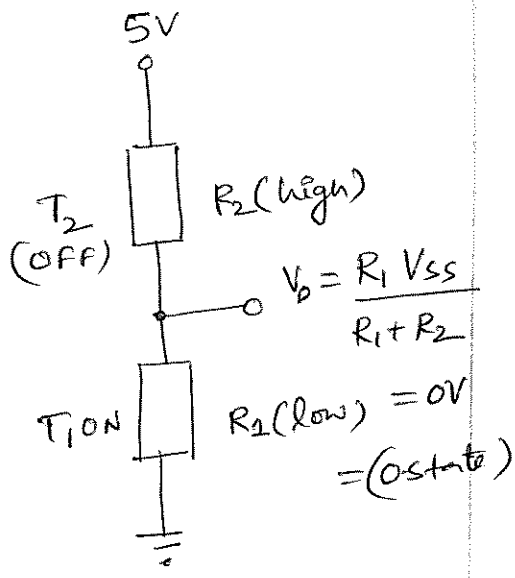
The one application is CMOS Inverter as shown in fig (2). The Digital Inverter used by nMOS & pMOS FET.



The source terminal of PMOS (T_2) is connected to $V_{SS} = 5V$, while the source terminal of NMOS(T_1) is grounded.



(a) CMOS inverter



(b) Equivalent circuit for $V_i = 5V$, state 1.

Fig: CMOS digital inverter

operation

when $V_i = 5V \Rightarrow$ 1 state

$V_{GS2} = 5 - 5 = 0V$ In this case T_2(pmos) is non conducting, OFF (ie V_T is negative, draws only leakage current, offers high resistance (R_2)

$V_{GS1} = 5V > V_T$.

T_1(nmos) is Conducting, ON, offers very low resistance (R_1). The equivalent circuit of CMOS digital inverter is shown in fig 2(b).

Output $V_o = 0$

$= 0$ - state.

From Fig 2 (b).

$$V_o = V_{ss} \cdot \frac{R_1}{R_1 + R_2}. \quad \text{because } R_1 = 0.$$

$$\simeq 0\ V.$$

For $V_i = 0$ Input $\Rightarrow$ state - 0.

$V_{GS2} = -5\ V$, T_2 Conducting (Low resistance)

$V_{GS1} = 0V$, T_1 nonconducting (High resistance)

output

$V_o = 5V \Rightarrow 1$-state.

We thus see that the ckt acts as an inverter, 1-state input produces 0-state output and 0-state produces 1-state output.

Here only one transistor is turned on in any of the output state. Here the transistors are connected in series, no current is drawn from the battery source in either of the two states.

only during state transition, the current is drawn from the battery. CMOS ckts draw extremely low power from the battery source and so their energy Consumption is very small. Hence the CMOS are used in digital application.

—o—

Silicon Controlled Rectifier (SCR) -

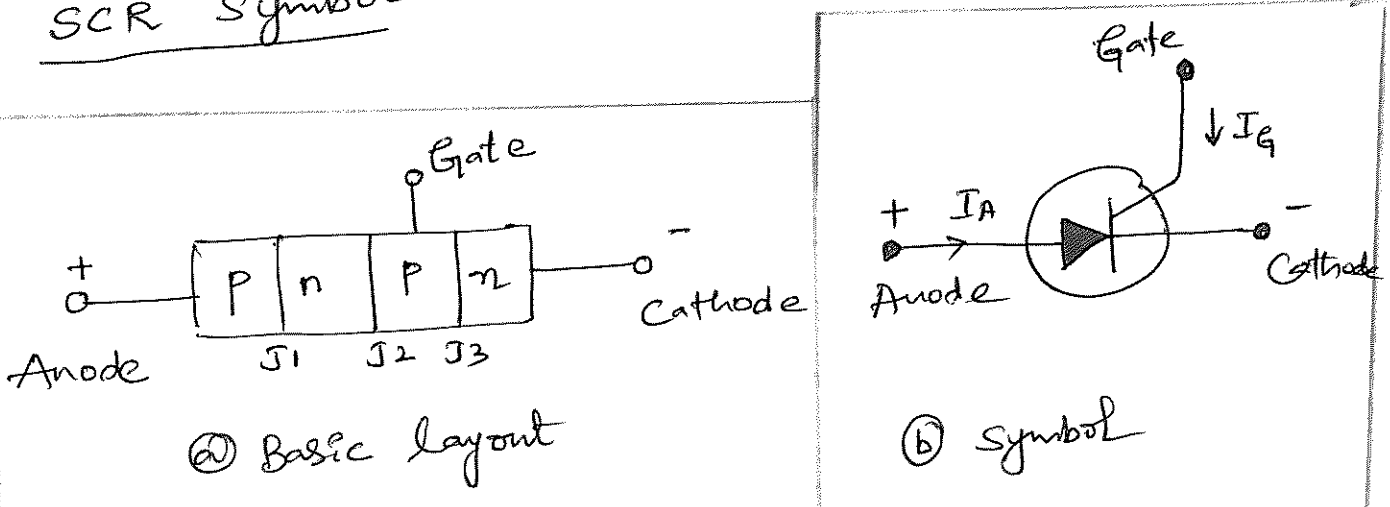
A silicon controlled Rectifier is a Four layer solid - state current controlling device.
It is also called as Semiconductor Controlled rectifier.

SCR along with associated circuitry has wide applications as.

>> Rectifiers
>> Regulated power supplies
>> dc to ac Conversion (inverters)
>> relay Control and
>> time delay circuits & many more.

SCRs are available to control power as high as 10MW with individual rating of 2KA and 1.8KV. The frequency range of 50KHz, are employed in high frequency applications like induction heating and ultrasonic cleaning.

SCR Symbol



(a) Basic layout (b) Symbol

Fig. 1 Silicon Controlled Rectifier (SCR)

Basic operation

The silicon is the material used for the fabrication of SCR, because of high temperate requirement of handling Large current and power. The Four layer arrangement of SCR is shown in figure 1(a) the "pnpn" structure is shown There are three p-N Junctions labeled J_1, J_2 and J_3 and three terminals namely Gate, Anode and Cathode.

The "anode" terminal of an SCR is Connected to the p-type material of PNPN structure, and the "Cathode" terminal is connected to the n-type layer, while "gate" of the SCR is Connected to the p-type material nearest to the Cathode. The Symbol of SCR is drawn in figure 1(b). The Symbol is similar to diode, the difference is indication of the gate terminal.

The Silicon Control Rectifier start Conduction when it is forward biased. The Forward Voltage is applied across the SCR. The Anode teominal is Connected to positive Supply & Cathode to negative teominal of the Supply. When positive clock pulse is applied at the gate terminal then the SCR turns ON

When SCR Forward biased by applying power supply The Junction J1 and J3 becomes foorward bias while the Junction J2 become reverse bias. when we apply a clock pulse at the gate teominal the Junction J2 becomes foorward bias and the SCR starts Condution.

The SCR turn ON and OFF very quickly. The foorward current Canode to Cathode) is offered a resistance as low as 0.01 to 0.1 Ω. The Dynamic reverse resistance of an SCR is as high as 100K Ω or more

Two transistor Model

Cross sectional view of an SCR with its four layers is shown in figure. 2(a). The middle n and p layers can be imagined to be subdivided into two halves, as shown by the dotted lines.

The SCR is now recognised as the device that Comprises one PNP and one NPN transistor. Here there is an electrical Continuity between the two halves of each of these layers, the base of PNP is Connected to the Collector of NPN; the Collector of PNP is Connected to the base of NPN while the gate is Connected to the base of NPN.

The equivalent two transistor circuit is shown in figure 2(b).

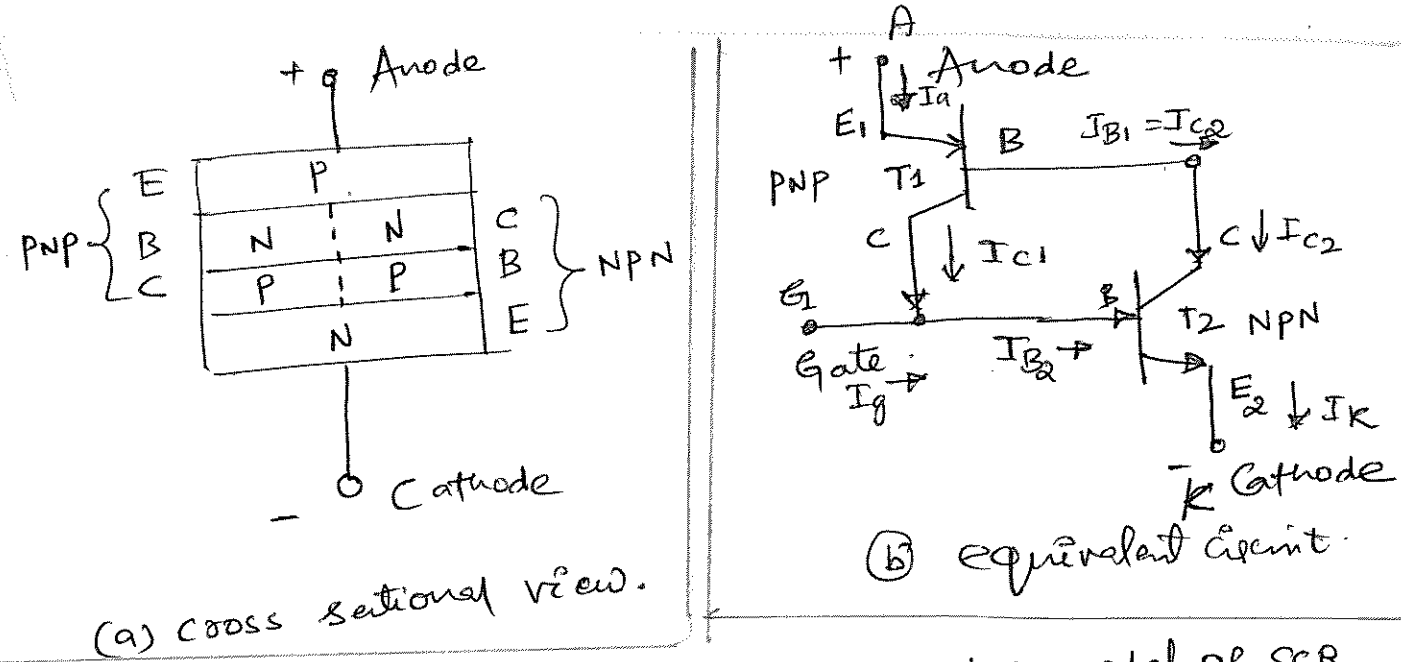


Figure (2). Two-transistor model of SCR.

Figure (2) is used to explain the action of the gate pulse I_G.

Switching Action;

Let a positive voltage V be applied to the anode (E1) and the cathode (E_2) and gate (G) be both grounded as shown in figure 3(a).

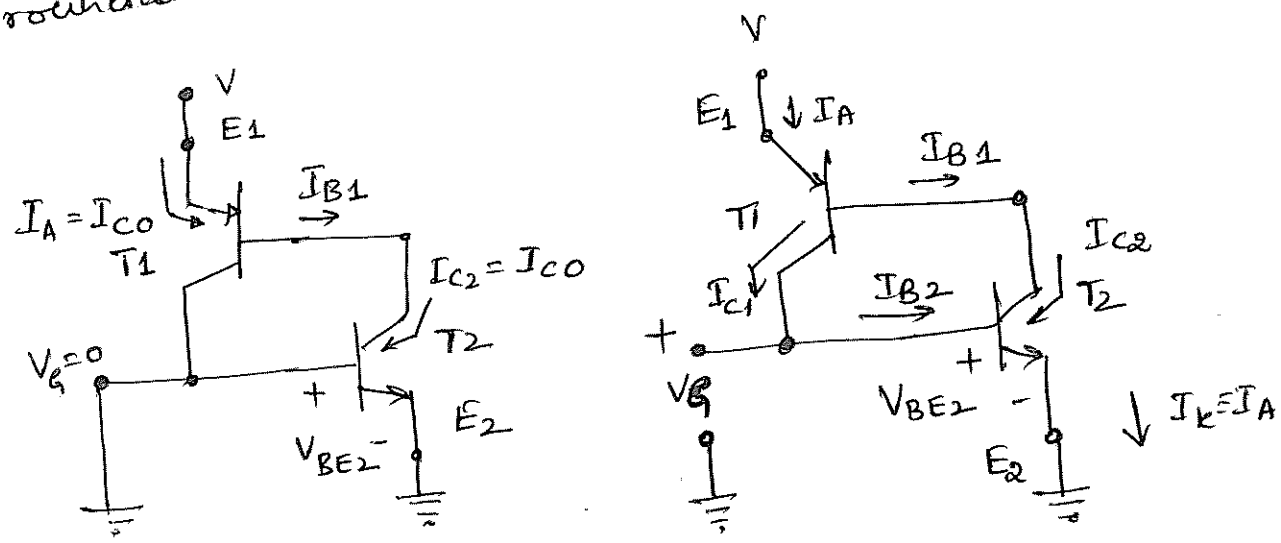


Fig (3) Switching action of a two-transistor SCR.

When $V_G = 0$, then $V_{BE_2} = 0$, The transistor T_2 is in OFF state. It means that CB junction of T_2, through EB Junction of T_1, is reverse biased.

Therefore, $I_{B1} = I_{CO}$ (minority carrier current) is too small to turn-on T_1. Thus both T_1 and T_2 are OFF and so anode current

$$I_A = I_{B1} = I_{CO}.$$

it is of negligible order. It means that SCR is in turn-OFF state, that is the switch between anode (E1) and Cathode (E2) is open.

Apply a voltage $+V_G$ at the gate terminal as shown in figure 3 (b).

As $V_{BE2} = V_G$, upon making V_G sufficiently large, I_{B_2} will cause T_2 to turn on and the Collector Current I_{C_2} becomes large.

As $I_{B1} = I_{C_2}$, T_2 turns on causing a large collector current I_{C1} ($I_A = I_{C1}$) to flow. This in turn, increases I_{B2} causing a regenerative action to set in (a positive internal feedback)

The result is that SCR is turned on, that is, the switch between the anode (E1) and Cathode (E_2) is closed (turn-ON).

The current I_A must be limited by the external circuit say a series resistance between the source & E1.

The turn-on time of an SCR is typically 0.1 to 1 μs.

However for high power devices in the range of 100 - 400A, turn on time may be 10-25 μs.

Turn OFF.

When the SCR is in Conduction mode, the gate is ineffective in turning it OFF.

The SCR turn-off mechanism is called Commutation and it can be achieved in two ways, namely

- Natural Commutation
- Forced Commutation.

The term Commutation means the transfer of current from one path to another. Commutation is the process of turning off a Conducting SCR.

Natural Commutation

Natural Commutation occurs in AC circuits. In AC supply, the current will flow through the zero crossing line while going from positive peak to negative peak. Thus a reverse voltage will appear across the device simultaneously which will turn off the thyristor immediately.

This process is called as Natural Commutation as SCR is turned off naturally without using any external components or circuit for commutation process.

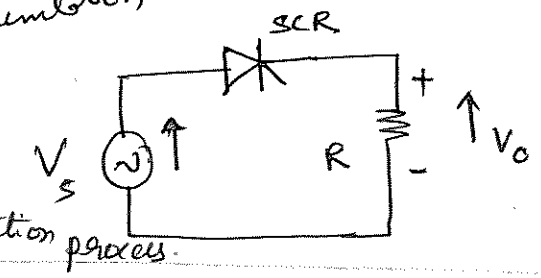


Fig: Natural Commutation process.

Forced Commutation

It is applied to DC circuits. Forced Commutation is achieved by reverse biasing SCR device or by reducing SCR Current below the holding current value.

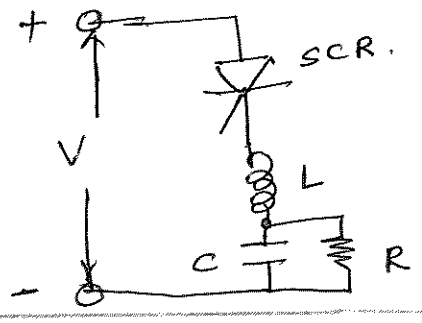
External circuit is used for forced Commutation process. It is called as Commutation circuit. The active or passive components / elements such as Inductance & Capacitance are used here. & these are called as Commutating elements.

Forced Commutation is applied to choppers & Inverters. Since SCR is turned off forcibly it is termed as a Forced Commutation process.

many different methods of forced Commutation are present namely

- self Commutation
- Impulse Commutation
- Resonant pulse Commutation
- Complementary Commutation
- External pulse Commutation
- Load side Commutation
- line side Commutation

An Example of self Commutation by resonating load is shown below.



Natural Commutation can be observed in AC voltage Controllers, phase Controlled rectifier and in cyclo Converters.

—o—

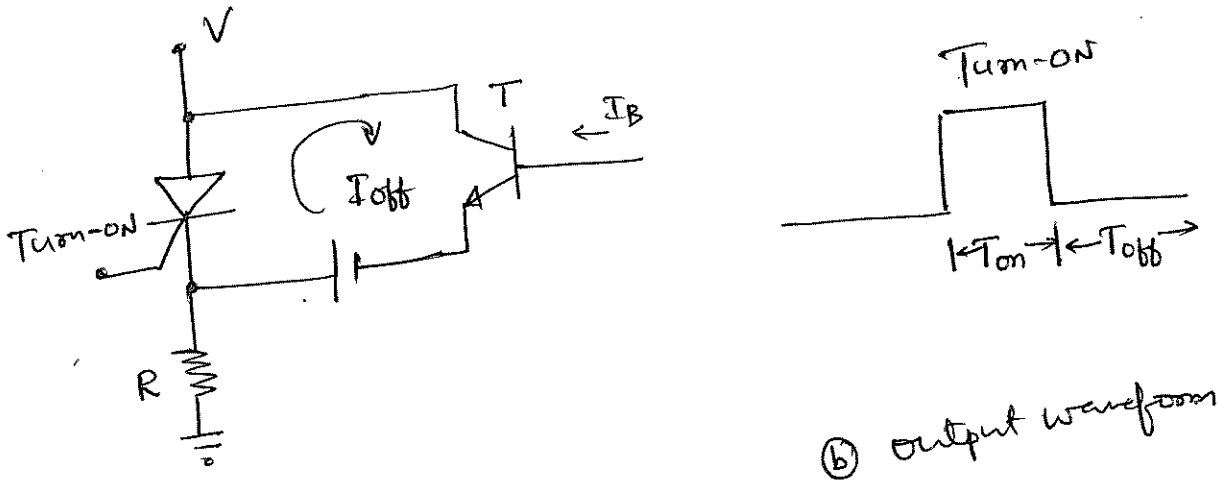
Another simple turn-off circuit is shown in figure below. Here a transistor and dc battery source in series are connected to the SCR.

When SCR is in condition mode (ON), $I_B = 0$ and when the transistor is off, it is almost an open circuit.

To turn off the SCR, a positive I_B pulse of magnitude large enough to drive the transistor into saturation is applied at the transistor base.

The transistor acts almost like a short circuit. This causes flow of very large I_{off} through the SCR in the opposite direction to its condition current. The total SCR current reduces to zero in a very short time causing it to turn off.

The Transistor has to withstand a large current but for a very short time. Turn-OFF time for an SCR is 5-30 μs.



(a) circuit. (b) output waveform.

Fig:- Turn-off circuit using SCR.

SCR characteristics and parameters

Forward & Reverse characteristics

Reverse characteristics

Consider a SCR shown in figure. Apply negative voltage to anode terminal and positive voltage to Cathode terminal.

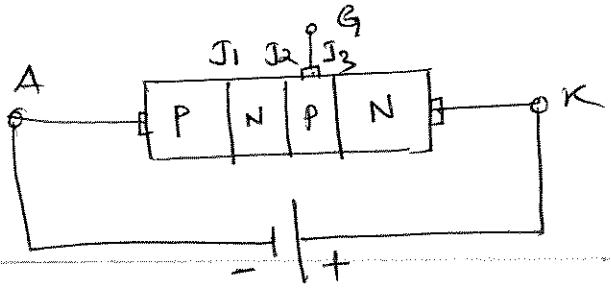
Then Junction J_2 is forward biased, while the Junction J_1 and J_3 are reverse biased.

When the reverse voltage $-V_{AK}$ is small, a small leakage current [of about 80 to 100 μA) flows, which is called as reverse blocking current.

If the reverse voltage is now increased, I_R (reverse Blocking current) practically remains Constant until $-V_{AK}$ becomes large enough to cause J_1 & J_3 to breakdown in the Zener or Avalanche mode.

As show in reverse characteristic curve, the reverse Current increases very rapidly when the reverse breakdown voltage is reached and if I_R is not limited, the SCR Could be damaged or destroyed

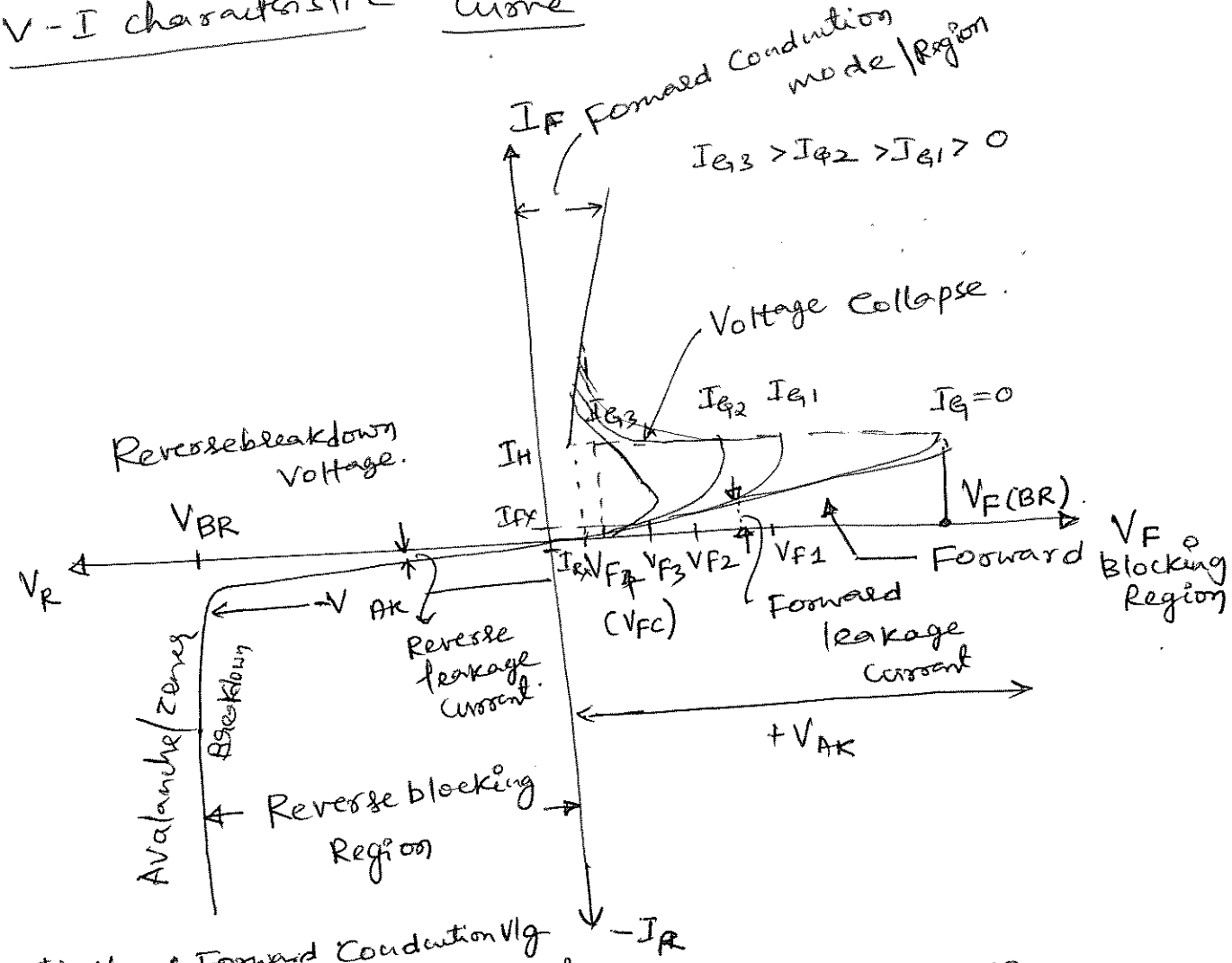
The Region of the reverse characteristics before reverse breakdown is Called reverse Blocking region.



J_1 & J_3 → Reverse Biased

J_2 → Forward Biased.

V-I characteristic Curve



Note:- V_{FC} : Forward Conduction Vlg
I_{RX} = Reverse Blocking Current

Figure : V-I characteristics.

If the SCR is forward biased with $I_G = 0$, the junctions J_1 & J_3 are forward biased and J_2 is reverse biased. If $+V_{AK}$ is very small, a small leakage current called as forward leakage current (I_{FX}) flows, which is almost equal to I_{RX} (reverse leakage current.

With $I_G = 0$, I_F remains at I_{FX} until $+V_{AK}$ is made large enough to cause the reverse biased Junction J_2 to break down. the Forward voltage at this point is called the Forward Breakover voltage $V_{F(BR)}$.

When $V_{F(BR)}$ is reached, the two transistors T_1 and T_2 are immediately switched on into saturation, and the anode cathode voltage falls to the Forward conduction voltage V_{F4} (V_{FC}).

The above method of triggering (Turn-ON) of transistor is called as Forward voltage triggering when in $I_G = 0$.

Consider when I_G is greater than zero. Then if $+V_{AK}$ is less than $V_{F(BR)}$, and $I_G = 0$ a small leakage current flows.

If I_G is made just slightly larger than the junction leakage currents, it will have a negligible effect on the level of $+V_{AK}$ for switch ON.

If I_G is made larger than the minimum base current required to switch the transistor T_2 ON, the SCR remains OFF until $+V_{AK}$ is large enough to forward bias the base-emitter junctions of T_1 and T_2.

As shown in figure. it is seen that when $I_G = I_{G3}$ $+V_{AK}$ must equal to V_{F3} for switch ON to occur.

The Forward conduction voltage, V_{F4} is made up ($V_{BE1} + V_{CE2}$) or ($V_{BE2} + V_{CE1}$).

The region of the V-I characteristics before switch-ON occurs is called the Forward Blocking region. & the region after switch-ON is called the Forward Conduction region. In FCR the SCR behaves as a Forward Biased Rectifier.

To switch the SCR OFF, the Forward current, I_F must be reduced below a level called Holding current I_H. The Holding current is the minimum level of I_F that will maintain the SCR in ON state.

(or)

Holding current is the value of current below which the SCR switches from the Conduction state to the forward blocking region.

As the gate current increases the triggering of the SCR will takes place for lesser value of the Anode-to Cathode voltage. as shown in figure.

$$I_{G3} > I_{G2} > I_{G1} > 0$$

and $$V_{F3} < V_{F2} < V_{F1} < V_{F(BR)}.$$

If a gate current greater than zero is maintained while the SCR is ON, lower values of holding current (I_{H1}, I_{H2} or I_{H3}) are possible.

Note:-

1. Forward Breakover voltage $V_{F(BR)}$ is the voltage at which for a given I_G, the SCR enters into Conduction mode. This voltage reduces as I_G increases. $V_{F(BR)}$ dependence on the circuit Connection between G and K terminals.

2. Holding current I_H is the value of current below which the SCR switches from Condution state to Forward Blocking regions of specified conditions.

3. Forward & Reverse blocking regions are those regions in which the SCR is open circuited and no current flows from anode to Cathode.

4. Reverse breakdown voltage corresponds to zener or avalanche region of a diode.

other parameters are
⟹ grid voltage, current and power are represented as

V_{GFM}, I_{GFM}, P_{GFM}.

Basically There are Different methods of Thyristor (SCR) turn-on techniques.

1. forward voltage triggering
2. gate triggering
3. dv/dt triggering
4. temperature triggering
5. Light triggering

Three modes are available

1. Forward Blocking mode
2. Forward Conduction mode
3. Reverse Blocking mode.

Application of SCR

These are used in rectifiers, regulated power supplies, dc to ac converter (inverters), delay Control & time delay Circuit.

The one application of SCR is variable Resistance phase control circuit is shown in below.

- Variable Resistance phase control,

upon triggering, an SCR (thyristor) permits flow of only forward current but blocks the current in reverse direction. The working of thyristor (SCR) this particular action is same as that of a diode.

On application of alternating voltage SCR causes rectified ac to flow but it needs to be triggered for each positive half cycle of ac.

It then produces constant dc (average value) current through load & dc voltage across load.

Adjusting the triggering time on positive half cycle of ac voltage would yield variable dc output.

This method is known as phase control.

A variable resistance phase control circuit is shown in figure. The SCR gate current is controlled through R and the variable Resistance R1.

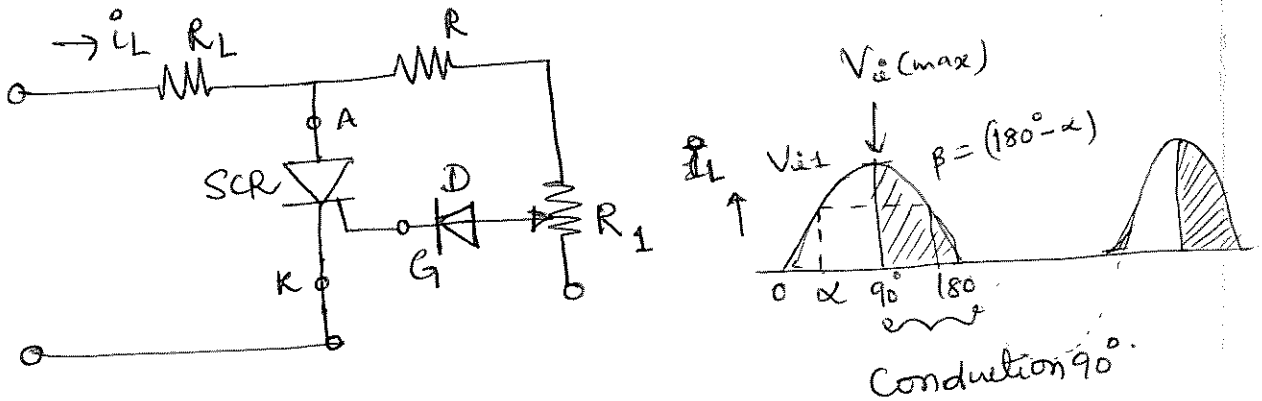
Let R_1 be adjusted to high value so that even at the peak value V_i (positive), $I_G < I_{G(TURN-ON)}$ and No Conduction take place.

Gradually Reduce R_1, then I_G increases to turn-ON SCR this triggering of SCR at a particular angle (time) of V_i take place.

Then SCR starts Conducting and Continues till V_i reaches zero (180°).

If we vary R_1, this allows the adjust of SCR firing angle from 0° to 90°. as shown in figure.

At R_1, corresponding to the firing angle of 90°, $V_i = V_i(max)$. If R_1 is adjusted for firing at α the firing will take place at angle $\alpha < 90^\circ$ but not at angle $\beta = (180^\circ - \alpha) > 90^\circ$ as the angle α is reached earlier in time on the V_i wave.
Hence this circuit is also known as half wave Variable resistance phase Control.



(a) Circuit (b) Firing angle

Figure : Variable resistance phase Control.

Thus $i_{L(dc)}$ Can be adjusted to the maximum value at 0° to the minimum value at 90°.
Diode is provided in the firing circuit to prevent the flow of reverse gate current.

— o —

Commutation

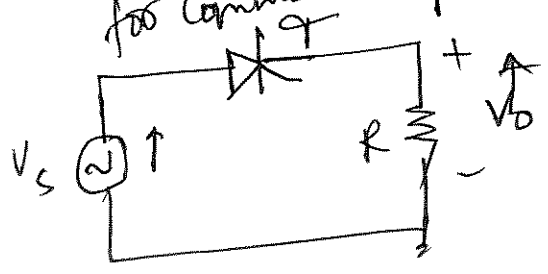
is the process of turning off a conducting SCR. There are two types of Commutation namely. current & voltage based.

Since the SCR is turned off forcibly it is termed as a forced Commutation process.

It occurs in AC circuits. ie when supply voltage is AC. Due to this SCR turns off when negative V/g appears across the SCR. Since there are no special CKTs needed to turn off the SCR, this type of Commutation is known as Natural Commutation

In AC supply, the current will flow through the zero crossing line while going from +ve peak to -ve peak. Thus a reverse V/g will appear across the device simultaneously which will turn off the thyristor immediately.

This process is called as NC as SCR is turned off naturally without using any external components or CKT or supply for Commutation process.



It is applied to DC CKTs. F.C is achieved by reverse biasing SCR device or by reducing SCR current below the holding current value. or by using active or passive components.

- Commutating elements such as inductance & Capacitance are used here.

FC is applied to choppers & inverters.

Following methods are used in F.C

- Self Commutation
- impulse
- Resonant pulse
- Complementary
- External pulse
- Load Side Commutation
- line Side Commutation.

NC can be observed in AC voltage Controllers, phase Controlled rectifiers & cycloconverters.

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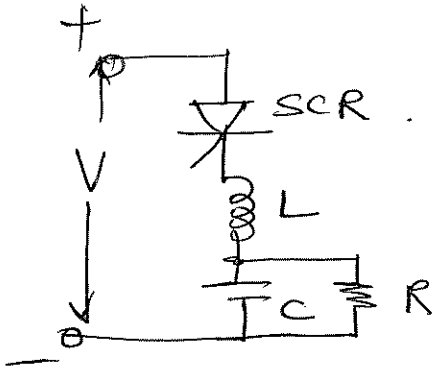

Self Commutated byresonatry load.

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Coauthors details (Mention maximum of three co authors details)

	Name	Contact Number	Email ID
Coauthor 1:			
Coauthor 2:			
Coauthor 3:			
Coauthor 4:			

External ckt is used for F.C process is called as Commutation process. is called as Commutation ckt & the elements in this ckt are called as Commutating elements

Module 3.

Operational Amplifiers & Applications

Introduction to Op-Amp
Op-Amp Input Modes
Op-amp parameters - CMRR
Input Offset voltage and current
Input Bias current
Input and Output Impedance, Slew rate

(12.1, 12.2 of Text 2)

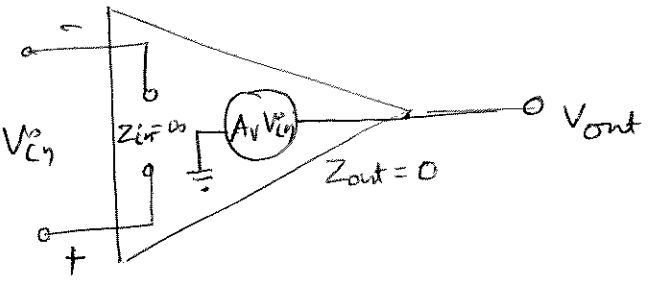
Application of op-amp.
Inverting amplifier
Non-inverting amplifier
Summer
voltage follower
Integrator
Differentiator
Comparator

(6.2 of Text 1).

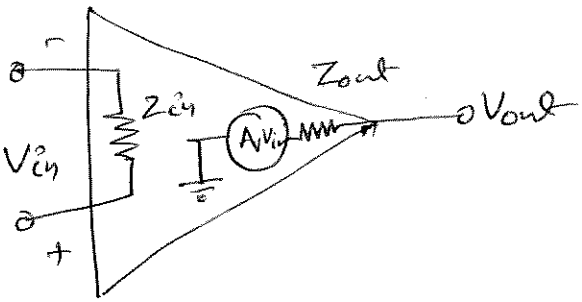
(RBT Levels : L1, L2 & L3)

(1)

Basic op-amp representation



(a) Ideal opamp representation.



(b) practical - op-amp representation.

Op-amp Input modes

Input signal modes

These are determined by the differential amplifier input stage of the op-amp.

(i) Differential mode:

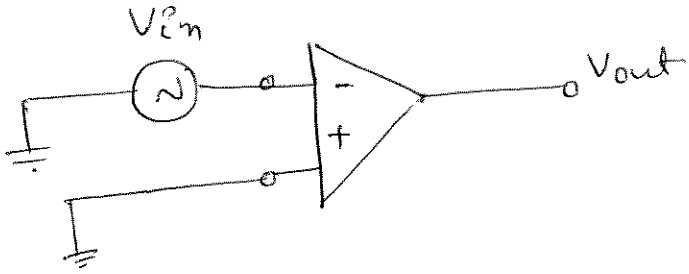
In this mode, either one signal is applied to an input with the other input grounded or two opposite polarity signals are applied to the inputs.

When an op-amp is operated in the single-ended differential mode, one input is grounded and a signal voltage is applied to the other input as shown in figure.

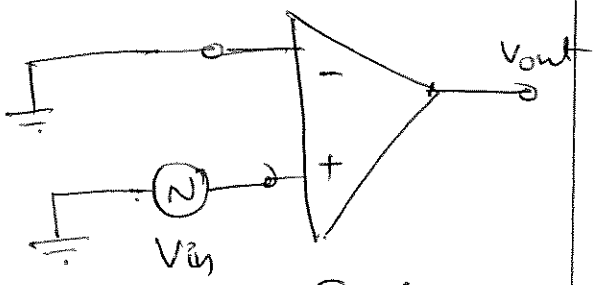
Case (1): Here the signal voltage is applied to the inverting input, an inverted, amplified signal voltage appears at the output.

Case (2): Here the signal is applied to the non-inverting input with the inverting input grounded. a non inverted, amplified signal voltage appears at the output

Single ended differential mode [SEDM]



(a) SEDM with input connected to inverting terminal.



(b) SEDM with input connected to non-inverting terminal.

In the Double ended differential mode, two opposite polarity (out of phase) signals are applied to inputs. as shown in figure. The amplified difference between the two inputs appear on the output.

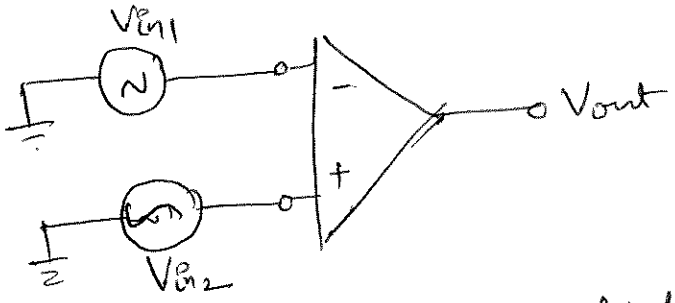


Fig: Double ended Differential mode

Common mode :- In common mode, two signal voltages of the same phase, frequency and amplitude are applied to the two inputs, as shown in figure. when equal input signals are applied to both inputs, they tend to cancel, resulting in a zero output voltage.

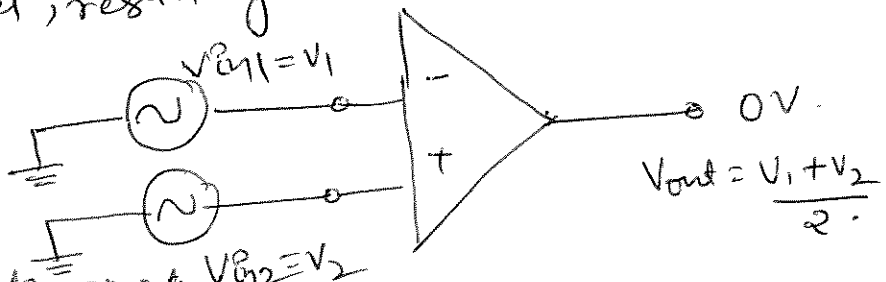


Fig: common mode operation.

Op-Amp parameters

In Common mode operation if same input appears on the both the input then output produced by the op-amp is zero. This is called Common-mode rejection. If any unwanted signal appears commonly on both op-amp inputs, then it rejects.

Common mode rejection means that this unwanted signal will not appear on the output & distort the desired signal. Common mode signals (noise) are the result of the pick-up of radiated energy on input lines, from adjacent lines, the 60Hz power lines, other sources.

Common Mode Rejection Ratio. [CMRR]

Desired signal can appear on only one input or with opposite polarities on both input lines can be amplified & appear on output. but unwanted signal (noise) appearing with the same polarity on both input is cancelled by the op-amp & do not appear on op-amp.

The measure of an amplifier's ability to reject Common mode signals is called as Common mode rejection ration [CMRR].

CMRR suggests the measure of the op-amp's performance in rejecting unwanted common-mode signals in the ratio of the open-loop differential voltage gain, A_{dm} to the Common-mode gain A_{CM}.

$$CMRR = \frac{A_{dm}}{A_{CM}} =$$

CMRR in decibels (dB)

$$CMRR = 20 \log \left(\frac{A_{dm}}{A_{CM}} \right)$$

Differential mode gain is also called as open loop gain (A_{OL}).

Open Loop Voltage gain :-

A_{OL}, of an op-amp is the internal voltage gain of the device.

It is the ratio of output voltage to input voltage when there are no external components.

$$A_{OL} = \frac{V_o}{V_{in}}$$

$A_{OL} = 200,000$ (106dB).

Also called as large-signal voltage gain.

CMRR of 100,000 for example, means that the desired input signal (differential) is amplified 100,000 times more than the unwanted noise (common mode).

Problem 1. A certain op-amp has an open-loop differential voltage gain of 100,000 & a common mode gain of 0.2. Determine the CMRR & express it in decibels.

Sol^n: $A_{OL} = 100,000$, $A_{cm} = 0.2$

$$CMRR = \frac{A_{OL}}{A_{cm}} = \frac{100,000}{0.2} = 500,000.$$

$$CMRR = 20 \log_{10}(500.000)$$

$$= 114 dB.$$

(2) Determine the CMRR and express it in dB for an op-amp with an open-loop differential voltage gain of 85,000 & a common-mode gain of 0.25.

Solution:- $A_{OL} = 85,000$, $A_{CM} = 0.25$.

$$CMRR = \frac{A_{OL}}{A_{CM}} = \frac{85000}{0.25}$$

$$CMRR = 20\log(\quad) = \quad .$$

Maximum Output voltage swing [$V_{O(p-p)}$]

With no input signal, the output of an op-amp is ideally 0V. This is called the quiescent output voltage. When an input signal is applied, the ideal limits of the peak-to-peak output signal are $\pm V_{CC}$.

Input offset voltage :- (V_{OS})

The ideal op-amp produces zero volts output for zero volts input. In a practical op-amp, however, a small dc voltage, $V_{out(error)}$, appears at the output when no differential input voltage is applied.

The main reason is a slight mismatch of the base-emitter voltage of the differential amplifier input stage of an op-amp.

V_{OS} → ideal value 0 Volts

V_{OS} → practical value 2mV or less.

Input offset voltage, V_{OS}, is the differential dc voltage required between the inputs to force the output to zero volts.

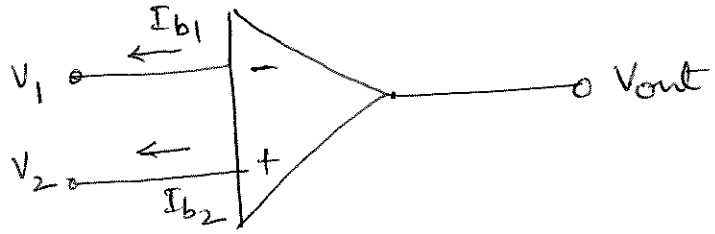
Input Bias Current (I_{Bias})

The input terminals of a bipolar differential amplifier are the transistor bases and, therefore, the input currents are the base currents.

The input bias current is the dc current required by the inputs of the amplifier to properly operate the first stage.

Input bias current is the average of both input currents.

$$I_{Bias} = \frac{I_{b_1} + I_{b_2}}{2}$$



$$I_{bias} = \frac{I_{b_1} + I_{b_2}}{2}$$

Figure :- Input bias current is the average of the two op-amp input current.

Input Impedance :-

- differential input impedance
- Common input impedance.

Differential input impedance is the total resistance between the inverting and the non-inverting inputs. as shown in fig.

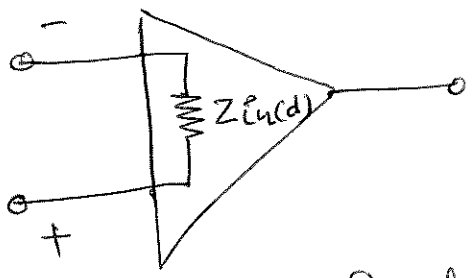
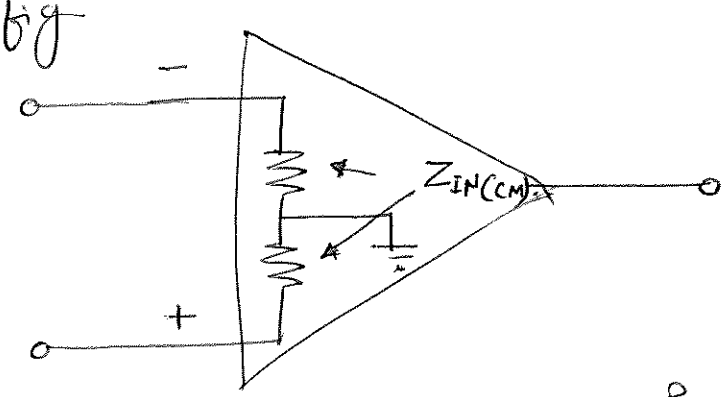


fig:- Differential input impedance

Differential impedance is measured by determining the change in bias current for a given change in differential input voltage.

The Common mode input impedance is the resistance between each input and ground and is measured by determining the change in bias current for a given change in common-mode input voltage. It is shown in fig



(b) Common-mode input impedance.

Input offset current :- I_{OS}

Ideally, the two input bias currents are equal, and thus their difference is zero.

Practically op-amp, however, the bias currents are not exactly equal.

The input offset current, I_{OS}, is the difference of the input bias currents, expressed as an absolute value.

$$I_{OS} = |I_{b1} - I_{b2}| = |I_{b1} - I_{b2}|$$

The effect input offset current is shown in figure

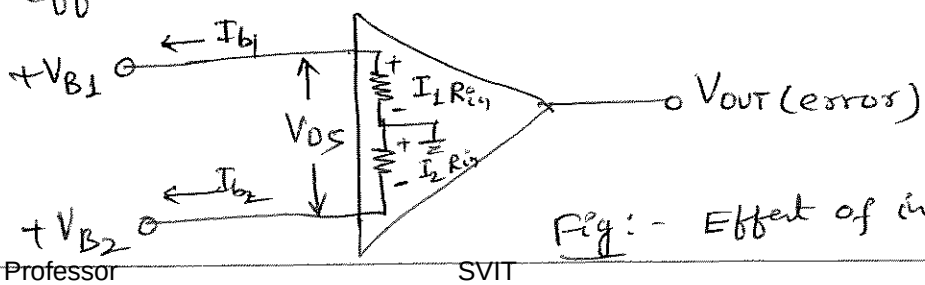


Fig :- Effect of input offset current.

The offset voltage developed by the input offset current is

$$V_{OS} = I_1 R_{in} - I_2 R_{in}$$
$$= (I_1 - I_2) R_{in}$$
$$V_{OS} = I_{OS} R_{in}$$

The error created by I_{OS} is amplified by the gain A_V of the op-amp and appears in the output as

$$V_{OUT(error)} = A_V I_{OS} R_{in}.$$

Output Impedance :-

The output impedance is the resistance viewed from the output terminal of the op-amp, as shown in figure.

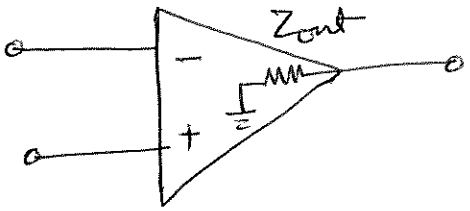


Fig. ~~output~~ op-amp output impedance

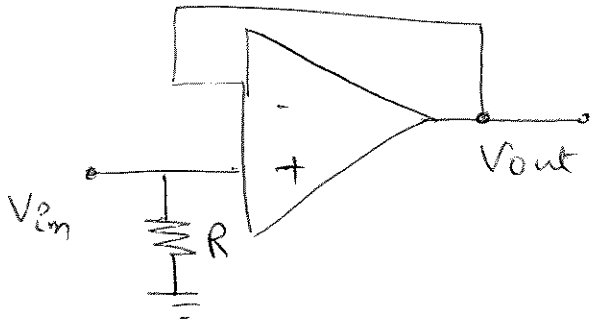
Slew rate :-

The maximum rate of change of the output voltage in response to a step input voltage is the slew rate of an op-amp.

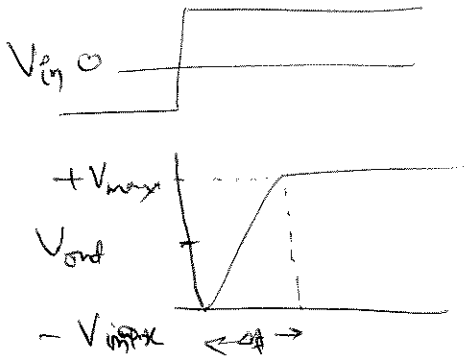
- The slew rate is dependent upon the high frequency response of the amplifier stages within the op-amp.
- Slew rate is measured with an op-amp connected as shown in figure.

The op-amp used here is the unity gain non inverting configuration

For step input, the slope on the output is inversely proportional to the upper critical frequency. slope increases as upper critical frequency decreases.



(a) Test circuit.



(b) step input voltage & the resulting output voltage.

Fig:- slew-rate measurement.

A pulse is applied to the input and the resulting ideal output voltage is indicated in figure (b)

The width of the input pulse must be sufficient to allow the output to slew from its lower limit to its upper limit.

Δt is the time interval required for the output voltage to go from its lower limit $-V_{max}$ to its upper limit $+V_{max}$, once the input step is applied.

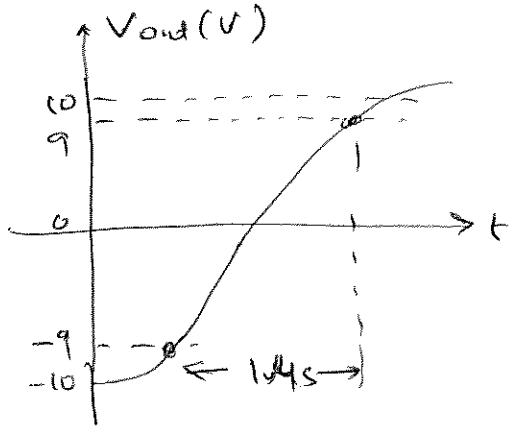
$$\text{slew rate} = \frac{\Delta V_{out}}{\Delta t}$$

$$\text{where } \Delta V_{out} = [+V_{max} - (-V_{max})]$$

$$\text{unit} = \underline{V/\mu s}.$$

problem:-

The output voltage of a certain op-amp appears as shown in figure in response to a step input. Determine the slew rate.



given data:-

$\Delta t = 1\mu s$

$V_{max} = 9V$, $-V_{max} = -9V$

$$\text{slew rate} = \frac{\Delta V_{out}}{\Delta t}$$

$$= \frac{+9V - (-9V)}{1\mu s} = 18V/\mu s$$

When a pulse is applied to an op-amp, the output voltage goes from $-8V$ to $+7V$ in $0.75\mu s$. What is the slew rate?

Operational amplifiers & Applications: - (1)

E&E Dept. Asha K SVIT.

Module - 3: -

Introduction to operational amplifiers: -

Ideal OPAMP, Inverting and non inverting opamp ckts. opamp applications: Voltage follower, Addition, subtraction, Integration, Differentiation, Numerical example as applicable

key words: IC: Integrated Ckts

Introduction: -

The op-amp is the common name of operational amplifiers was designed in 1948 using vacuum tubes. In those days, it was used in the analog computers to perform a variety of mathematical operations such as addition, subtraction, multiplication etc. hence the name operational amplifier. Those op-amp are bulky, power consuming and expansive.

The op-amp is perhaps the most important & versatile IC; it is used in analog signal processing and analog filtering.

The IC version of opamp uses BJTs (Bipolar Junction Transistors) and FETs which (Field effect Transistors) which are fabricated using semiconductor chip or wafer. The ckt design becomes very simple. These are low cost, small size, versatility, flexibility & dependability, op-amps are used in the fields of process control, Communications, Computers, power & signal sources, displays & measuring systems.

The op-amp is an excellent high gain D.C amplifier.

The symbol of an op-amp is shown in figure (1). It has two input terminals, one is inverting terminal (-) and non-inverting (+), and one output terminals. also

requires the positive supply voltage terminal V_{CC} or $+V$. The negative supply voltage terminal $-V_{EE}$ or $-V$.

The op-amp can be defined as high gain, direct coupled difference amplifier.

$$\text{gain of op-amp} = \frac{\text{output voltage}}{\text{input voltage}}.$$

Direct coupled indicates the op-amp can amplify signals of zero frequency. zero frequency means DC signals.

Difference amplifier means that the op-amp will have two inputs and the output is proportional to the difference between the two input voltages.

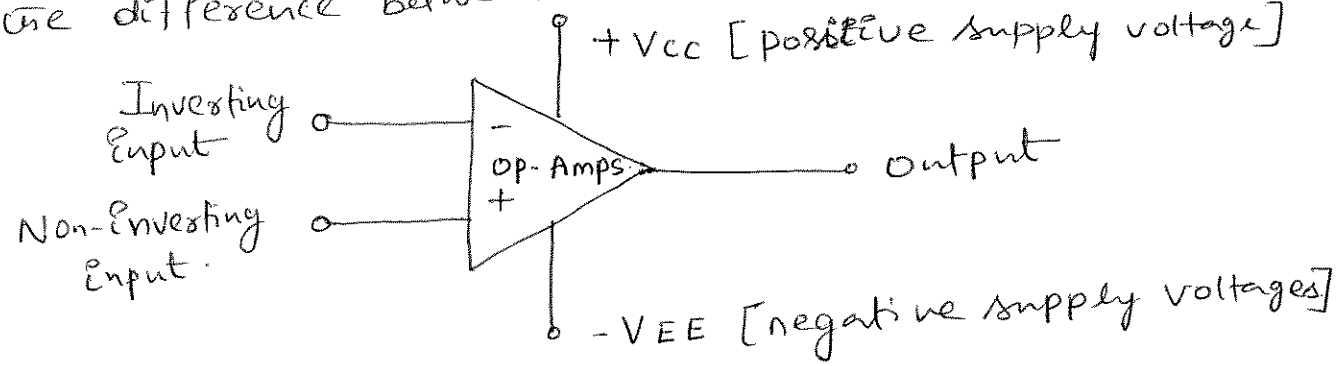
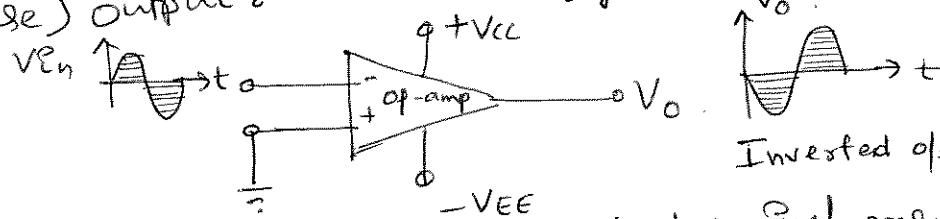


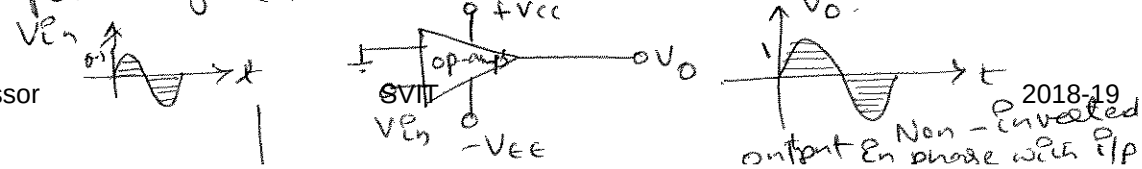
Figure (1) op-amp symbol.

Commercially used power supply voltages are ±15V. Balanced dual supply. popular supply voltages are ±9V, ±12V, ±22V.

- The input at inverting input terminal result in opposite polarity (antiphase) output. as shown in fig (2)

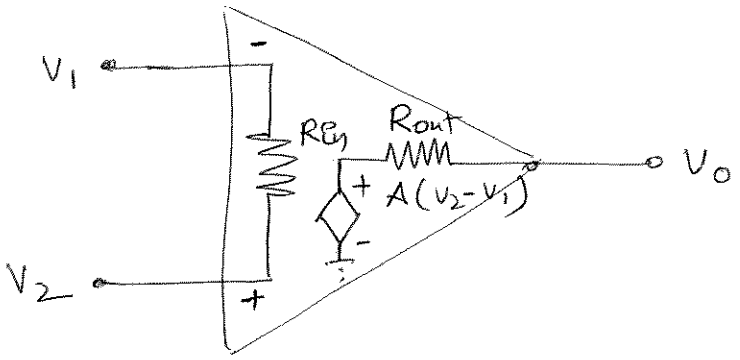


while the input at non inverting input terminal result in same polarity (phase) output. as shown in fig (3).



The simplified circuit model of an op-amp is shown in figure (4). It has a gain of A, input resistance R_{in} and output resistance R_{out}

An ideal op-amp has $A = \infty$, $R_{in} = \infty$ and $R_{out} = 0$.



figure(4). circuit model of op-amp - IC 741

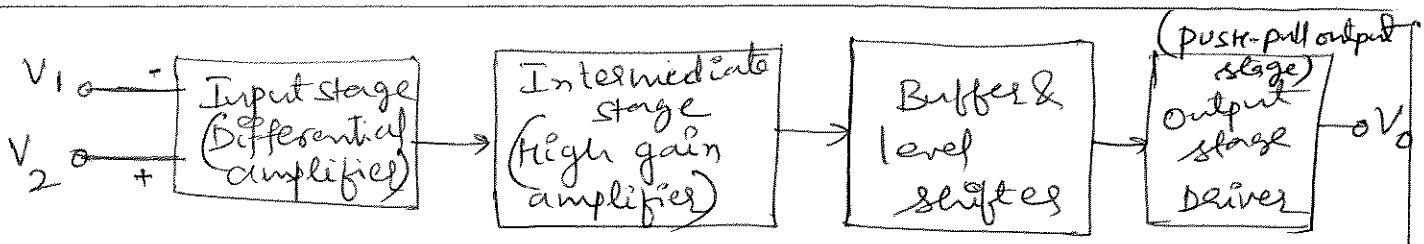
- The resistance R_{in} between the two input terminals is called input resistance of the op-amp. R_{in} - in MΩ range.
- The voltage source on the output side represents the output of the op-amp.
- The voltage gain 'A' indicated along with the source is called open loop gain. A = in order of 10^6.
- term $V_2 - V_1$ is called difference input voltage. The output proportional to difference between the two input voltages.
- The resistance in series with the voltage source is the output resistance (R_{out}) of the op-amp.

R_{out} is very low.

op-amp architecture.

Commercial op-amps (IC) consists of four cascaded block as shown in figure (5). It consists of

- Input stage (Differential amplifier).
- Intermediate stage (High-gain amplifier)
- Buffer & Level shifter stage
- (Driver) & output stage.



figure(1) Block diagram of op-amp. IC 741.

Input stage :-

- It requires high input impedence to avoid loading on the sources. It requires two input terminals. It also requires low output impedance.
- All these requirements are achieved by using the dual, input, balanced output Differential amplifier as input stage.
- function of a Differential amplifier is to amplify the difference b/w the two input signals. It provide voltage gain of the amplifier. DA Consists of two BJT's (MOSFET) emitter terminal Connected together.

Intermediat stage :-

- The output of the input stage drives the next stage which is an intermediate stage. It is also an differential amplifier.

the overall gain requirement of op-amp is very high. The input stage alone cannot provide such a high gain. Intermediate stage provides an additional voltage gain required. This stage consists of Cascaded amplifiers Called multistage amplifier used to get high gain.

Buffer & Level shifting stage

The level shifter shifts the level of the output of the Intermediate stage. This stage shifts the DC level.

- The level shifter stage brings the d.c. level down to ground potential, when no signal is applied to the input terminals. Then the signal is given to the last stage which is the output stage. Emitter Switching ckt is used.

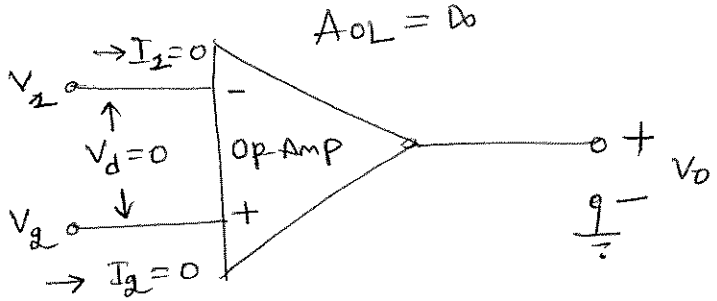
Output stage :-

The basic requirements are low output impedance, large a.c output voltage swing and high current sourcing & sinking capability.

push-pull complementary amplifier are used as Driver stage. The output stage provides the required power output. This is also called power amplifier.

IDEAL OPAMP

The figure (6) shows ideal amplifier. It has two input signals V_2 & V_1 applied to Non Inverting & Inverting terminals respectively.



Ideal op-amp.

The characteristics of ideal op-amp are.

(a) Infinite input impedance ($R_{in} = \infty$)

- The input impedance of the op-amp is infinity.
- The input impedance is defined as the impedance seen at the input terminals of the op-amp. The impedance is a parameter which opposes the flow of current. $R_{in} = \infty$, ensures that no current can flow into the ideal op-amp.

(b) Infinite voltage gain $A_{OL} = \infty$.

The differential open loop gain is infinite for ideal op-amp.

$$A = \frac{V_o}{V_{id}} = \infty.$$

for any input voltage, the output voltage of op-amp becomes infinite.

(c) Zero output impedance : ($R_o = 0$)

For ideal op-amp $R_o = 0$. This ensures that the output voltage of the op-amp remains same, irrespective of the value of the load resistance connected.

(d) Infinite CMRR :- ($\rho = \infty$)

The ratio of differential gain & common mode gain is defined as CMRR.

if CMRR $= \infty$, an ideal op-amp ensures zero common mode gain. Due to this common mode noise output voltage is zero for an ideal op-amp.

(e) Zero offset voltage ($V_{ios} = 0$)

The presence of the small output voltage though $V_1 = V_2 = 0$ is called an offset voltage. It is zero for an ideal op-amp. This ensures zero output for zero input signal voltage.

(f) Temperature independency :- The characteristics of op-amp do not change with temperature.

(g) Infinite Bandwidth

The range of frequency over which the amplifier performance is satisfactory is called Bandwidth. Bandwidth $= \infty$. This means that operating frequency range is from 0 to ∞.

This ensures that the gain of the op-amp will be constant over the frequency range from d.c (zero frequency) to infinite frequency. So op-amp can amplify d.c as well as a.c. signals.

(h) Matched Transistors.

The transistors used in difference amplifier are identical.

(i). Infinite slew rate : (S = ∞)

Slew rate indicates ~~speed~~ the rate at which the output varies.

"Infinite slew rate indicates that the output voltage can change simultaneously with the changes in the input voltage."

(j) power supply rejection ratio (PSRR = 0)

PSRR is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping other power supply voltage constant. It is also called as power supply sensitivity or supply voltage rejection ratio (SVRR).

unit - mV/V or μV/V ideal value = 0.

Ideal characteristics table

Sl.no	characteristics	Symbol	Ideal values	practical
1	open loop voltage gain	A_{OL}	∞	2×10^5
2.	Input Impedance	R_{in}	∞	2MΩ
3.	output Impedance	R_o	0	75Ω
4.	I/p offset voltage	V_{OOS}	0	2mV.
5.	Bandwidth.	BW	∞	1MHz
6.	CMRR	ρ	∞	90dB.
7.	slew rate	S	∞	0.5V/μsec
8.	power supply rejection ratio	PSRR	0	30μV/V.
	Input bias current	I_b	0	80nA

Typical parameter of μA741 IC op-amp are

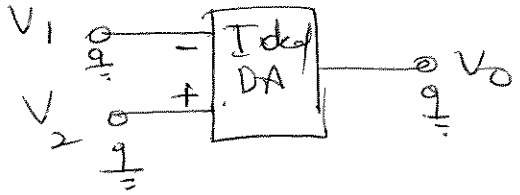
$A = 200,000$ $R_{in} = 2M\Omega$ $R_o = 75\Omega$ CMRR = 80-100dB

100dB = 10^5

Ideal op-amp [OP-Amp Input Modes AND Parameters]

- Differential amplifier (DA): An amplifier which amplifies the difference between the two input signal. Hence
- it is called Differential (or Difference) amplifier.

apply two input signal to DA while V_o is the single ended output. Each signal is measured with respect to ground.



$$V_o \propto (V_2 - V_1) \quad \rightarrow (1)$$

Differential gain (A_d)

From eqn (1), we can write

$$V_o = A_d (V_2 - V_1)$$

$A_d \rightarrow$ Constant of proportionality.

The A_d is the gain with which D.A. amplifies the difference between two input signals. hence it is differential gain. A_d.

let difference voltage $V_d = V_2 - V_1$.

$$V_o = A_d V_d$$

Hence differential gain $= A_d = \frac{V_o}{V_d}$.

Differential gain in decibel (dB)

$$\boxed{A_d = 20 \log_{10} (A_d) \text{ in dB}}$$

Common mode gain. (A_c)

- If we apply two input voltages which are equal in all the respects to the differential amplifier i.e $V_1 = V_2$ then ideally the output voltage must be equal to zero.

• But the output voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average or Common level of the two inputs.

if average level of the two input signal is applied to op-amp denoted as $V_c = \frac{V_1 + V_2}{2}$.

practically the Differential amplifier produces the output voltage proportional to such Common mode signal.

The output voltage

$$V_o = A_c V_c.$$

$A_c \rightarrow$ Common mode gain.

$$A_c = \frac{V_o}{V_c}$$

So the total output of any differential amplifier is.

$$V_o = A_d V_d + A_c V_c.$$

For ideal op-amp, $A_d = \infty$, $A_c = 0$. This ensures zero o/p for $V_1 = V_2$.

Common mode Rejection ratio

• The ability of an op-amp to reject a Common mode signal is expressed by a ratio called CMRR. denoted by ρ.

• It defined as the ratio of differential voltage gain A_d to Common mode voltage gain A_c

$$CMRR = \rho = \left|\frac{A_d}{A_c}\right|$$

Ideally $A_c = 0$, hence $CMRR = \infty$.

practical OA, A_d is large, A_c is small, hence CMRR = very large

CMRR in dB $= 20 \log \left| \frac{A_d}{A_c} \right|$ dB.

Important parameters of op-amp [practical] ① $A_{OL} = 10^5$ to 10^6

② $R_i = 1$ MΩ to 100 MΩ

③ $R_o = 100$ to 200 Ω.

④ BW = small

⑤ Input offset current $I_{ios} = I_{B1} - I_{B2}$

① Input offset voltage

Differential voltage (V_{os}) needed to make $V_o = 0$.

Typical value $V_{os} = 1$ mV.

② Input Bias current :-

$I_B = \frac{I_{B1} + I_{B2}}{2}$ to make $V_o = 0$,

I_{B1} & I_{B2} are base currents of two transistors.

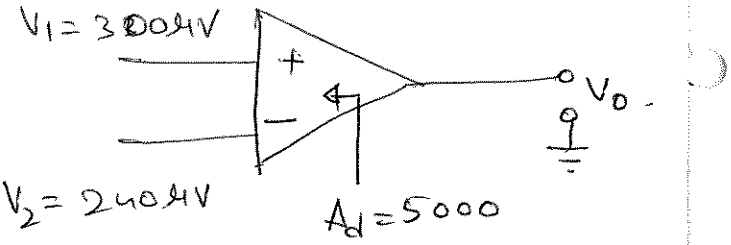
Typical value is 80 nA.

③ Input offset current $I_{ios} = |I_{B1} - I_{B2}|$.

① Determine the output voltage of an op-amp for the input voltage of 300 μV & 240 μV. The differential gain of the amplifier is 5000 and the value of the CMRR is 10^5. (4M)

$A_c = \frac{A_d}{CMRR} = \frac{5000}{10^5}$

$= 0.05$.



$V_o = A_d V_d + A_c V_c$

$= 5000 * (V_1 - V_2) + A_c \frac{(V_1 + V_2)}{2}$

$= 5000 * 60 + 0.05 \times 270$.

$= 300013.5\,\mu V$. $= 300.0135$ mV.

we know that

$$V_o = A_d V_d + A_c V_c$$

$$= A_d V_d \left[1 + \frac{A_c V_c}{A_d V_d}\right]$$

$$\boxed{V_o = A_d V_d \left[1 + \frac{1}{CMRR} \cdot \frac{V_c}{V_d}\right]}$$

if we know A_d, V_c, V_d & CMRR we can easily calculate V_o, without knowing A_c → Common mode voltage gain.

Slew rate and Frequency response

Frequency response.

Some RC Couplings are provided in an op-amp circuit so as to reduce the gain at high frequencies.

otherwise, a positive feedback occurs from stray Capacitances causing high frequency Oscillations.

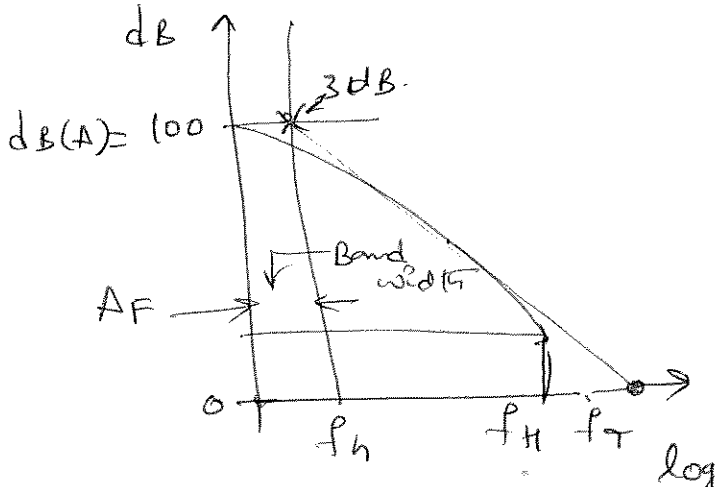
The op-amp acts like a Low-pass filter with a break frequency at $f_h = 10Hz$.

Typical frequency response is shown in fig using Bode plot.

From Bode plot

$$20\log\frac{f_T}{f_h} = dB(A) = 20\log A$$

$$\therefore \frac{f_T}{f_h} = A.$$



$A f_h = f_T$ = unity gain (0dB) op-amp LPF frequency response.

frequency = Constant.

$A f_h$ = gain Bandwidth product

If negative feedback around op-amp it reduces the gain to A_F, then

$$A_F f_H = f_T$$

or $$f_H = \frac{f_T}{A_F} >> f_h.$$

Due to reduction in gain caused by feedback, the bandwidth increases from f_h to f_H.

Slew Rate :-

Because of presence of capacitances, which is RC combination it can change at a limited rate, & the rate of change of output of the op-amp is limited to

$$\text{Slew rate } S = \left.\frac{dv_o}{dt}\right|_{max.}$$

Its typical value is 0.5 V/μs as shown in figure

For a sinusoidal signal

$$V_o = V_m \sin\omega$$

$$S = \left.\frac{dV_o}{dt}\right|_{max} = V_m\omega.$$

or $$S = 2\pi f V_m$$

or It is a combination of frequency & peak value of output.

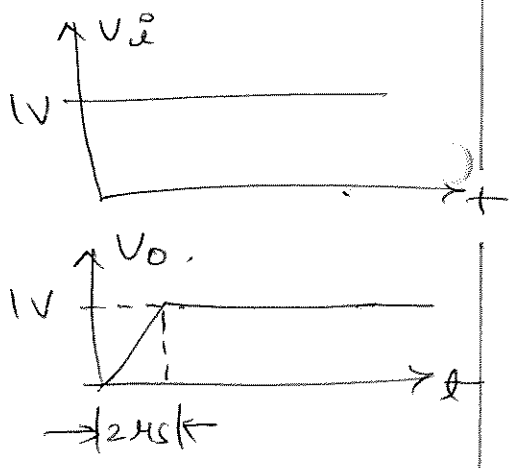


Fig. Effect of slew rate

———o———

The two assumptions are.

1. Zero input current :-
The current drawn by either of the input terminals (inverting & non inverting) is zero.

2. Virtual ground.
This means that differential input voltage V_d b/w non inverting & inverting input terminals is essentially zero.

If V_o = few volts, due to large open loop gain of op-amp,

$$V_d = 0 = V_1 - V_2$$

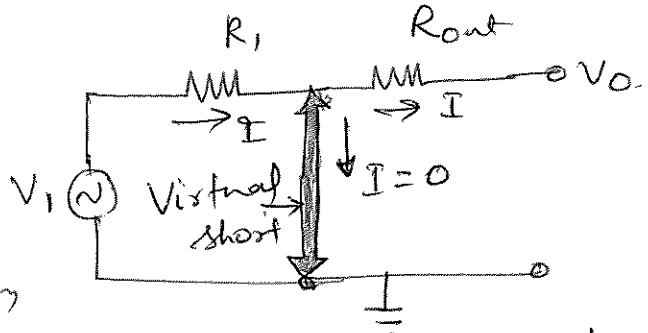
$$V_o = V_d A_{OL} \text{ i.e } V_d = \frac{V_o}{A_{OL}} = \underline{0}, \quad A_{OL} = \text{very big } \infty$$

$$V_d = (V_1 - V_2) = 0$$

$$\boxed{V_1 = V_2}$$

Thus under linear range of operation there is virtually short circuit between the two input terminals, in the sense that their voltages are same.

Fig shows the concept of the virtual ground. The thick line indicates the virtual short circuit between the input terminals.



Concept of virtual ground

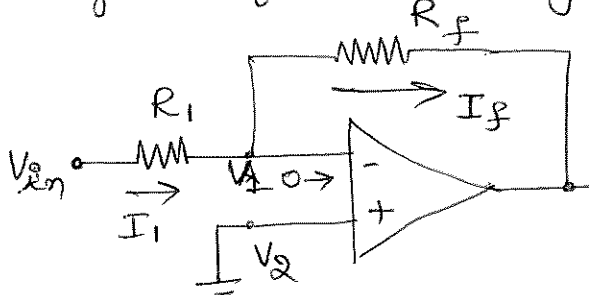
- Now if the non-inverting terminal is grounded by the concept of virtual short, the inverting terminal is also at ground potential, though there is no physical connection b/w the inverting terminal & the ground. This is principle of virtual ground.

It is defined as phenomenon by which the potential difference between the two input terminal is zero.

Inverting op-amp circuits

An amplifier which provides a phase shift of 180° between input & output is called inverting amplifier.

- The basic circuit diagram of an inverting amplifier is shown in figure.



- Connect input signal V_{in} to the non-inverting terminal through a resistor R_1. The non inverting terminal is grounded.
- The resistance R_f connects the output terminal to inverting terminal to provide the negative feedback.

Note:- all amplifier should have negative feedback.

When (+) terminal is grounded, the (-) terminal is virtually at ground potential. **Step1**: V_{in} at V_2 terminal. $V_2 = 0$ because connected ground.

Step2: The input impedance of op-amp is $R_{in} = \infty$ hence current into an op-amp terminal is zero. From virtual ground concept $V_1 = 0$.

$$V_2 = V_1 = 0 \rightarrow (1)$$

Step3: applying KCL to inverting terminal

$$I_f = I_1 \rightarrow (2)$$

Step4: replace current by ohms law

$$I_f = \frac{V_1 - V_o}{R_f} = \frac{-V_o}{R_f}$$

$$I_1 = \frac{V_{in} - V_1}{R_1} = \frac{V_{in}}{R_1}$$

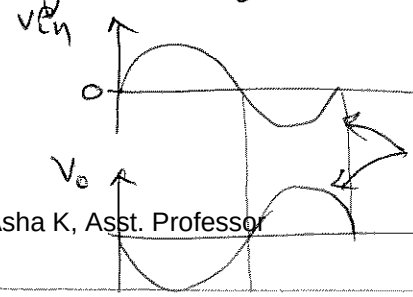
$$\frac{0 - V_o}{R_f} = \frac{V_{in}}{R_1}$$

The gain is.

$$A_V = \text{voltage gain} = \frac{V_o}{V_{in}} = -\frac{R_F}{R_1}$$

Here the output voltage is the negative of the input voltage, i.e it is inverted.

$$V_o = -\left(\frac{R_f}{R_1}\right) V_{in}$$



Waveform of inverting amplifier.

problem (1)

An inverting amplifier has $R_1 = 2K\Omega$ $R_f = 10K\Omega$. for an input voltage of 1.5 V, find the output voltage of the circuit.

$R_1 = 2K\Omega$ $R_f = 10K\Omega$ $V_{in} = 1.5V$ $V_o = ?$

$$V_o = -\left(\frac{R_f}{R_1}\right) \cdot V_{in}$$

$$= -\left(\frac{10\times10^3}{2\times10^3}\right) * 1.5.$$

$$= -7.5 \text{ Volts}.$$

(2). Design an inverting amplifier to provide an output voltage of -9 V for an input of 2V.

given $V_{in} = 2V$ $V_o = -9V$.

Find R_1, R_2.

$$A_V = \frac{V_o}{V_{in}} = \frac{-9}{2} = 4.5.$$

$$A_V = -\frac{R_f}{R_1} = . \quad \text{let } R_1 = 1K\Omega$$

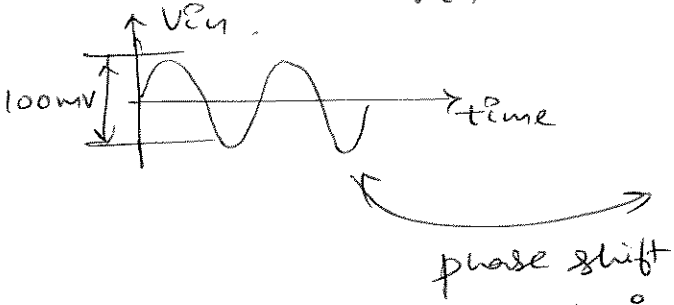
$$-4.5 = \frac{-R_f}{1K\Omega} \qquad \boxed{R_f = +4.5K\Omega}.$$

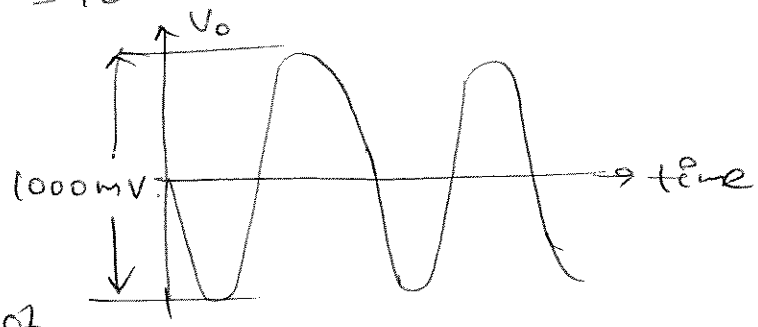
(3). An op-amp is used as an inverting amplifier to amplifies an input sine wave of amplitude 100 mV. (peak to peak) the input Resistance $R_1 = 1K\Omega$ and feedback resistance $R_f = 10K\Omega$. Calculate the voltage gain & sketch the output waveform to scale.

given:- $V_{in} = 100mV$, $R_1 = 1K\Omega$ $R_f = 10K\Omega$. $A_V = ?$

$$V_o = -\left(\frac{R_f}{R_1}\right) * V_{in} = \frac{-10\times10^3}{1\times10^3} * 100mV. = -1V$$

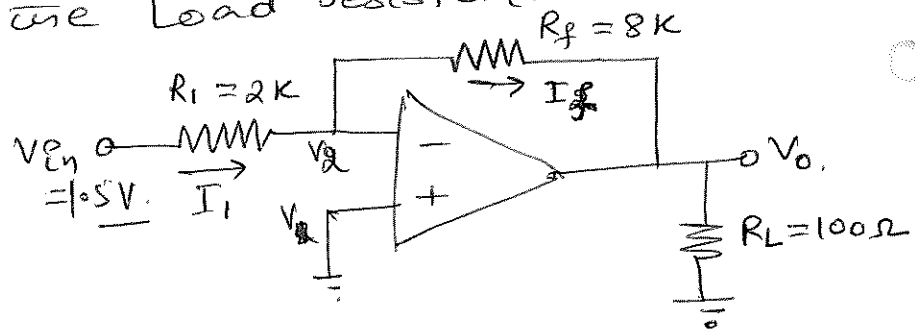
$$A_V = \frac{-V_o}{V_{in}} = \frac{-1\ V}{100mV} = -10.$$





phase shift of 180°.

④. In the following op-amp circuit find voltage gain, input current (current drawn) from the source), output voltage, the current through the Load resistor, power delivered to the Load resistor.



given Data :-

$R_f = 8K.$

$R_1 = 2K$

$R_L = 100\Omega$

$V_{in} = 1.5\ V$

Find $A_V, I_{in}, V_o, I_L, P_o$

$$A_V = \frac{-V_o}{V_{in}} = \frac{R_f}{R_1} = \frac{-8}{2} = -4.$$

$$I_{in} = \frac{V_{in}}{R_1} = \frac{1.5}{2K} = 750\ \mu A = 0.75\ mA.$$

$$V_o = A_V V_{in} = (-4) * 1.5 = -6\ V.$$

$$P_o = (V_o)^2 / R_L = (-6)^2 / 100$$

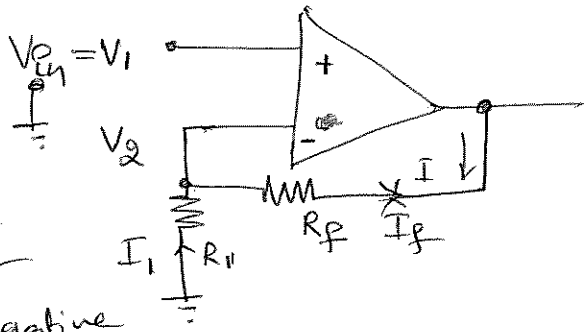
$$= 0.36\ W.$$

$$I_L = \frac{V_o}{R_L} = \frac{-6}{100} = -0.06\ A.$$

Non-Inverting amplifier :-

An amplifier which amplifies the input without producing any phase shift between input & output is called Non-inverting amplifier.

The circuit Diagram is shown in figure.



Input signal is applied to the non-inverting terminal.

The resistance R_f connects the output terminal to inverting terminal to provide the negative feedback.

Feedback circuit is completed by connecting ~~it~~ to resistance R_1 and following ground.

Step ①
The voltage V_1 at the non-inverting terminal.

$$V_{in} = V_1$$

Step ②
From the concept of virtual ground, $\boxed{V_1 = V_2 = V_{in}}$.

Step ③
By applying KCL at the inverting terminal. Let I_1 is the current through resistor R_1. I_f is the current through the resistor R_f.

Step ④ Replace current by ohms law. $I_1 = I_f$

$$\frac{0 - V_2}{R_1} = \frac{V_2 - V_o}{R_f} \Rightarrow \frac{-V_2}{R_1} = \frac{V_2}{R_f} - \frac{V_o}{R_f}$$

$$\frac{V_o}{R_f} = \frac{V_2}{R_f} + \frac{V_2}{R_1}$$

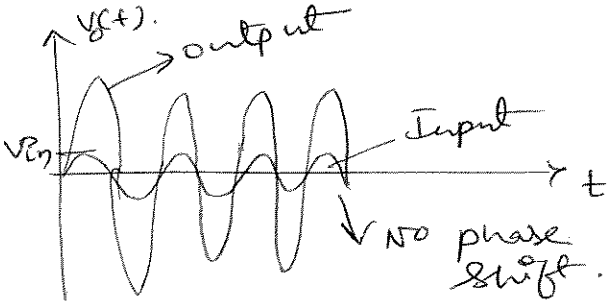
$$\frac{V_o}{R_f} = V_2\left[\frac{R_1 + R_f}{R_f * R_1}\right] \qquad V_2 = V_1$$

$$\frac{V_o}{R_f} = V_1\left[\frac{R_1 + R_f}{R_f R_1}\right]$$

A_V Voltage gain $= \frac{V_o}{V_i} = \left[\frac{R_1 + R_f}{R_1}\right] = \left[1 + \frac{R_f}{R_1}\right]$

If $R_1 = \infty$ then $A_V = 1$ the ckt is then Voltage follower.

& $R_f = 0$ then also $A_V = 1$ unity gain.



Waveform of non-inverting amplifier.

Problems:-

(1) A non-inverting amplifier has $R_1 = 2K\Omega$, $R_f = 10K\Omega$. for an input voltage of 1.5V, Find the output voltage of the circuit.

$$\frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1} \qquad V_o = \left[1 + \frac{R_f}{R_1}\right] V_{in}.$$

$$= \left[1 + \frac{10}{2}\right] 1.5 = 9\,V$$

$$A_V = \frac{V_o}{V_{in}} = \frac{9V}{1.5V} = 6$$

(2) Design a non-inverting amplifier to provide an output voltage of 9V for an input of 2V.

given. $V_o = 9V$ $V_{in} = 2V$.

$$A_V = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}$$

$$\frac{9}{2} = 1 + \frac{R_f}{R_1} \qquad \text{if } R_1 = 1K\Omega.$$

$$\frac{R_f}{R_1} = 4.5 - 1$$

$$R_f = 3.5 * R_1$$

$$R_f = 3.5K\Omega \qquad R_1 = 1K\Omega.$$

The open loop voltage gain of op-amp is A_V and due to finite gain the concept of virtual ground cannot be used.

$$V_d = V_1 - V_2 = V_{in} - V_2$$

& $$V_o = A_V V_d = A_V (V_{in} - V_2) \rightarrow (1).$$

Here R_f & R_1 forms a voltage divider.

$$V_2 = R_1 * \frac{V_o}{R_1 + R_f} = \beta V_o.$$

$$\beta = \frac{R_1}{R_1 + R_f} = \text{feed back factor}.$$

$$V_o = A_V [V_{in} - \beta V_o]$$

$$V_o = A_V V_{in} - A_V \beta V_o \quad \text{i.e } V_o(1 + A_V \beta) = A_V V_{in}.$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{A_V}{1 + A_V \beta}.}$$

But $\frac{V_o}{V_{in}}$ is called closed loop voltage gain denoted as A_{vf}

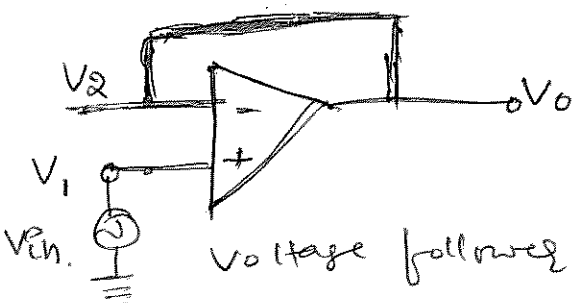
$$\boxed{A_{vf} = \frac{A_V}{1 + A_V \beta}.}$$

23.b.11

Voltage follower :-

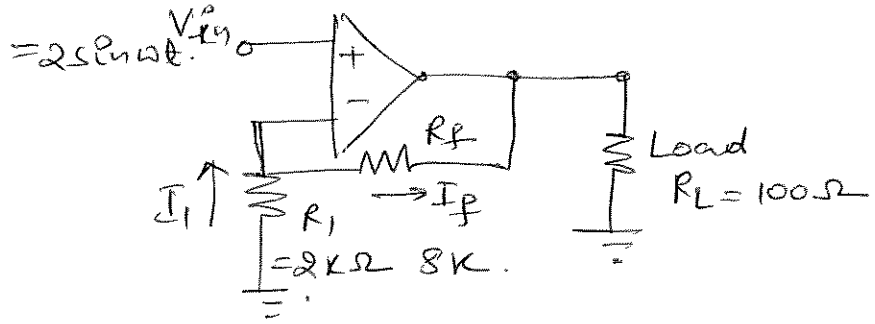
A circuit in which the output voltage follows the input voltage is called voltage follower circuit. A voltage follower is a circuit with non-inverting configuration. The voltage gain is unity.

- Input signal V_i is connected to the non inverting terminal
- The output terminal is connected to inverting terminal directly to provide the negative feedback.



Voltage follower.

(3) In the following op-amp circuit find voltage gain, current drawn from the source, output voltage, the current through the Load resistor. power delivered to the Load resistor.



given.

$R_1 = 2K\Omega$

$R_f = 8K\Omega$

$V_{in} = 2\sin\omega t$.

Find A_V, I_{in}, V_o, I_L P_o.

$$A_V = 1 + \frac{R_f}{R_1} = 1 + \frac{8}{2} = 5.$$

$$I_{in} = \frac{V_{in}}{R_1} = \frac{2}{2K\Omega} = 1mA \text{ (peak value)}.$$

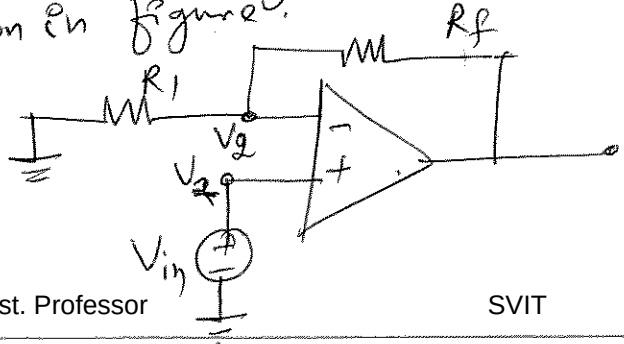
$$V_o = A_V V_{in} = (5)\,2 = 10V$$

$$V_{o(rms)} = \frac{V_o}{\sqrt{2}} = \frac{10}{\sqrt{2}} = 7.07\,V.$$

$$P_o = \frac{V_o^2}{R_L} = (7.07)^2/100 = 0.5 \text{ Watts}.$$

Question Draw the non-inverting voltage amplifier circuit using an op-amp & show that the closed loop voltage gain is given by $A_{vf} = \frac{A_V}{1 + A_V \beta}$ where A_V → open loop voltage gain of an op-amp. β → feedback factor.

Ans:- The non-inverting amplifier is shown in figure.



Step① The voltage V_1 at non-inverting terminal is $V_1 = V_{in}$

Step② The node V_1 is also at the same potential as V_2 i.e V_{in} according to the concept of virtual ground.

$$V_1 = V_2 = V_{in}.$$

Step③ Since the node V_2 is connected to the output terminal directly, the voltage at the output terminal is same as the inverting terminal.

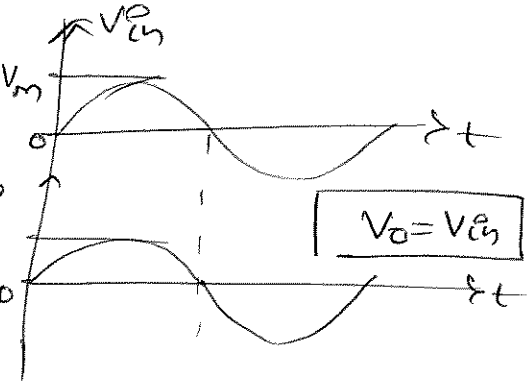
$$\therefore V_o = V_1 = V_2.$$

It is also called source follower, unity gain amplifier, buffer amplifier or isolation amplifier.

The output voltage is said to be following the input voltage. ∴ the ckt is called a voltage follower.

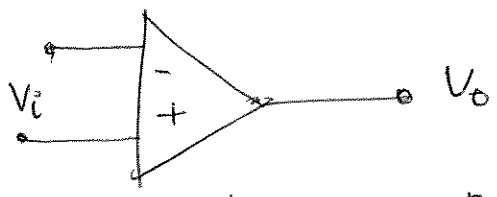
The waveform shown in figure.

- Voltage follower has large bandwidth.
- Very large input resistance, in MΩ
- Low output impedance, almost zero.
- The o/p follows the input exactly without any phase shift.

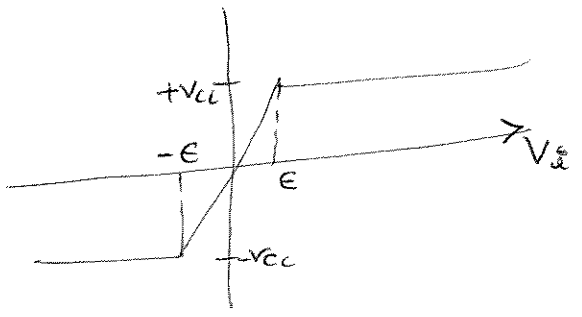


Transfer characteristics of op-amp

An op-amp is linear with high gain over a very small value of $V_i = \epsilon$ as shown in fig. beyond which it saturates, $V_o = V_{cc}$



(a) open loop op-amp



(b) Transfer characteristics

Problem① The input to the op-amp is $10\sin 10t$ volts. Draw the output waveform indicating time period & maximum value.

Ans:- the ckt is ^ follower

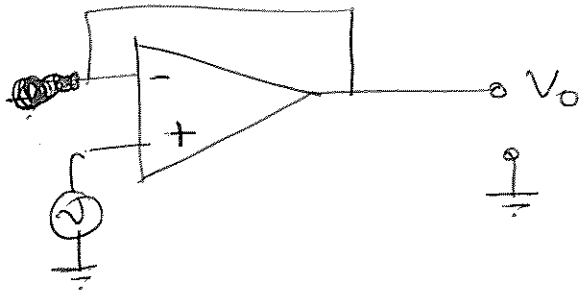
$V_o = V_{in}$

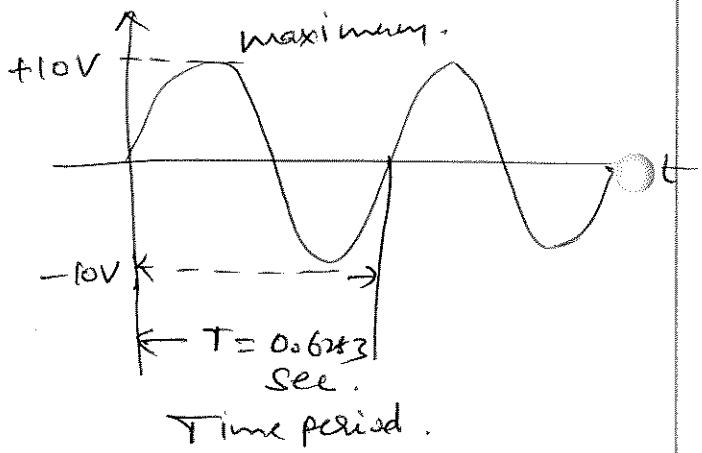
$= 10\sin 10t$.

maximum value $= 10V$

$\omega = 10 = \frac{2\pi}{T}$

$T = 0.6283$ sec.





Addition or Summer ckt :-

An op-amp ckt in which the output voltage is proportional to the sum of the all the input voltages can be defined as summer ckt.

Two types of summer ckt

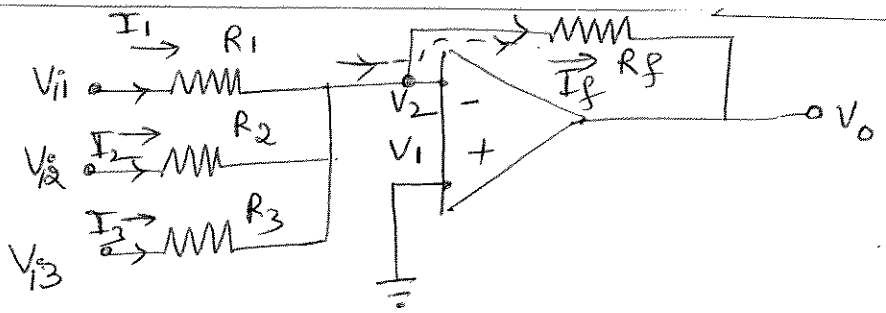
① Inverting Summer ckt

② Non inverting Summer ckt.

Classification made depending upon the sign of the output.

Inverting Summing amplifier

- In this ckt, all the input signal to be added are applied to the inverting input terminal of the op-amp. The ckt with three input signal in figure.



Summer circuit.

Step 1:- The non inverting terminal is grounded. $\therefore V_1 = 0$.

Step 2:- using the concept of virtual ground, the voltage V_2 at the inverting terminal is equal to V_1

$$V_2 = V_1 = 0.$$

Step 3:- From KCL -
At the inverting terminal

$$I_1 + I_2 + I_3 = I_f.$$

[KCL states that the sum of the currents entering a terminal must be equal to the current leaving the terminal.]

Step 4:- Replace each current by ohm's law.

$$\frac{V_{i1} - V_2}{R_1} + \frac{V_{i2} - V_2}{R_2} + \frac{V_{i3} - V_3}{R_3} = \frac{V_2 - V_o}{R_f} \quad ; \text{ put } V_2 = 0.$$

$$\frac{V_{i1}}{R_1} + \frac{V_{i2}}{R_2} + \frac{V_{i3}}{R_3} = \frac{-V_o}{R_f} \qquad \text{let } R_1 = R_2 = R_3 = R.$$

$$V_o = -\frac{R_f}{R}\left[V_{i1} + V_{i2} + V_{i3}\right] \qquad \text{if } R = R_f.$$

$$V_o = -\left[V_{i1} + V_{i2} + V_{i3}\right]$$

The significance of the negative sign is that the input signal & output signals are out of phase by 180°.

problem: ① Calculate the output of summing amplifier with $R_1 = 200K\Omega$, $R_2 = 250K\Omega$, $R_3 = 500K\Omega$ $R_f = 1000K\Omega$

$V_{i1} = -2V$, $V_{i2} = 2V$, & $V_{i3} = 1V$.

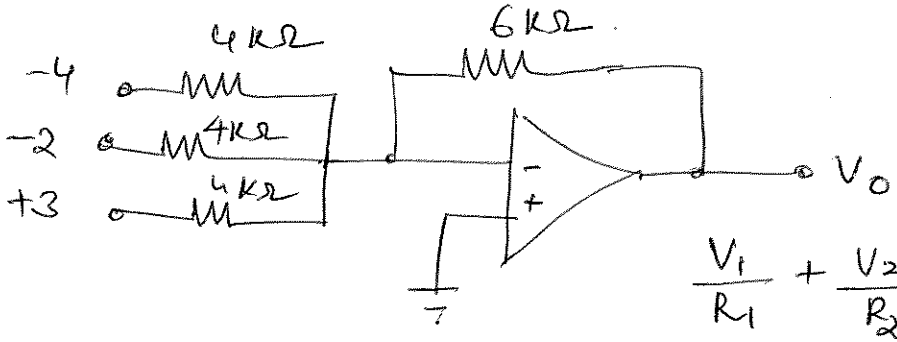
$$\frac{V_{i1}}{R_1} + \frac{V_{i2}}{R_2} + \frac{V_{i3}}{R_3} = \frac{-V_o}{R_f}.$$

$$\frac{-2}{200} + \frac{2}{250} + \frac{1}{500} = \frac{-V_o}{1000}.$$

$$\left[-0.01 + 0.008 + 0.002\right] * 1000 = -V_o.$$

$$\boxed{V_o = 0}$$

② Find the output voltage of the 3-input adder circuit shown below.



$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_o}{R_f}.$$

$$\frac{-4}{40} - \frac{2}{4} + \frac{3}{4} = \frac{-V_o}{6} \Rightarrow$$

$$6\left(-1 - 0.5 + 0.75\right) = -V_o.$$

$$6\left(-0.75\right) = -V_o.$$

$$\boxed{V_o = 4.5}$$

③ Design a adder circuit to get an output voltage of $V_o = -(3V_1 + 4V_2 + 5V_3)$ choose $R_f = 30K$.

From given expression is $V_o = -(3V_1 + 4V_2 + 5V_3)$. → (1)

$$V_o = -R_f\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

$$V_o = -\left[V_1\frac{R_f}{R_1} + V_2\frac{R_f}{R_2} + V_3\frac{R_f}{R_3}\right] \rightarrow (2)$$

By comparing eqn (1) & (2).

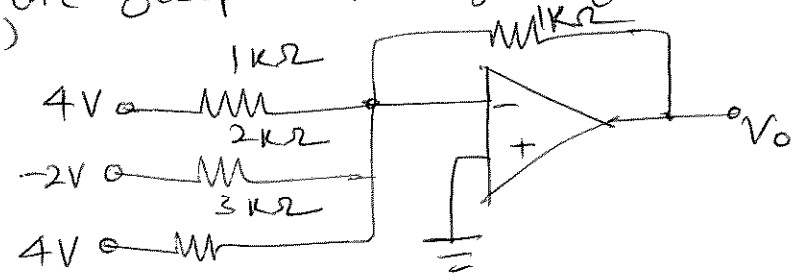
$\frac{R_f}{R_1} = 3$ $\frac{R_f}{R_2} = 4$ $\frac{R_f}{R_3} = 5$. let $R_f = 30K$.

$\frac{30}{R_1} = 3$ $\frac{30}{R_2} = 4$ $\frac{30}{R_3} = 5$.

$R_1 = 10K\Omega$ $R_2 = 7.5K\Omega$ $R_3 = 6K\Omega$

(4). Find the output voltage of op-amp circuits given. (4 Marks) VTU, June 2012

(a)



inverting summer with $R_f = 1K\Omega$.

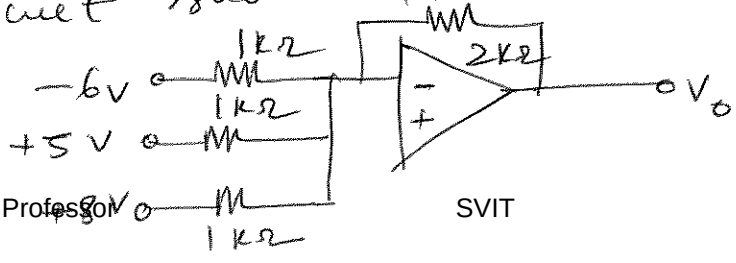
here $R_1 = 1K\Omega$, $R_2 = 2K\Omega$, $R_3 = 3K\Omega$ $V_1 = 4V$ $V_2 = -2V$ $V_3 = 4V$.

$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

$$= -\left[\frac{1\times10^3}{1\times10^3} \times 4V + \frac{1}{2} \times (-2) + \frac{1}{3} \times 4\right]$$

$$= \left[4V - 1V + 1.33V\right] = 4.33\ V.$$

(b). Determine the output voltage of the op-amp circuit shown below. VTU: June 12. 4 Marks.

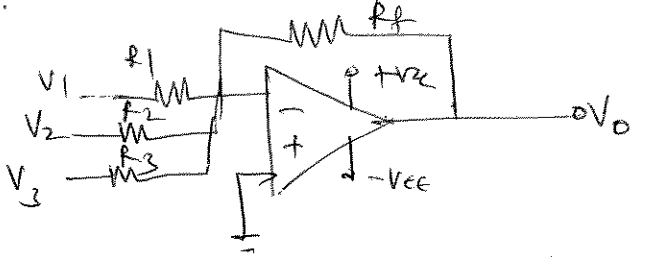


$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

$$= -\left(\frac{2}{1}\times(-6) + \frac{2}{1}\times5 + \frac{2}{1}\times8\right)$$

$$= -14\ V$$

(7) Calculate the ~~output~~ voltages of the circuit given below. VTU Jan 13 (5M)



let $V_o = -(0.1V_1 + 0.5V_2 + 20V_3)$

$R_f = 10K\Omega$

The output of inverting summer is

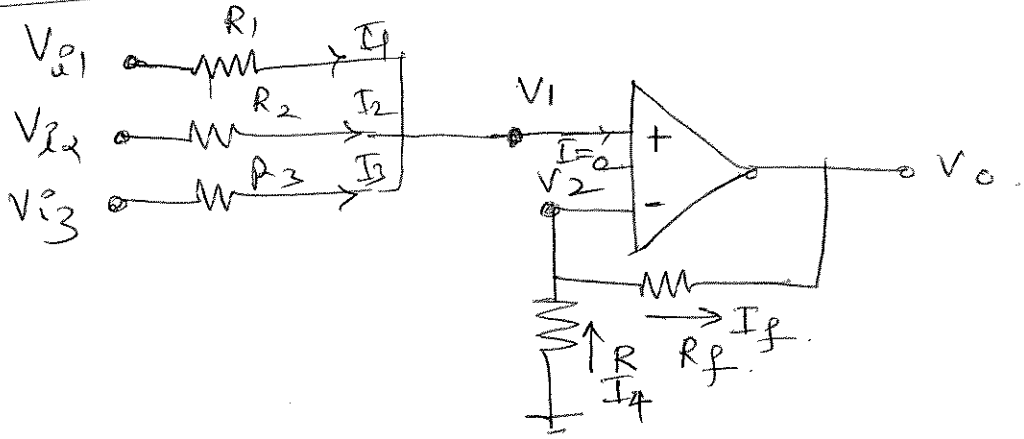
$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

$$= -0.1V_1 + 0.5V_2 + 20V_3.$$

$\frac{R_f}{R_1} = 0.1 \quad \frac{R_f}{R_2} = 0.5 \quad \frac{R_f}{R_3} = 20.$ if $R_f = 10K\Omega$.

$R_f = 10K\Omega$, $R_1 = 100K\Omega$ $R_2 = 20K\Omega$, $R_3 = 0.5K\Omega$.

Non-inverting Summing circuit



non-inverting summing circuit.

Here multiple input signals are connected to the non-inverting terminal - Each input signal is connected to a seperate resistor.

- The output terminal is Connected to inverting terminal through a resistor. R_f: it provided negative feedback.
- The inverting terminal is also Connected to ground through a resistor.

Step 1 : The voltage V_1 at the non-inverting terminal.

many inputs are connected to the non-inverting terminal. The voltage V_1 found by applying KCL. KCL states that sum of the currents entering terminal must be equal to the current leaving the terminal.

$$I_1 + I_2 + I_3 = 0.$$

$$\frac{V_{i1} - V_1}{R_1} + \frac{V_{i2} - V_1}{R_2} + \frac{V_{i3} - V_1}{R_3} = 0.$$

let $R_1 = R_2 = R_3 = R$.

$$\frac{V_{i1} - V_1}{R} + \frac{V_{i2} - V_1}{R} + \frac{V_{i3} - V_1}{R} = 0$$

$$3V_1 = V_{i1} + V_{i2} + V_{i3}.$$

$$\boxed{V_1 = \frac{V_{i1} + V_{i2} + V_{i3}}{3}}$$

Step 2 :- using the concept of virtual ground, the voltage V_2 at the inverting terminal is equal to V_1.

$$V_2 = V_1 = \frac{V_{i1} + V_{i2} + V_{i3}}{3}.$$

Step 3 :- apply KCL at the inverting terminal. Let I_4, I_f are the current through resistors R_1, R_f respectively.

$$I_4 = I_f.$$

Step 4 :- Replace each current by ohm's law.

$$\frac{0 - V_2}{R} = \frac{V_2 - V_o}{R_f}$$

$$\frac{-V_2}{R} = \frac{V_2}{R_f} - \frac{V_0}{R_f}$$

$$\frac{V_0}{R_f} = \frac{V_2}{R_f} + \frac{V_2}{R}$$

$$\frac{V_0}{R_f} = V_2\left[\frac{R+R_f}{R_f * R}\right]$$

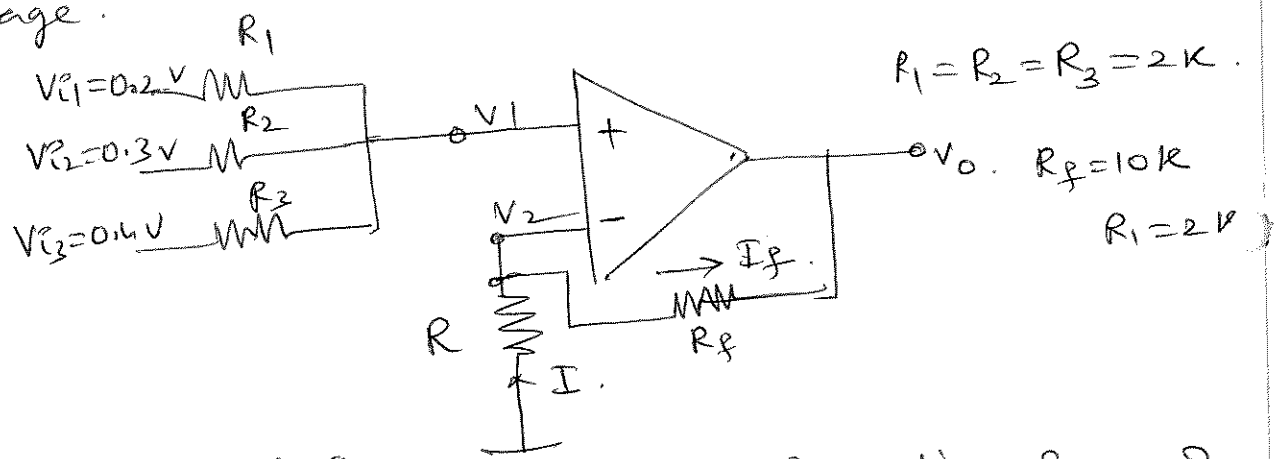
$$V_0 = V_2\left[\frac{R+R_f}{R_f * R}\right] R_f$$

$$V_0 = V_2\left[1 + \frac{R_f}{R}\right]$$

$$V_0 = \left(\frac{V_{i1}+V_{i2}+V_{i3}}{3}\right)\left[1 + \frac{R_f}{R}\right]$$

If $\boxed{R_f = 2R_1}$, Then $\boxed{V_0 = V_{i1}+V_{i2}+V_{i3}}$

problem ① for the following circuit, find output voltage.



$R_1 = R_2 = R_3 = 2K$.

$R_f = 10K$

$R_1 = 2K$

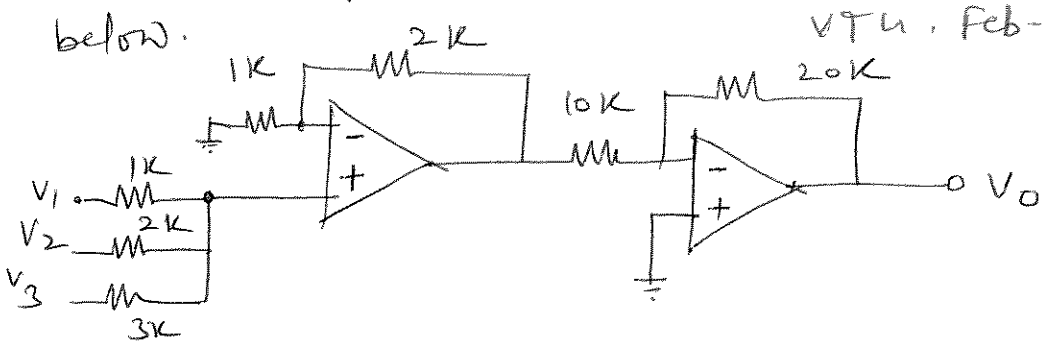
The given circuit is an non-inverting Summer.

$$V_0 = \left\{\frac{V_{i1}+V_{i2}+V_{i3}}{3}\right\}\left[1 + \frac{R_f}{R}\right]$$

$$V_0 = \frac{0.9}{3} \times \left[1 + \frac{10}{2}\right]$$

$$\boxed{V_0 = 1.8\,V}$$

(2) Calculate the output voltage of the circuit given in fig. below. VTU, Feb-09, (8M)



$V_1 = 1V$, $V_2 = 2V$ $V_3 = 3V$.

Soln:- By using super position theorem, & consider each input acting seperately.

Case (1). V_1 acting V_2 & V_3 grounded.

This is non inverting amplifier with $R_f = 2K\Omega$, $R_1 = 1K\Omega$.

Then $2K\Omega \,||\, 3K\Omega = \frac{2\times 3}{2+3} = \frac{6}{5} = 1.2K\Omega$

$$V_B = \frac{V_1(2K\Omega \,||\, 3K\Omega)}{1*K\Omega + [2K\Omega + 3K\Omega)} = \frac{V_1 * 1.2K}{1K + 1.2K}$$

$$V_B = 0.5454\, V_1$$

$$V_{O1} = \left[1 + \frac{R_f}{R_1}\right] V_B.$$

$$= \left[1 + \frac{2}{1}\right] * 0.5454\, V_1 = 1.6363\, V_1$$

Case (2):- V_2 acting V_1 & V_3 grounded. $1K\Omega \,||\, 3K\Omega = 750\Omega$.

$$V_B = \frac{V_2 \times 750}{2K + 750} = 0.2727\, V_2.$$

$$V_{O2} = \left[1 + \frac{R_f}{R_1}\right] V_B = \left[1 + \frac{2\times 10^3}{1\times 10^3}\right] 0.2727\, V_2$$

$$= 0.8181\, V_2.$$

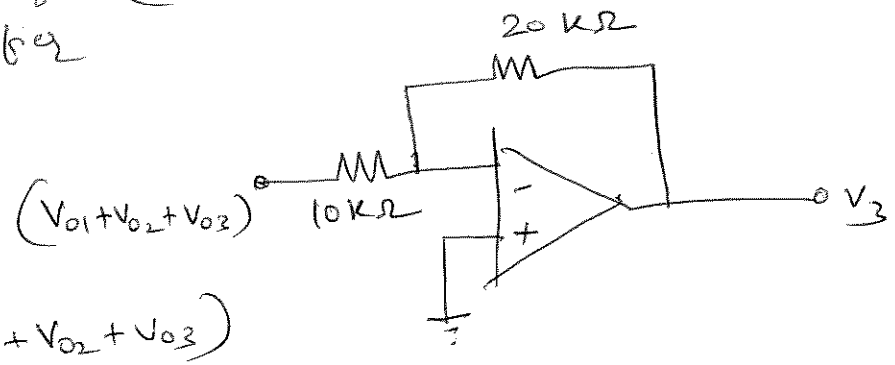
Case (3):- V_3 acting V_1 & V_2 grounded, $1K\Omega \,||\, 2K\Omega \,||\, = 666.67\Omega$

$$V_B = \frac{V_3 \times 666.67}{[3\times 10^3 + 666.67]} = 0.1818\, V_3.$$

$$\therefore V_{O3} = \left[1 + \frac{R_f}{R_1}\right] V_B = \left[1 + \frac{2\times 10^3}{1\times 10^3}\right] \times 0.1818\, V_3$$

$$V_{O3} = 0.5454\, V_3$$

Now the voltage $(V_{o1}+V_{o2}+V_{o3})$ is applied to inverting terminal of amplifier



$$\therefore V_o = \frac{-R_f}{R_1}(V_{o1}+V_{o2}+V_{o3})$$

$$= \frac{-20}{10}\left[1.6363V_1 + 0.8181V_2 + 0.5454V_3\right)$$

$$\therefore V_o = (-3.2726V_1 - 1.6362V_2 - 1.0909V_3)$$

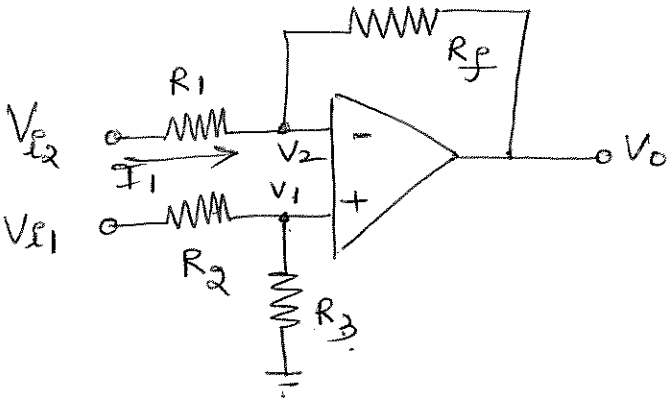
with $V_1 = 1V$, $V_2 = 2V$ $V_3 = 3V$.

$$\therefore V_o = -9.8178\ V$$

Subtractor or Difference amplifier

VTU. Aug 04, 05 (M-S)

The circuit diagram of subtractor is shown in figure.



Difference amplifier.

- One of the input voltage is connected to the non inverting terminal through a potential divider network R_2 and R_3 as shown in figure.
- Another input voltage is connected to the inverting terminal through a resistor R_1
- The resistor R_f connects the output terminal to inverting input terminal to provide negative feed back.

Step 1 :- At the non-inverting terminal, two resistor are connected. the voltage across one of the resistor is found by applying voltage divider rule.

$$V_1 = V_{i1} \frac{R_3}{R_2+R_3}$$

step 2 :- using the concept of virtual ground, the voltage V_2 at the inverting terminal is equated to the voltage at non inverting terminal.

$$V_2 = V_1 = V_{i1} \frac{R_3}{R_2+R_3}.$$

step 3 : By applying KCL at the inverting terminal. Let I_1, I_f are the current through resistors R_1, R_f.

$$I_1 = I_f.$$

step 4 : Replace the each current by ohm's law.

$$\frac{V_{i2} - V_2}{R_1} = \frac{V_2 - V_0}{R_f}$$

$$\frac{V_{i2}}{R_1} - \frac{V_2}{R_1} = \frac{V_2}{R_f} - \frac{V_0}{R_f}.$$

$$\frac{V_0}{R_f} = \frac{V_2}{R_f} + \frac{V_2}{R_1} - \frac{V_{i2}}{R_1}$$

$$\frac{V_0}{R_f} = V_2 \left[\frac{R_f + R_1}{R_f * R_1} \right] - \frac{V_{i2}}{R_1}$$

$$V_0 = V_2 \left[\frac{R_f + R_1}{R_1} \right] - V_{i2} \frac{R_f}{R_1}$$

$$V_0 = V_{i1} \left(\frac{R_3}{R_2+R_3} \right) \left(\frac{R_f + R_1}{R_1} \right) - V_{i2} \cdot \frac{R_f}{R_1} \quad ; \text{ let } R_3 = R_f \quad R_2 = R_1$$

$$V_0 = V_{i1} \left(\frac{R_f}{R_1+R_f} \right) \left(\frac{R_f+R_1}{R_1} \right) - V_{i2} \cdot \frac{R_f}{R_1} = \frac{R_f}{R_1} V_{i1} - \frac{V_{i2} R_f}{R_1}$$

$$\boxed{V_0 = \frac{R_f}{R_1} (V_{i1} - V_{i2})}$$

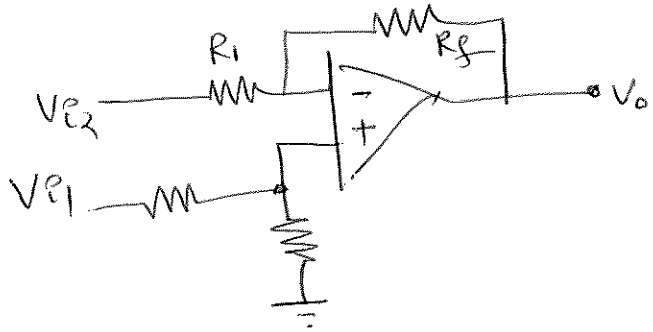
$\frac{R_f}{R_1}$ = Voltage gain.

If $R_f = R_1$, the voltage gain becomes unity, then the circuit is subtractor circuit.

If $R_f > R_1$, then voltage gain becomes greater than unity and the circuit is called difference amplifier.

problem.

(1) For the given op-amp circuit find the output voltage. Take $R_f = R_3 = 12K\Omega$ $R_1 = R_2 = 3K\Omega$, $V_{i1} = 2.1V$, $V_{i2} = 0.9V$.

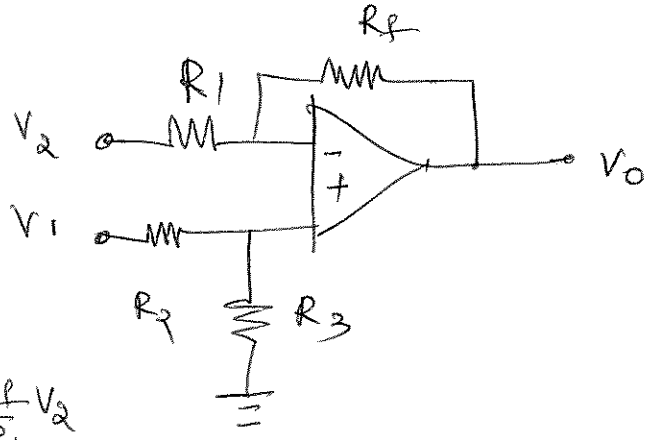


The given circuit is a difference amplifier.

$$V_o = \frac{R_f}{R_1}\left[V_{i1} - V_{i2}\right]$$

$$= \frac{12K}{3K}\left[2.1 - (0.9)\right] = 12V.$$

(2) Design a suitable circuit to realize the given expression $V_o = 0.4V_1 - 8V_2$. where V_1 & V_2 are the input voltages Draw the circuit.



The expression for the output voltage is.

$$V_o = \frac{R_3}{R_2+R_3}\left(\frac{R_1+R_f}{R_1}\right)V_1 - \frac{R_f}{R_1}V_2$$

$\frac{R_f}{R_1} = 8$ $\quad R_f = 8R_1$ let $R_1 = 10K\Omega$ $R_f = 80K\Omega$.

Comparing the coefficient of V_1 we get.

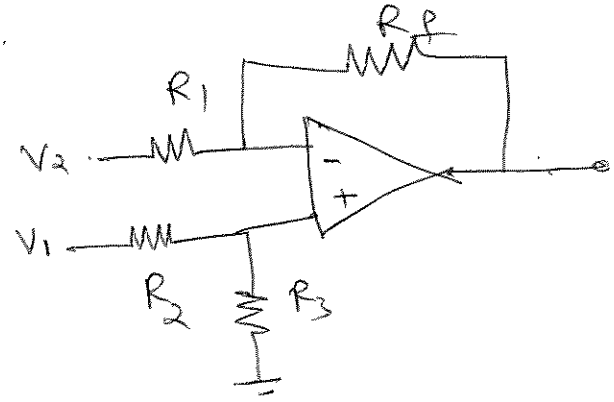
$$\frac{R_3}{R_2+R_3}\left[\frac{R_1+R_f}{R_1}\right] = 0.4 \qquad \frac{R_3}{R_2+R_3}\left[\frac{10+80}{10}\right] = 0.4$$

$\frac{R_3}{R_2+R_3} = \frac{0.4}{9} = 0.044$, $\frac{R_2+R_3}{R_3} = 22.72$ $1 + \frac{R_2}{R_3} = 22.72$ if $R_3 = 10K\Omega$

$R_2 = 21.72K\Omega$

(3) Design an op-amp circuit to get the required expression $V_o = 8(V_1 - V_2)$. → (*)

Since the 2 input voltages are subtracted, the required circuit is as follows.



Since the coefficient of V_1 & V_2 are same.

Choose $R_1 = R_2$

$R_f = R_3$

$$V_o = \frac{R_f}{R_1}(V_1 - V_2) \rightarrow (1)$$

By comparing eqn (*) & (1)

$$\frac{R_f}{R_1} = 8 \qquad R_f = 8 * R_1$$

let $R_1 = 10K\Omega$, $R_f = 80K\Omega$

---

(4) Design the op-amp circuit which can give the output as $V_o = 2V_1 - 3V_2 + 4V_3 - 5V_4$

The positive & negative terms can be added seperately using two adder then subtractor.

$2V_1 + 4V_3$, → (*) let $R_{f1} = 100K\Omega$.

$$V_{o1} = -\left(\frac{R_{f1}}{R_1}V_1 + \frac{R_{f1}}{R_3}V_3\right)$$

Comparing with (*)

$$\frac{+R_{f1}}{R_1} = 2 \qquad \frac{R_{f1}}{R_3} = 4$$

$R_1 = 50K\Omega$ $\quad R_3 = 25K\Omega$.

$3V_2 + 5V_4$, let $R_{f2} = 120K\Omega$

$$V_{o2} = -\left\{\left(\frac{R_{f2}}{R_2}V_1 + \left(\frac{R_{f2}}{R_4}\right)V_3\right\}\right.$$

$\frac{R_{f2}}{R_2} = 3$ hence $R_2 = 40K\Omega$

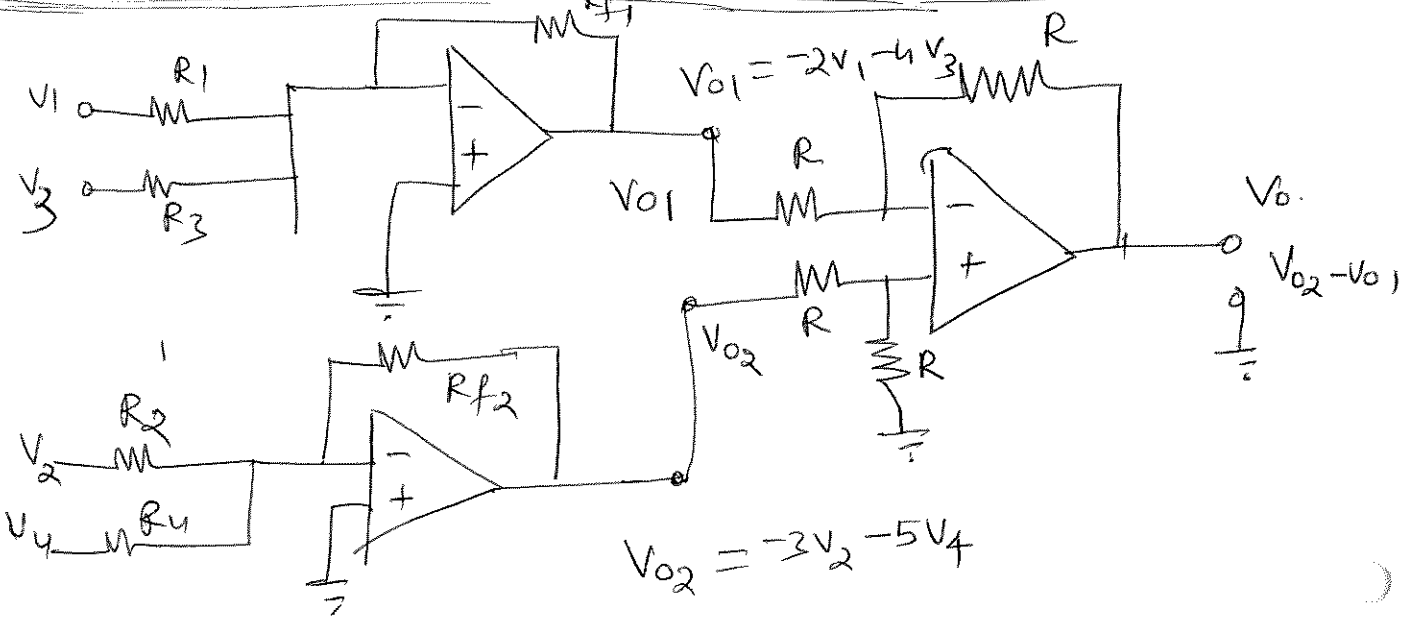
$\frac{R_{f2}}{R_4} = 5$ hence $R_4 = 24K\Omega$.

use the subtractor with all the resistances of same value of $R = 100K\Omega$.

Here $V_o = V_{o2} - V_{o1}$, where V_{o2} & V_{o1} are the two inputs of the subtractors.

$$V_o = V_{o2} - V_{o1} = -3V_2 - 5V_4 - (-2V_1 - 4V_3)$$

$$= 2V_1 - 3V_2 + 4V_3 - 5V_4.$$



Integrator: –

VTU – Mar 01, 05
Feb 03, 04
June 13.
Jan 08 – 11.

Any circuit whose output voltage is proportional to the integral of the input voltage can be defined as an integrator.

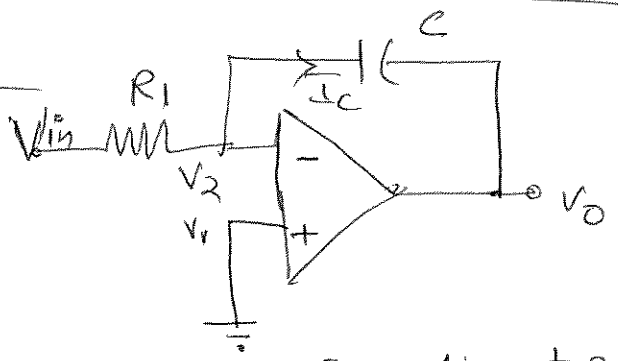
A capacitor is used for realizing the integrator. The voltage across the capacitor is.

$$V_c = \frac{1}{C}\int i_c \cdot dt.$$

i_c → is the current through the capacitor

Here the output voltage is an integration of the input voltage.

- passive integrator
  Active integrator.



The input signal is connected to the inverting terminal through a resistance R. It is inverting integrator.

- For the circuit to behave as an integrator, a capacitor is necessary. ∴ the capacitor is connected in the feedback path between the output terminal & the inverting terminal.
- The non-inverting terminal is connected to ground.

Step 1:- The voltage V_1 at the non-inverting terminal since the non-inverting terminal is grounded $V_1 = 0$.

Step 2:- From the concept of virtual ground,

$$V_2 = V_1 = 0.$$

Step 3:- apply KCL at the inverting terminal.
let I_1 be the current through R_1 & i_C is the current through capacitor.

$$I_1 = i_C$$

Step 4:- replace current (by I_1) by ohms law.

$$\frac{V_i - 0}{R} = i_C$$

$$\boxed{i_C = \frac{V_i}{R}}$$

the output voltage is $V_o = -V_C$.

$$= -\frac{1}{C}\int i_C \cdot dt$$

$$V_o = -\frac{1}{C}\int \frac{V_i}{R} \cdot dt = \frac{-1}{RC}\int V_i \cdot dt.$$

Thus output voltage is proportional to the integral of the input voltage & hence the circuit can be called integrator :-

applications :-

In analog computer
Solving the differential equation
In ramp generators
In ADCs.
Various Signal Wave shaping circuits.

problem:-

(1) A sinusoidal signal with peak value of 6mV & 2kHz frequency is applied to the input of an ideal op-amp integrator with $R_1 = 100k\Omega$, $C_f = 1\mu F$. find the output voltage.

For an ideal integrator,

$$V_o = \frac{1}{R_f C_f}\int_0^t V_{in}\,dt$$

Now $R_1 = 100k\Omega$ & $C_f = 1\mu F$, $V_{in} = V_m \sin\omega t$

where $V_{in} = 6mV$ $\omega = 2\pi f = 2\times\pi\times10^3\times2$

$= 4\pi\times10^3$ rad/sec.

$$V_o = \frac{1}{R_f C_f}\int_0^t V_{in}\,dt$$

$$= \frac{1}{100\times10^3\times1\times10^{-6}}\int_0^t 6\times10^{-3}\sin(4\pi\times10^3)\,dt$$

$$= -0.06\left[\frac{-\cos(4\pi\times10^3 t)}{4\pi\times10^3}\right]_0^t$$

$$= -4.77\times10^{-6}\left\{\cos(4000\pi t) - 1\right\}\ V$$

$$V_o = 4.77\times10^{-6}\left\{1 - \cos(4000\pi t)\right\}$$

Differentiator :-

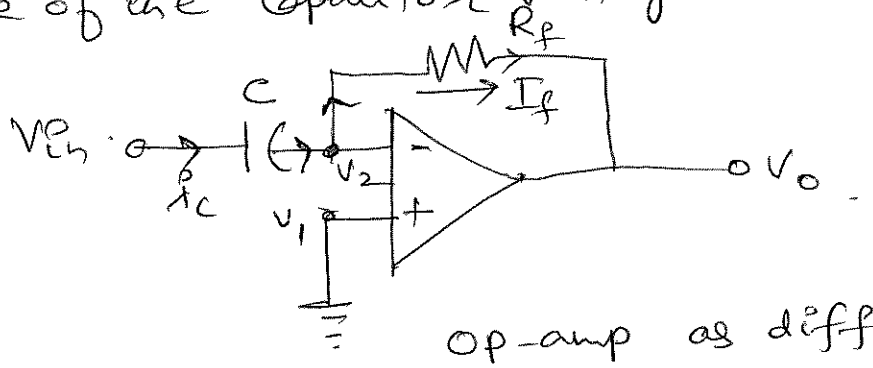
Any circuit whose output voltage is proportional to the derivative of the input voltage can be defined as a differentiator.

A capacitor is used to realize the differentiator. The voltage across the capacitor is

$$V_c = \frac{1}{C}\int i_c \cdot dt .$$

$$i_c = C \cdot \frac{d}{dt}(V_c).$$

Thus, the current through the capacitor is proportional to the derivative of the capacitor voltage.



Op-amp as differentiator.

- V_{in} is connected to inverting terminal through the capacitor C. The Resistor R_f is connected in the feedback path between the output terminal & the inverting terminal.
- The non-inverting terminal is connected to ground.

Step 1 : The voltage V_1 at the non-inverting terminal is $V_1 = 0$, since non-inverting terminal is grounded.

Step 2 :- From the concept of virtual ground, the

$$V_2 = V_1 = 0 .$$

Step 3 :- apply KCL at the inverting terminal.

Let I_f is the current through resistor R_f & i_c is the current through the capacitor

$$i_c = I_f .$$

Replace the current by ohms law

$$\frac{V_2 - V_0}{R_f} = i_c = \frac{0 - V_0}{R_f}$$

$$i_c = -\frac{V_0}{R_f}$$

let V_c is the voltage across the capacitor

$$V_c = V_{in} - V_2$$

$$V_c = V_{in} - 0$$

$$\boxed{V_c = V_{in}}$$

$$i_c = C \cdot \frac{d}{dt} V_c \quad \text{W.R.T} \quad i_c = -\frac{V_0}{R}$$

$$-\frac{V_0}{R} = C \frac{d}{dt} \cdot V_c$$

$$\boxed{V_0 = -RC \cdot \frac{d}{dt}(V_c)} \qquad V_c = V_{in}$$

$$\boxed{V_0 = -RC \frac{d}{dt}(V_{in})}$$

Note:- applⁿ of differentiator

In the wave shaping circuits to detect the high frequency components in the input signal.

As a rate of change of detector in FM demodulators.

Thus, the output voltage is proportional to the derivative of the input voltage & hence the circuit can be called a differentiator.

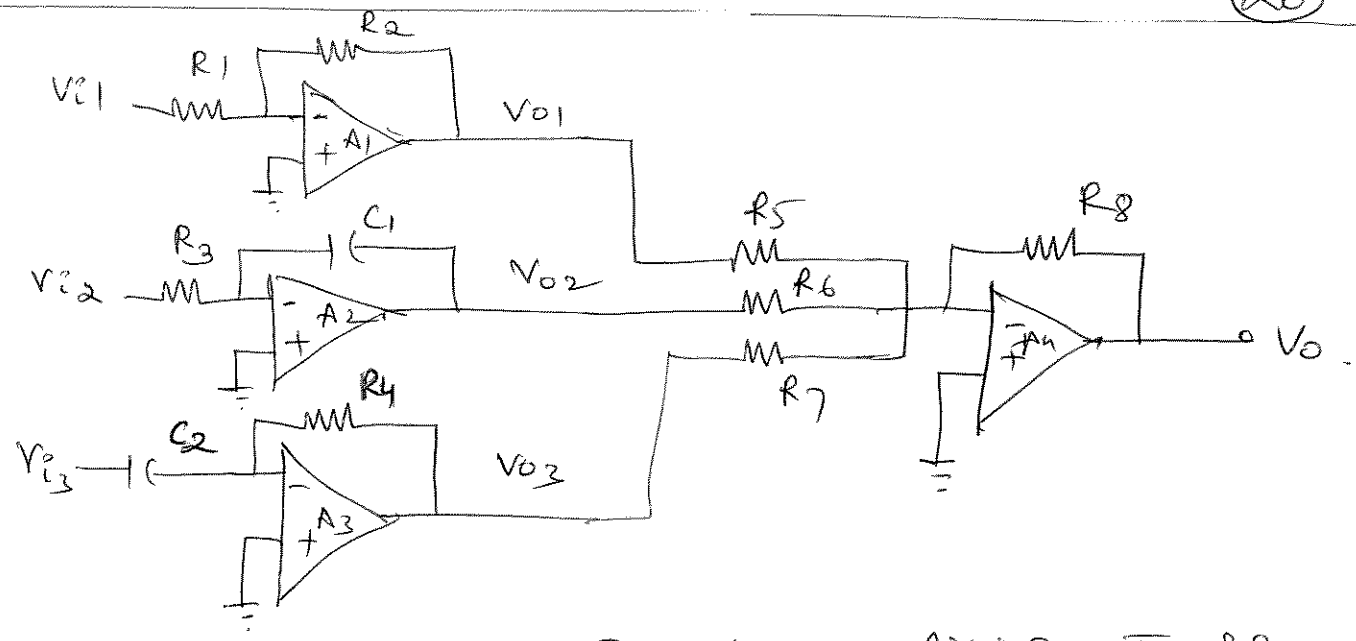
-ve sign shows that the op-amp is connected as an inverting configuration.

Problem "Extra sloved Examples"

(1). For the following circuit Find the expression for the output voltage.

given. $R_1 = R_2 = R_5 = R_6 = R_7 = R_8 = 1K\Omega$

$R_3 = R_4 = 1M\Omega \quad C_1 = C_2 = 1\mu f.$



The op-amp A_1 is an inverting amplifier. Therefore the output of A_1 can be written as

$$V_{o1} = -\frac{R_2}{R_1} v_{i1} = -v_{i1}.$$

The op-amp A_2 is an inverting integrator.

The output of A_2

$$V_{o2} = -\frac{1}{R_3 C_1} \int v_{i2} \cdot dt$$

$$= \frac{-1}{1\times10^{6}\times1\times10^{-6}} \int v_{i2} \cdot dt$$

$$= -\int v_2 \cdot dt$$

The op amp A_3 is an inverting differentiator. The output of A_3 is

$$V_{o3} = -R_4 C_2 \frac{d}{dt}(v_{i3})$$

$$= -1\times10^{6}\times1\times10^{-6} \frac{d}{dt}(v_{i3})$$

$$V_{o3} = -\frac{d}{dt}(v_{i3})$$

The op-amp A_4 is inverting summer.

The output of A_4 is.

$$V_o = \frac{-R_8}{R_5}\left[V_{o1} + V_{o2} + V_{o3}\right]$$

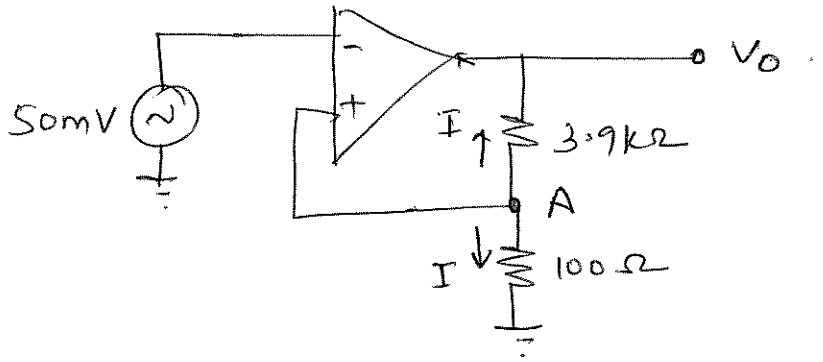
$R_8 = R_5$.

$$= \left[-V_{i1} + \left(-\int V_{i2}\cdot dt\right) + \frac{d}{dt}\left(-V_{i3}\right)\right]$$

$$\boxed{V_o = V_{i1} + \int V_{i2}\cdot dt + \frac{d}{dt} V_{i3}}$$

Problems.

(1). Find the output & closed loop gain of the op-amp ckt.



$V_{in} = 50mV$.

$$\underset{(100\Omega)}{I} = \frac{50}{100} = 0.5\ mA.$$

No current flows into the +ve terminal

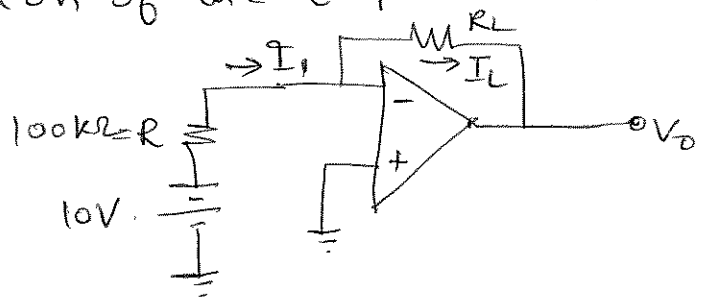
$$I(3.9K) = 0.5\ mA$$

$$V_o = V_A + 3.9 \times 0.5 \times 10^3 \times 10^{-3}.$$

$$= 50m + 1950m = \underline{2000mV}.$$

$$A_F = \frac{V_o}{V_{in}} = \frac{2000}{50} = \underline{40}.$$

(2) In the figure R_L is the transducer resistance which can vary from 1 KΩ to 10 KΩ. Determine the range of variation of the output voltage.



$$I_1 = I_L$$

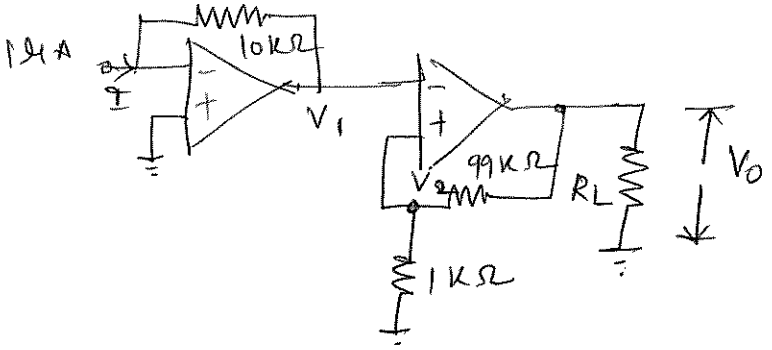
$$\frac{10}{100} = -\frac{V_o}{R_L}$$

$$V_o = \frac{-R_L}{10}$$

$R_L = 1K\Omega$, $V_o = -0.1V$ } range.

$R_L = 10K\Omega$, $V_o = -1V$ }

(3) Find the V_o of op-amp circuit of figure below.



$$V_1 = -1\times10^{-6}\times10\times10^{3} = -0.01V$$

because virtual ground concept

$$V_2 = V_1 = -0.01V$$

Applying KCL at node (2)

$$\frac{V_2}{1k} + \frac{V_2 - V_o}{99k} \Rightarrow V_o = (99+1)V_2$$

$$= 100 * -0.01$$

$$= -1.0V$$ Independent of R_L

An op-amp has a slew rate of 0.8V/μs. What is the maximum amplitude of undistorted sine wave that the op-amp can produce at a frequency of 40KHz? What is the maximum frequency of the sine wave that op-amp can reproduce if the amplitude is 3V?

(a) $S = 2\pi f V_m$.

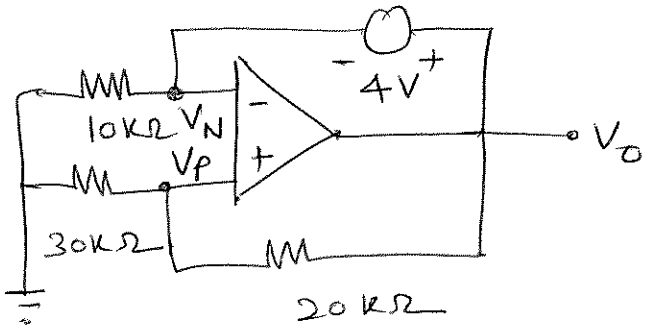
$0.8 \times 10^6 = 2\pi \times 40 \times 10^3 V_m$

$\boxed{V_m = 3.18V}$

$0.8 \times 10^6 = 2\pi f \times 3$.

$\boxed{f = 42.44KHz}$

For an op-amp circuit of figure below determine V_p, V_n, V_o and also power supplied / absorbed by the 4V source.



$V_p = \frac{30}{30+20} \cdot V_o = 0.6 V_o$.

$V_N = V_p = 0.6 V_o$

$V_N + 4 = V_o \Rightarrow 0.6 V_o + 4 = V_o$

$\boxed{V_o = 10V}$

$V_p = 0.6 V_o = 0.6 \times 10 = 6V = V_N$

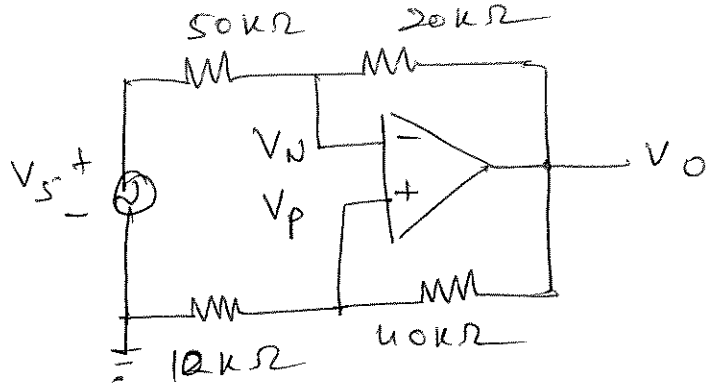
$i(10K) = \frac{6}{10} = 0.6mA$

i(4V source) = 0.6mA entering at +ve terminal

power absorbed = $p = 4 \times 0.6mA$

$\boxed{p = 2.4mW}$

For an op-amp circuit of figure find V_o if $V_s = 9V$. All resistance are in KΩ.



Soln:-

$$V_P = \frac{10}{10+40} \cdot V_o - 0.2\,V_o$$

$$V_N = 0.2\,V_o$$

By applying KCL at V_N node.

$$\frac{V_s - V_N}{50} = \frac{V_N - V_o}{20}$$

$$\frac{9 - 0.2V_o}{50} = \frac{0.2V_o - V_o}{20}$$

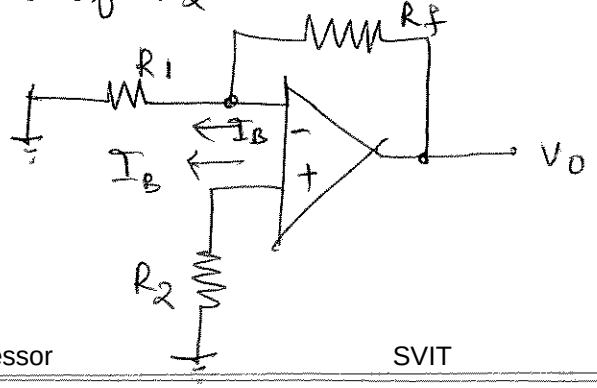
$$(9 - 0.2V_o)\,20 = (0.2V_o - V_o)\,50$$

$$180 - 4V_o = 10V_o - 50V_o$$

$$180 = 10V_o - 50V_o + 4V_o$$

$$180 = -36V_o \Rightarrow V_o = -5\ V$$

Fig below shows the effect of bias current ($I_{B1} = I_{B2} = I_B$) on the output for an inverting op-amp circuit. What value of R_2 will make $V_o = 0$?



$V_+ = R_2 I_B$.

at the -ve terminal

$$I_B = \frac{V_+}{R_1} + \frac{V_+ - V_o}{R_f}$$

$V_o = 0$.

$$\boxed{R_2 = R_1 \parallel R_F}$$

The two input voltages of an op-amp are 2V & 3V. The Common output voltage is 2mV. The difference mode o/p voltage is 9V. Find CMRR.

$V_1 = 2V \quad V_2 = 3V \qquad A_C = A_D = ?$

$V_{c.mo} = 2mV. \qquad V_{dmo} = 9V.$

$$A_C = \frac{V_{CM.O}}{V_{CM\,in.}} = \frac{2mV}{(2+3)/2} = 0.8 \times 10^{-3}$$

$$A_d = \frac{V_{dm.o}}{V_{dm.in}} = \frac{9V}{(3V-2V)} = 9.$$

$$CMRR = \frac{A_d}{A_C} = 9/0.8\times10^{-3} = 11250.$$

(*) An operational amplifier has two input voltage of 6V and 3V. The difference mode output voltage is 10V find the total output voltage. Find the Common mode voltage gain & total output voltage Take CMRR = 10,000.

$V_{id} = V_1 - V_2 = 3V \qquad A_d = \frac{V_{od}}{V_{id}} = \frac{10}{3} = 3.33.$

$V_{(CM)} = \frac{V_1 + V_2}{2} = 4.5V$)

$CMRR = \frac{A_d}{A_C}$

$A_C = \frac{3.33}{10000} = 3.33\times10^{-4}$

$V_o = V_{o(cm)} + V_{od}$.

$= (3.33\times10^{-4} \times 4.5 + 3.33 \times 3$

$= 0.001499 + 9.99$

$= 9.991499\ V$

Module -4

BJT Applications, Feedback Amplifiers and Oscillators

BJT as an amplifier, BJT as a switch
Transistor switch circuit to switch ON | OFF an LED and a lamp in a power circuit using a relay [refer 4.4 and 4.5 of Text 2).

Feedback Amplifiers

Principle, Properties & Advantages of Negative Feedback, Types of feedback, Voltages series feedback, gain stability with feedback (7.1-7.3 of Text 1)

Oscillators -

Barkhausen's criteria for oscillation, RC phase shift oscillator, Wien Bridge oscillator (7.7-7.9 of Text 1)

IC 555 Timer and Astable oscillator using IC 555 (17.2 and 17.3 of Text 1)

[RBT Levels: L1, L2 & L3)

BJT as an amplifier

Amplification is the process of linearly increasing the amplitude of an electrical signal and is one of the major properties of a transistor.

BJT exhibits high current gain called β.

When a BJT is biased in the active (or linear) region. the Base-Emitter (BE) junction has a low resistance due to forward bias & the Base-Collector (BC) junction has a high resistance due to reverse bias.

Representation of DC and AC Quantities

- Here italic capital letters are used for both dc and ac currents (I) and voltage (V).
- Ac current & voltages are always rms values unless stated otherwise.
- lower case i & v used for instantaneous values of current and voltage respectively.
- DC quantities always carry an uppercase roman (nonitalic) subscript.

  Example - I_B, I_C, and I_E are DC Transistor currents

  V_{BE}, V_{CB}, and V_{CE} are DC voltages from one terminal to other.

  V_B, V_C, V_E represents dc voltages from the transistor terminal to ground.

* AC & all time varying quantities carry a lowercase italic subscript.

Example:- I_b, I_c, and I_e are ac transistor currents.

V_{be}, V_{cb} and V_{ce} all ac voltages from one terminal to other.

V_b, V_c & V_e are ac voltages from transistor terminal to ground.

* Transistors have internal ac resistance that are designated by lowercase r' with an appropriate subscript.

Eg. r'_e → internal ac emitter resistance.

* Circuit resistance external to transistor itself use the standard italic capital R with a subscript to identifies the resistance as dc or ac.

Eg. R_E ⇒ external dc emitter resistance

R_e ⇒ external ac emitter resistance.

Voltage amplification

In Bipolar junction Transistor, In common emitter configuration, the output current and Input current relationship is given by

$$I_C = \beta I_B$$

i,e transistor amplifies current because the collector current is equal to the base current multiplied by current gain.

Here I_B is very small compared to collector current (I_C) and emitter current (I_E). hence Here

$$I_C \simeq I_E$$

Basic transistor amplifier circuit with ac source voltage V_s and dc bias voltage V_{BB} superimposed is shown in figure ①.

V_s is superimposed on the V_{BB} by capacitive coupling. The dc bias voltage V_{CC} is connected to the collector through the resistor R_C.

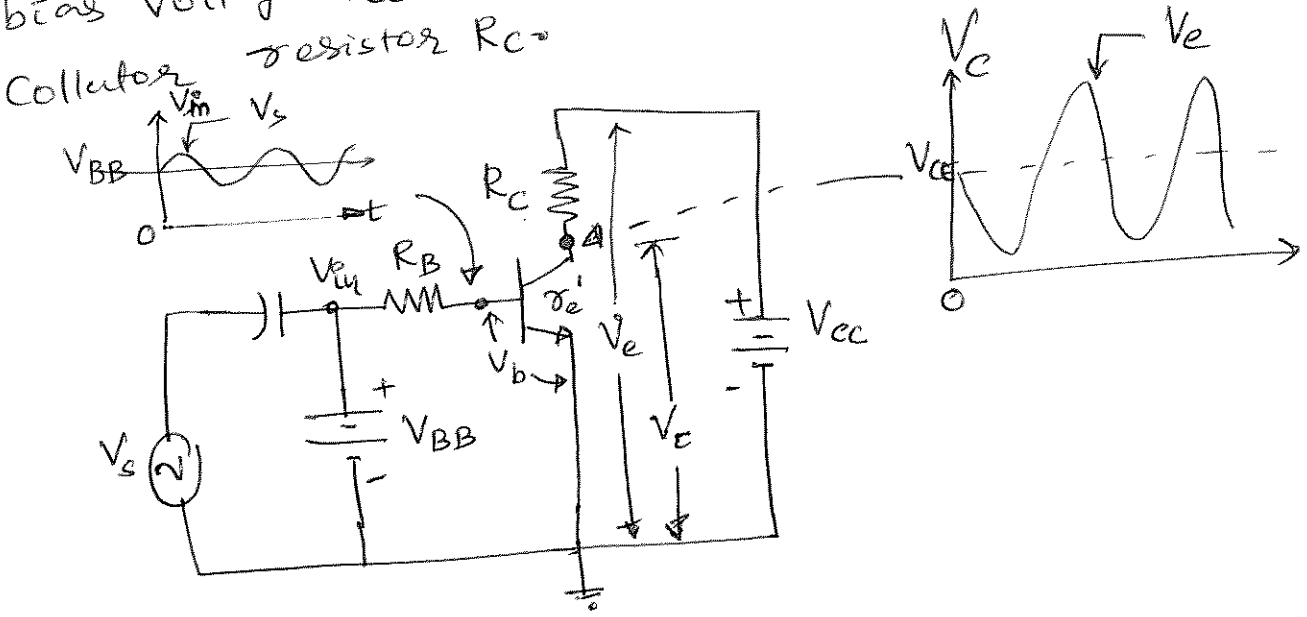


Fig ① Transistor amplifier circuit
Common emitter configuration.

The ac input voltage produces an ac base current, which results in a much larger ac collector current.

The ac collector current produces an ac voltage across R_C, thus producing an amplified but inverted, reproduction of ac input voltage in the active region of operation.

The forward biased-base emitter junction presents a very low resistance to the ac signal. This internal ac emitter resistance is designated r_e' in fig ① & appears in series with R_B. The ac base voltage is

$$V_b = I_e r_e'$$

The ac collector voltage V_c, equals to voltage drop across the R_C.

$$V_c = I_c R_C$$

Here $I_C \approx I_e$, ac collector voltage is

$$V_c \cong I_e R_C$$

V_b is given by apply KVL to input side.

$$V_S - V_b - I_b R_B$$

$$V_b = V_S - I_b R_B.$$

Here V_C is transistor ac voltage. For a transistor voltage gain is defined as the ratio of the output voltage to the input voltage.

The ration of V_c to V_b is ac voltage gain A_v of transistor.

$$A_v = \frac{V_c}{V_b}.$$

Substitute $V_c = I_e R_C$ & $V_b = I_e r_e'$

$$A_V = \frac{I_e R_C}{I_e r_e'}$$

$$\boxed{A_v \cong \frac{R_C}{r_e'}} \longrightarrow (x).$$

equation (x) shows that the transistor provides amplification in the form of voltage gain, which is dependant on the values of R_C and r_e'.

R_C is greater than r_e' hence the output voltage is greater than input voltage. hence Transistor in CE mode is also a very good voltage amplifier.

Determine the voltage gain and the ac input voltage in figure. if $r_e' = 50\Omega$.

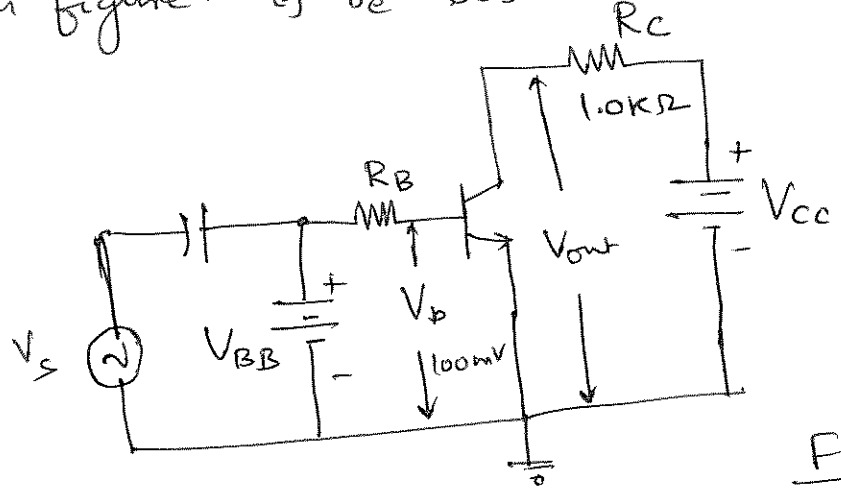


Fig ②.

The voltage gain is

$$A_v \cong \frac{R_c}{r_e'} = \frac{1.0K\Omega}{50\Omega} = 20.$$

Therefore, the ac output voltage is

$$V_{out} = A_v V_b$$

$$= 20 * 100mV = 2V_{rms}$$

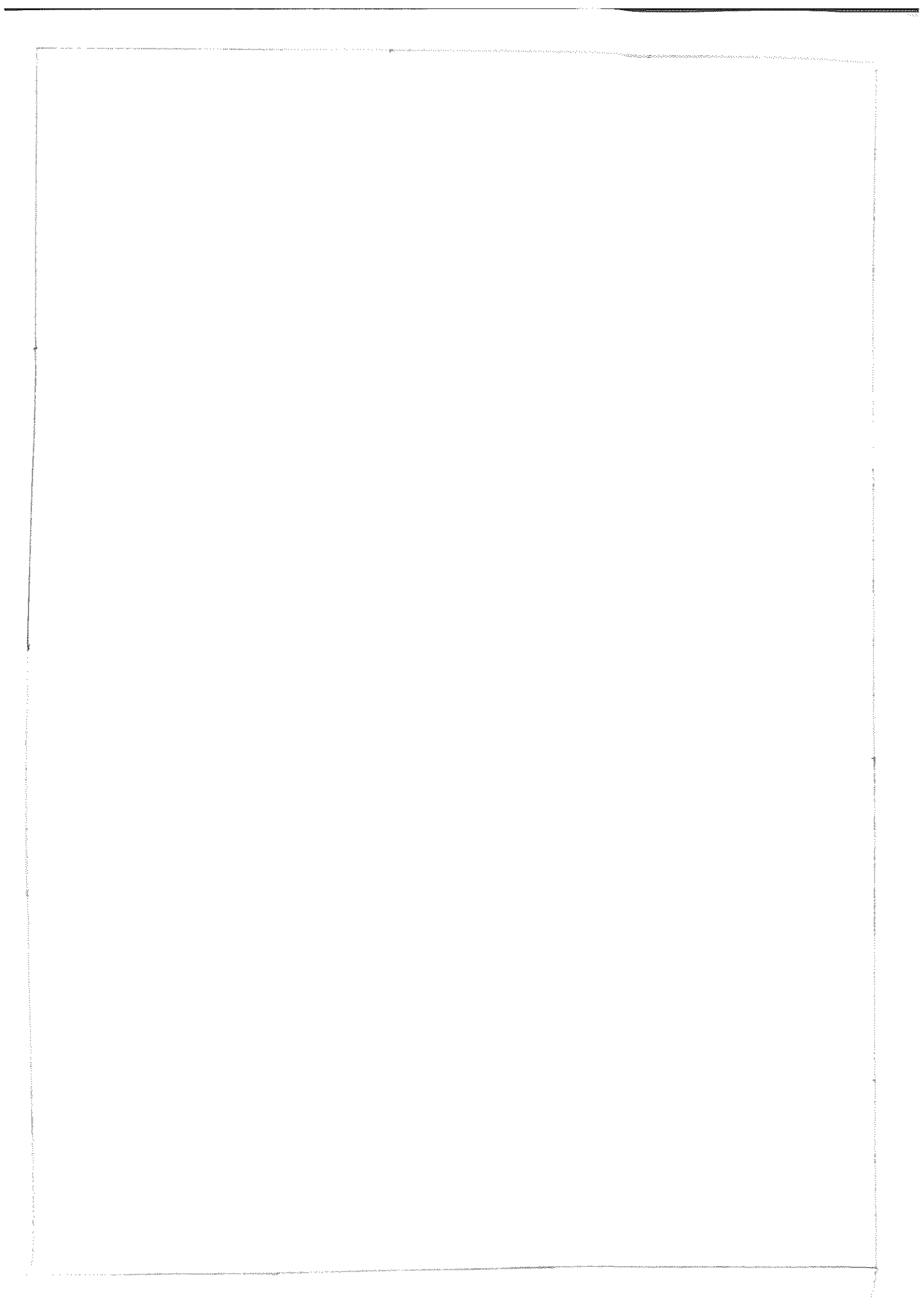
② Determine the value of R_c in fig ① when it will take to have a voltage gain of 50.

$R_c = ?$ $\quad A_v = 50, \quad r_e' = 50$

$A_v = \frac{R_c}{r_e'}$ $\quad R_c = A_v * r_e' = 50 * 50$

$= 2500$

$R_c = 2.5K\Omega$



The BJT as a Switch

The first application of BJT as a linear amplifier. The second major application area is BJT as a switch. For first application BJT will be in Active region of operation. For second application BJT normally operated alternatively in cutoff and Saturation.

When transistor is applied with external voltage i,e Biased, the transistor works in one of the following three regions. They are

1. active region
2. cut off region
3. Saturation region.

Region.	Emitter – Base Junction	Collector - Base Junction
1. Active	Forward biased	Reverse Biased
2. cut-off	Reverse biased	Reverse biased
3. Saturation	Forward biased	Forward biased.

For Normal operation of transistor, Base - emitter junction is forward biased and Collector - Base is reverse biased.

Switching operation.

Figure (3) shows the Basic operation of a BJT as a switching device.

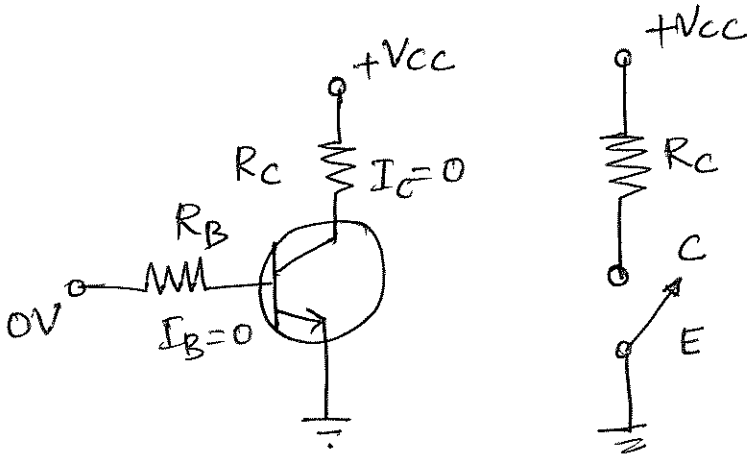
In fig(a), the transistor is operated in the cut off region because Base - emitter junction is not forward Biased.

In this case, transistor is ideally, an open between collector and emitter, as indicated in equivalent ciruit.

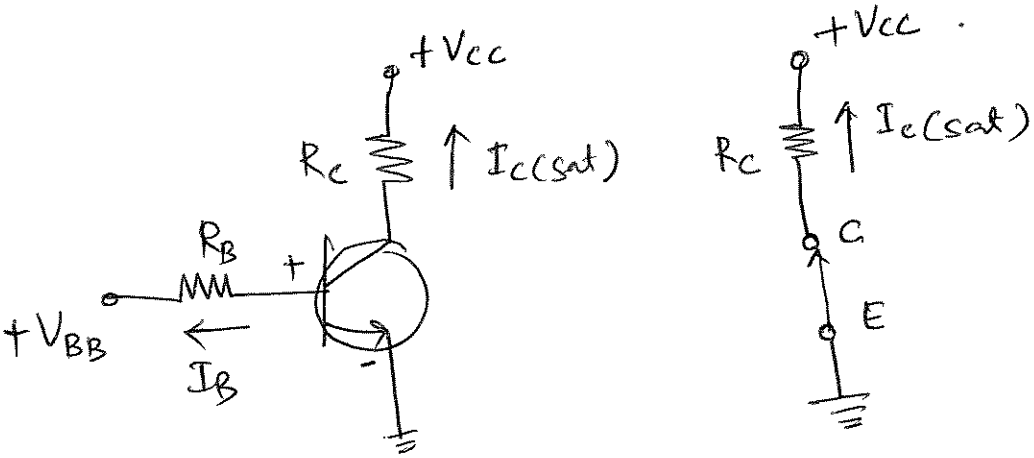
In Figure 3 (b). transistor is in the Saturation region because the base emitter junction and base-collector junction are forward biased and the base current is made large enough to cause the collector current to reach its saturation value.

The Transistor acts as a closed switch, hence there is a short between collector & emitter, as shown in equivalent circuit.

Here a small voltage drop appears across the transistor which is saturation voltage. $V_{CE(sat)}$.



(a) Transistor is in cut off region - open switch.



(b). Transistor in Saturation - closed switch.

Figure (3). Switching action of an ideal Transistor.

In cut-off regions of operation, neglecting leakage current, all of the currents are zero, and V_{CE} is equal to V_{CC}

$$V_{CE(cutoff)} = V_{CC}$$

During saturation, the base-emitter junction is forward biased and there is enough base current to produce a maximum collector current, the transistor is saturated.

Apply KVL to equivalent circuit.

$$V_{CC} - I_{C(sat)}R_C - V_{CE(sat)} = 0.$$

Then. collector saturation current is given by

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

$V_{CE(sat)} \ll V_{CC}$. Hence can be neglected.

$$I_{C(sat)} \cong \frac{V_{CC}}{R_C}.$$

The minimum value of base current needed to produce Saturation is.

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}}$$

Normally I_B. value chosen will be greater than $I_{B(min)}$ to ensure that the transistor is Saturated.

Note:- The ratio of output current I_C with respect to input current I_B is called as Common-emitter current gain β.

$$\beta = \frac{I_C}{I_B}$$

problem:

For the transistor circuit shown figure (4).

(a) what is V_{CE} when $V_{in} = 0V$?

(b) what minimum value of I_B is required to saturate this transistor if β_{dc} is 200? neglet $V_{CE(sat)}$)

(c) Calculate the maximum value of R_B when $V_{in} = 5V$.

Solution:-

(a) When $V_{IN} = 0V$, the transistor is in cutoff mode (acts as open switch).

$$V_{CE} = V_{CC} = 10V.$$

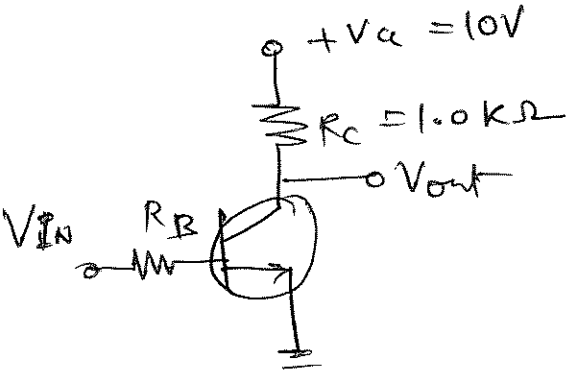


Figure (4)

(b) Since $V_{CE(sat)}$ is neglated $= 0V$

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10V}{1.0K\Omega} = 10mA.$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}} = \frac{10mA}{200} = 50\mu A.$$

(c) when the Transistor is on, $V_{BE} = 0.7V$. The voltage across R_B is

$$V_{R_B} = V_{IN} - V_{BE} = 5V - 0.7V$$
$$= 4.3V$$

using ohm's law.

$$R_{B(max)} = \frac{V_{R_B}}{I_{B(min)}} = \frac{4.3V}{50\mu A} = 86K\Omega$$

Problem (2)

Determine the minimum value of I_B required to saturate the transistor in Figure (4) if β_{DC} is 125 & $V_{CE(sat)}$ is 0.2V.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10 - 0.2}{1.0} = 9.8mA.$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{9.8mA}{125} =$$

A simple application of a transistor switch

The transistor in figure 5 is used as a switch to turn the LED on and off. For example, a square wave input voltage with a period of 2 is applied to the input as shown. when the square wave is at 0V, the transistor is in cutoff; and since there is no collector current, the LED does not emit light.

when the square wave goes to its high level, the transistor saturates. This forward biases the LEDs the resulting collator current through the LED causes it to emit light. Thus, the LED is on for 1 second and off for 1 second.

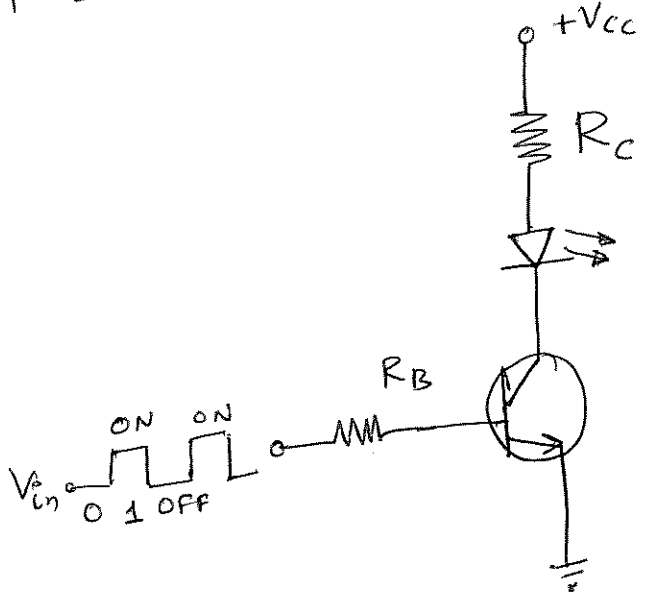


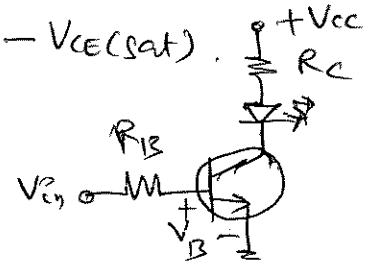
Fig (5). A Transistor used to switch an LED On and off.

Problem.

The LED in figure 5 requires 30 mA to emit a sufficient level of light. Therefore, the collector current should be approximately 30 mA. For the following circuit values, determine the amplitude of the square wave input voltage necessary to make sure that the transistor saturates. use double the minimum value of base current as a safety margin to ensure saturation.

$V_{CC} = 9V$, $V_{CE(sat)} = 0.3V$, $R_C = 220\Omega$, $R_B = 3.3K\Omega$, $\beta_{DC} = 50$, and $V_{LED} = 1.6V$

Apply KVL $\Rightarrow I_{C(sat)} R_C = V_{CC} - V_{LED} - V_{CE(sat)}$.



Solution:-

$$I_{C(sat)} = \frac{V_{CC} - V_{LED} - V_{CE(sat)}}{R_C}$$

$$= \frac{9 - 1.6 - 0.3}{220} = 32.3\ mA.$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}} = \frac{32.3\ mA}{50} = 646\ \mu A.$$

To ensure saturation, use twice the value of $I_{B(min)}$, which is 1.29 mA.

Apply KVL to input side.

$$V_{in} - I_B R_B - V_{BE} = 0.$$

$$I_B = \frac{V_{in} - V_{BE}}{R_B} = \frac{V_{R_B}}{R_B}$$

To calculate V_{in}.

$$V_{in} = V_{BE} + I_B R_B$$

$$= 0.7 + (1.29\ mA)(3.3\ K\Omega).$$

$$\boxed{V_{in} \geq 4.96V.}$$

Feedback Amplifiers

- In a feedback amplifier, voltage or current output is fedback to the input through a modifying network, which determines the magnitude & phase.
- Here a fraction of the amplifier output is fed back to the input circuit.
- This partial dependence of amplifier output on its input helps to control the output.
- A feedback amplifier has two parts namely
  - An Amplifier
  - Feedback circuit

The feedback control opposes the input (negative feedback) or aids the input (positive feedback). Characteristics of the amplifier can be altered in a desirable manner using feedback. The main purpose of amplifier is to amplify the signal without changing its characteristics except its amplitude.

The amplifier which works on the principal of feedback is known as feedback amplifier.

Feedback is a process where in a fraction of output (voltage | current) is fed back to the input. Then there will be two signals at the input i.e the original input signal & fed back signal.

There are two types of Feedback, namely

- positive feedback
- Negative feedback

This classification is based upon how and in what phase the input signal and fraction of output are mixed.

positive feedback amplifier

positive feedback amplifier as shown in figure ① The two inputs to the amplifiers are input signal and returned signal (feedback signal) are in same phase, & these signals are then added up and the resultant output increases, These circuits performing above operation are called positive feedback amplifiers.

The positive feedback is also called as regenerative or direct feedback. positive feedback causes distortion and instability in amplifiers and hence it is not suitable used as amplifier.

But positive feedback amplifier. Increases the gain & overall power of input signal hence used as oscillator circuits.

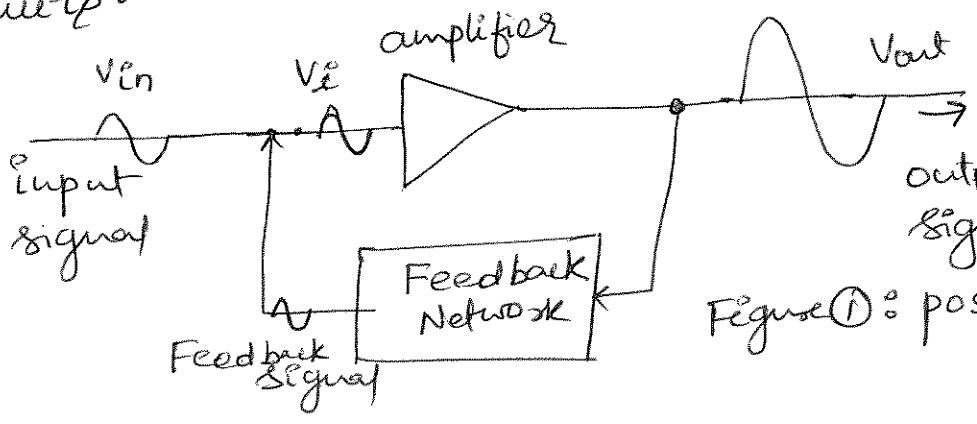


Figure ①: positive feedback amplifier

Voltage gain with positive feedback is given by

$$A_f = \frac{A}{(1 - \beta A)}$$, where $\beta \rightarrow$ Feedback factor.

From Figure (1).

$$V_i = V_{in} + \beta V_{out}$$

we know that

$$V_{out} = A \cdot V_i = A V_{in} + A\beta V_{out}$$

$$V_{out} = A V_{in} + A\beta V_{out}$$

$$A V_{in} = V_{out} - A\beta V_{out}$$

$$V_{out}(1 - A\beta) = A \cdot V_{in}$$

$$\boxed{A_F = \frac{V_{out}}{V_{in}} = \frac{A}{1 - \beta A}}$$

Negative feedback amplifier :-

In negative feedback amplifier, the feedback signal (returned signal) has phase opposite to the input signal, the net input signal is a difference of input and feedback signals. Here the negative feedback is also called as inverse or degenerative feedback.

Negative feedback reduces the overall gain of the amplifier but it has numerous advantages such as gain stability, less distortion hence widely used as amplifier circuit applications.

The figure ② shows the negative feedback amplifier. The voltage gain with negative feedback is given by

$$A_f = \frac{A}{1+\beta A} \qquad \beta \rightarrow \text{feedback factor.}$$

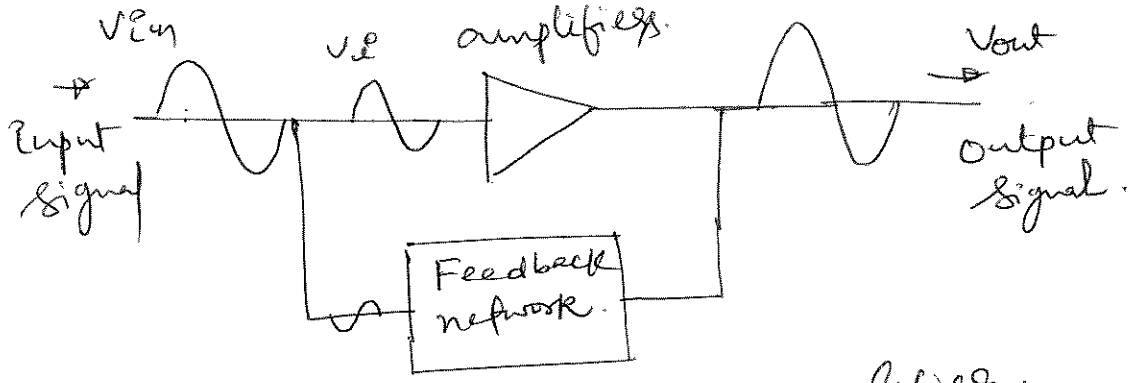


Figure ②. Negative feed back amplifier.

$$A_F = \frac{V_{out}}{V_{in}}$$

$$V_i = V_{in} - \beta V_{out}$$

$$V_{out} = V_i \cdot A_F.$$

$$V_{out} = A * \{V_{in} - \beta V_{out}\}$$

$$V_{out} + A\ \beta \cdot V_{out} = A\ V_{in}.$$

$$\boxed{A_f = \frac{V_{out}}{V_{in}} = \frac{A}{1+\beta A.}}$$

Properties of Negative Feedback Amplifier

- **Desensitize the gain**: It brings stability to amplifier by making gain less sensitive to all kind of variations.

- **Reduce nonlinear distortion**

In negative feedback amplifier, the negative feedback makes the output proportional to the input, i.e reduces non-linear distortion.

- **Reduce the effect of Noise.**

The another property of Negative feedback amplifier are minimizes the contribution by unwanted electrical signals. These unwanted signals are called noise, these may be generated by circuit components or by extraneous interference.

- **Control the input & output impedances**

Negative feedback amplifiers are capable of modifying or controlling [i.e increase or decrease] the input and output impedances. This is done by choosing appropriate feedback topology.

- **Extend the bandwidth of the amplifier**

By incorporating negative feedback, the bandwidth can be increased.

Advantages of Negative feedback

In negative feedback amplifier, the gain of the amplifier reduces, however it is still used in almost every amplifier due to its various advantages.

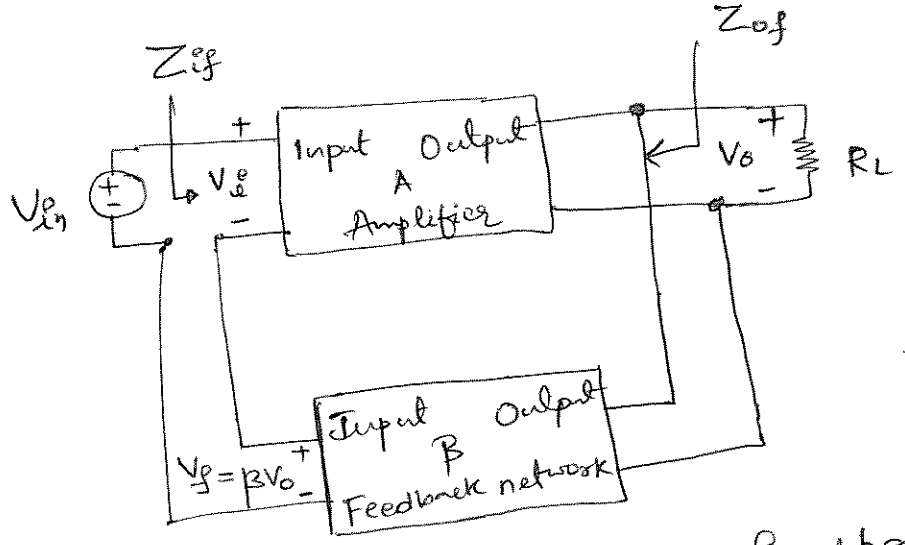
- Gain stability
- Significant extension of Bandwidth
- very less distortions
- Decreased output resistance
- Stable operating point
- Reduces noise and other interference in amplifier

Types of feedback

There are four types of feedback

1) Voltage series
2) Voltage shunt
3) Current series
4) Current shunt

The voltage series feedback circuit is shown in figure ③. It is also known as series - parallel feedback circuit. Here also the feedback is negative.



where $\beta = \frac{V_f}{V_o}$

Figure (3). Voltage-series feedback

From Figure (3). The $V_i = V_{in} - V_f$

$$V_i = V_{in} - \beta V_o$$

The gain of the amplifier is given by $A = \frac{V_o}{V_i}$

$$V_o = A V_i = A V_{in} - A\beta V_o \quad \longrightarrow (1)$$

The gain with feedback is given by

$$A_F = \frac{V_o}{V_{in}} \Rightarrow$$

From (1) $\quad V_o + A\beta V_o = A V_{in}$

$$V_o(1 + A\beta) = A V_{in}$$

$$A_F = \boxed{\frac{V_o}{V_{in}} = \frac{A}{1 + \beta A}}$$

This general gain with feedback applies to all types of feedback circuits.

The amplifier gain reduces by a factor of $(1 + \beta A)$.

Note:- gain stability is important feature of series v/g negative feedback amplifiers.

A negative feedback amplifier has an open loop gain of 400 and a feedback factor of 0.1. If the open loop gain changes by 20% due to temperature, find the percentage change in closed loop gain.

Given Data:- $A = 400$ & $\beta = 0.1$

closed loop gain.

$$A_f = \frac{A}{1+\beta A} = \frac{400}{1+(400\times 0.1)}$$

$$= 9.75.$$

when $A = 320$, i.e. open loop gain varied by $400 \times \left(\frac{20}{100}\right) = 80$.

$20\% = (400-80) = 320$

$$A_F = \frac{320}{1+(0.1*320)} = 9.7.$$

If 20% variation in open loop gain then.

$$A = (400+80) = 480.$$

$$A_F = \frac{480}{1+[0.1\times 480]} = 9.8$$

It is seen that while the open loop amplifier gain varies by ± 20%, the amplifier gain with feedback varied by only ± 0.5%.

An improvement of $\frac{20}{0.5} = 40$ times observed.

(2) The overall gain of a multistage amplifier is 140. when negative voltage feedback is applied, the gain is reduced to 17.5. Find the fraction of the output that is fedback to the input.

given Data:

$$A = 140, \quad A_F = 17.5$$

let β be the feedback fraction.

voltage gain with negative feedback is given by

$$A_F = \frac{A}{1+\beta A}$$

$$17.5 = \frac{140}{1+\beta(140)}$$

$$17.5(1+\beta*140) = 140.$$

$$\beta = \frac{140-17.5}{17.5*140} = 0.05. = \frac{1}{20}$$

(3). With a negative voltage feedback, an amplifier gives an output of 10V with an input of 0.5V. when feedback is removed, it requires 0.25 V input for the same output. Calculate (i). gain without feedback (ii) feedback fraction β.

(i) gain without feedback $= A = \frac{V_o}{V_i} = \frac{10}{0.25}$

$= 40.$

(ii) gain with feedback $= A_F = \frac{V_o}{V_{in}} = \frac{10}{0.5}$

$= 20.$

(4) When negative voltage feedback is applied to an amplifier of gain 100, the overall gain falls to 50.

(i) Calculate the fraction of the output voltage feedback

(ii) If this fraction is maintained, calculate the value of the amplifier gain required if the overall stage gain is to be 75.

Given data:-

(i) gain without feedback = 100

gain with feedback = 50.

Let β be the fraction of the output voltage feedback.

$$A_F = \frac{A}{1+\beta A}$$

$$50 = \frac{100}{1+\beta \times 100} \Rightarrow 50 + 5000\beta = 100$$

$$\beta = \frac{100-50}{5000} = \underline{\underline{0.01}}.$$

(ii). $A_F = 75$, $\beta = 0.01$, $A = ?$

$$A_F = \frac{A}{1+\beta A}$$

$$75 = \frac{A}{1+0.01A}$$

$$75 + 0.75A = A.$$

$$A = \frac{75}{1-0.75} = \underline{\underline{300}}.$$

(5). The voltage gain of an amplifier without feedback is 3000. Calculate the voltage gain of the amplifier if negative voltage feedback is introduced in the circuit. given that feed back fraction $\beta = 0.01$.

given data:-

$$A = 3000, \quad \beta = 0.01$$

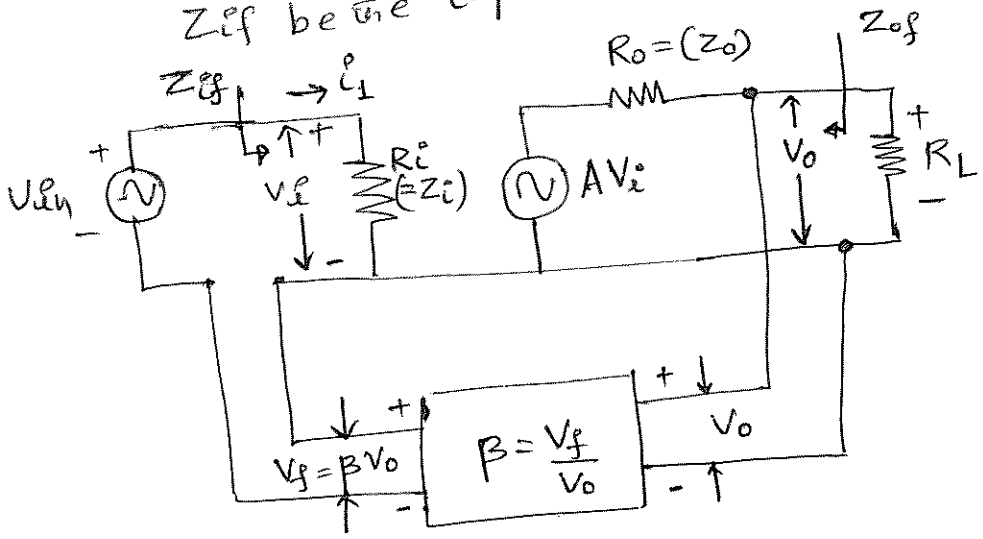
∴ Voltage gain with negative feed back is

$$A_F = \frac{A}{1+\beta A} = \frac{3000}{1+3000*0.01} = \frac{3000}{31} = 97.$$

Input Impedance of Negative feedback amplifier

Let Z_i be the input impedance without feedback

Z_{if} be the input impedance with feedback.



Voltage series feedback.

Voltage gain without feedback $A = \frac{V_o}{V_i}$

feedback fraction (factor) $= \beta = \frac{V_f}{V_o}$.

Voltage gain with feedback

$$A_F = \frac{V_o}{V_{in}} = \frac{A}{1+\beta A}$$

In voltage series feedback circuit, the input current $I_i = \frac{V_i}{Z_i}$, where V_i = Input voltage.

But $V_i = V_{in} - V_f$ where V_f = feedback voltage

$$I_i = \frac{V_{in} - V_f}{Z_i} = \frac{V_{in} - \beta V_o}{Z_i}$$

But $V_o = AV_i$ where A – open loop voltage gain.

$$I_i = \frac{V_{in} - \beta A V_i}{Z_i}$$

$$I_i Z_i = V_{in} - \beta A V_i$$

$$V_{in} = I_i Z_i + A\beta V_i \qquad \text{substitute } I_i Z_i = V_i.$$

$$V_{in} = V_i + A\beta V_i$$

$$V_{in} = V_i(1 + A\beta).$$

$$V_{in} = I_i Z_i (1 + A\beta).$$

$$\frac{V_{in}}{I_i} = Z_i (1 + A\beta).$$

But $\frac{V_{in}}{I_i} = Z_{if} = Z_i (1 + A\beta)$.

The input impedance with feedback.

$$\therefore \boxed{Z_{if} = Z_i (1 + A\beta).}$$

Hence the input impedance with feedback is $(1 + A\beta)$ times the input impedance without feedback. Thus the effect of negative feedback is to increase the input impedance of a series-voltage negative feedback amplifier by a factor $(1 + A\beta)$.

Output impedance of Negative feedback amplifier.

Let Z_o output impedance without feedback.
& Z_{of} → be the output impedance with feedback

Let the source signal voltage V_{in} be set equal to zero, & let a voltage V be applied to the output port. Let the resulting current in the output circuit be i.

we have $AV_i + iZ_o = V$ ⟶ (*). putting $Z_o = R_o$.

in general.

$V_i = V_{in} - V_f$. where V_f = feedback voltage

when $V_{in} = 0$.

$$V_i = -V_f. \longrightarrow (1)$$

subeq (1) in (*)

$$\therefore V = -V_f A + iZ_o.$$

or.

$$V = iZ_o - A(\beta V).$$

i.e.

$$V + A\beta V = iZ_o$$

$$V(1 + A\beta) = iZ_o$$

or

$$\frac{V}{i} = \frac{Z_o}{(1 + A\beta)}$$

But $\frac{V}{i} = Z_{of}$ = the output impedance with feedback

$$Z_{of} = \frac{Z_o}{(1 + A\beta)}$$

Hence Due to negative feedback, the output impedance gets reduced by the factor $(1 + A\beta)$.

Voltage Series feedback amplifier has input impedance with feedback,

$$Z_{if} = Z_i(1+\beta A), \text{ increases.}$$

Output impedance with feedback,

$$Z_{of} = \frac{Z_o}{(1+\beta A)} \text{ . decreases.}$$

we know that closed loop gain. [gain with feedback]

$$A_f = \frac{A}{1+\beta A}$$

If $\beta A >> 1$ then closed loop gain.

$$A_f = \frac{A}{\beta A} = \frac{1}{\beta}.$$

This means that feedback gain independent of amplifier gain. Thus all the distortions do not appear in A_f.
This also happens to a noise signal, which gets attenuated by feedback.

Any variations in magnitude of A does not appear in A_f, which means A_F has high gain stability.

Gain and Bandwidth of feedback amplifier

The negative feedback reduces the amplifier gain. Therefore, as per the principle the amplifier increases its bandwidth. In RC-Coupled amplifier, the gain reduces at low frequency and high frequency ends. So βA_0 is no longer much more than unity.

As a result, the percent reduction in gain is less at the two feedback ends compared to the mid-band.

The reduction in gain & increase in bandwidth of amplifiers are shown in figure (4).

As $f_1 \ll f_2$ and $f_{1f} \ll f_{2f}$.

$$BW = (f_2 - f_1) \simeq f_2$$

$$BW = (f_{2f} - f_{1f}) \simeq f_{2f}.$$

The constant product of gain bandwidth is

$$A_0 (f_2 - f_1) = A_{0f} (f_{2f} - f_{1f})$$

$$A_0 f_2 = A_{0f} f_{2f}$$ for $f_1 \ll f_2$ & $f_{1f} \ll f_{2f}$.

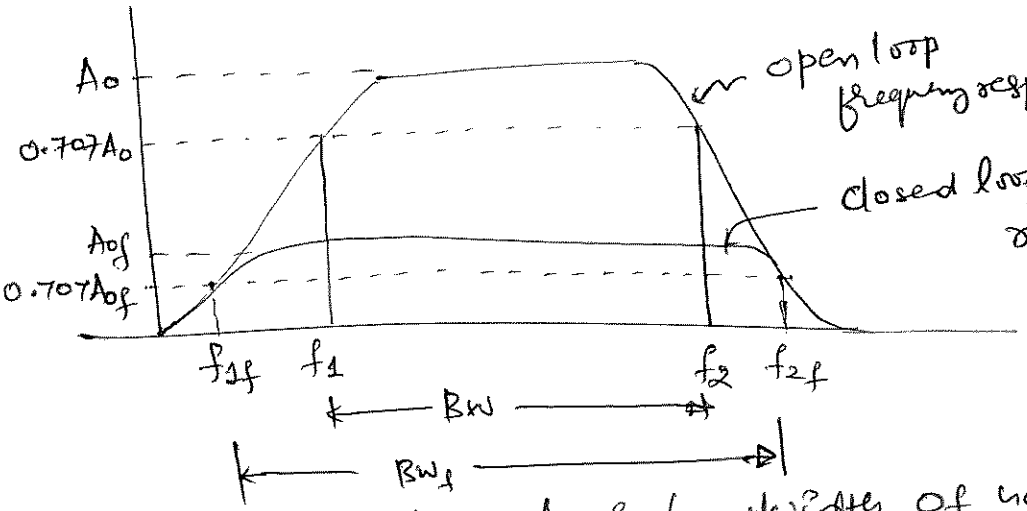


Fig (4):- effect on A_0 & bandwidth of negative feedback

Bandwidth of an amplifier without feedback is equal to seperation between the 3dB frequency f_1 and f_2.

f_1, f_2 are lower & upper 3dB frequency.

The gain Bandwidth product is.

$$= A * BW.$$

$$= A * (f_2 - f_1)$$

When the negative feedback is applied, the amplifier gain is reduced. Since the gain Bandwidth product has to remain the same in both the cases, it is obvious that the Bandwidth must increase to Compensate for the decrease in the gain.

In negative amplifier, the lower & upper 3dB frequencies of an amplifier become.

$$f_{1f} = \frac{f_1}{(1+\beta A)} \quad \& \quad f_{2f} = f_2(1+\beta A).$$

f_{1f} → has decreased and f_{2f} → has increased, these by giving a wider Repeation or bandwidth.

$$A\,BW = A_f\,BW_f.$$

In negative feedback amplifier, gain is reduced & Band width is increased.

Gain Stability with feedback

The overall gain with negative feedback is

$$A_F = \frac{A}{1+\beta A}.$$

Differentiation of the above equation leads to

$$\frac{dA_f}{A_f} = \frac{1}{(1+\beta A)} \cdot \frac{dA}{A}$$

$$\frac{dA_f}{A_f} = \frac{1}{\beta A} \frac{\partial A}{A} \cdot \text{ for } \beta A >> 1$$

The above relation shows that the relative change (dA/A) in the basic amplifier gain is reduced by the factor βA & the relative change (dA_f/A_f) in the overall gain of the feedback amplifier.

An amplifier has a high frequency response described as

$$A = \frac{A_0}{1 + (j\omega/\omega_2)} \quad \text{where } A_0 = 1000,\ \omega_2 = 10^4 \text{ rad/s}$$

Find the feedback (negative) factor β, which will raise the upper corner frequency (ω_2) to 10^5 rad/s. What is the corresponding overall gain of the amplifier? Find the gain-bandwidth product in each case.

Soln: For amplifier, we divide A_0 by $(1+\beta A_0)$ & we multiply frequency ω_2 by $(1+\beta A_0)$. Hence gain with feedback is given by

$$A_f = \frac{A_0/(1+\beta A_0)}{1 + \{j\omega/[\omega_2(1+\beta A_0)]\}} = \frac{A_0(\text{new})}{1 + [j\omega/\omega_2(\text{new})]}$$

where $A(\text{new}) = \frac{A_0}{1+\beta A_0}$

$$\omega_2(\text{new}) = \omega_2(1+\beta A_0)$$

Substituting values, $10^5 = 10^4(1+\beta \times 1000)$

$$\beta = 0.009$$

$$A_{\text{new}} = \frac{A_0}{1+\beta A_0} = 100$$

Gain bandwidth products, without & with feedback are

$$\omega_2 A_0 = 10^4 \times 10^3 = 10^7$$

$$\omega_2(\text{new})\, A(\text{new}) = 10^5 \times 100 = 10^7$$

Here Gain-bandwidth product is maintained constant.

Oscillators.

Introduction :- The process of raising the strength of a weak signal without any change in its shape is known as faithful amplification.
The dc signal applied to the amplifier is amplified in accordance with the instantaneous value of input ac signal.
But an oscillator is an energy Converter. It receives dc energy and changes it into ac energy of desired frequency.
The frequency of oscillations depends upon the constants of the device. The Composite electric circuit associated with an active device when used to produce an alternating current is called an oscillator circuit.
Oscillators can be both sinusoidal and non-sinusoidal.
Non-sinusoidal oscillators are also called Relaxation oscillators which are rich in harmonics.

Classification of oscillator

Based on the nature of output waveform.
(a) Sinusoidal
(b) Non-sinusoidal / Relaxation oscillators.

Based on the wether feedback is used or not
(a) Feedback type
(b) Non-feedback type Eg. UJT Relaxation type oscillator.

Based on the range of operating frequency.
(a) Low frequency or Audio frequency (20Hz to 200KHz)
(b) Heigh frequency or Radio frequency (200KHz to few GigaHz)
(c) UHF oscillators.
(d) Microwave oscillators.

According to the circuit employed.

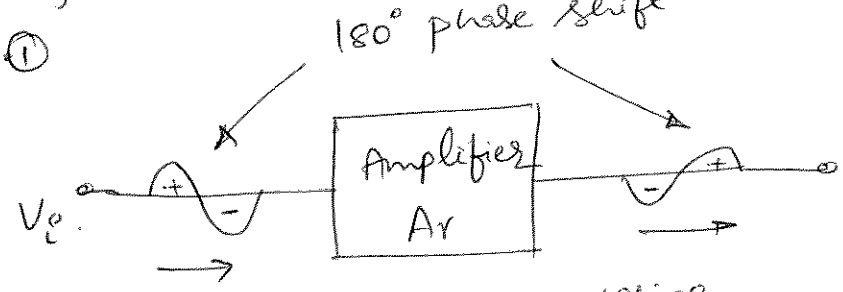
(a) LC oscillators.

(b) RC oscillators.

Barkhausen criterion.

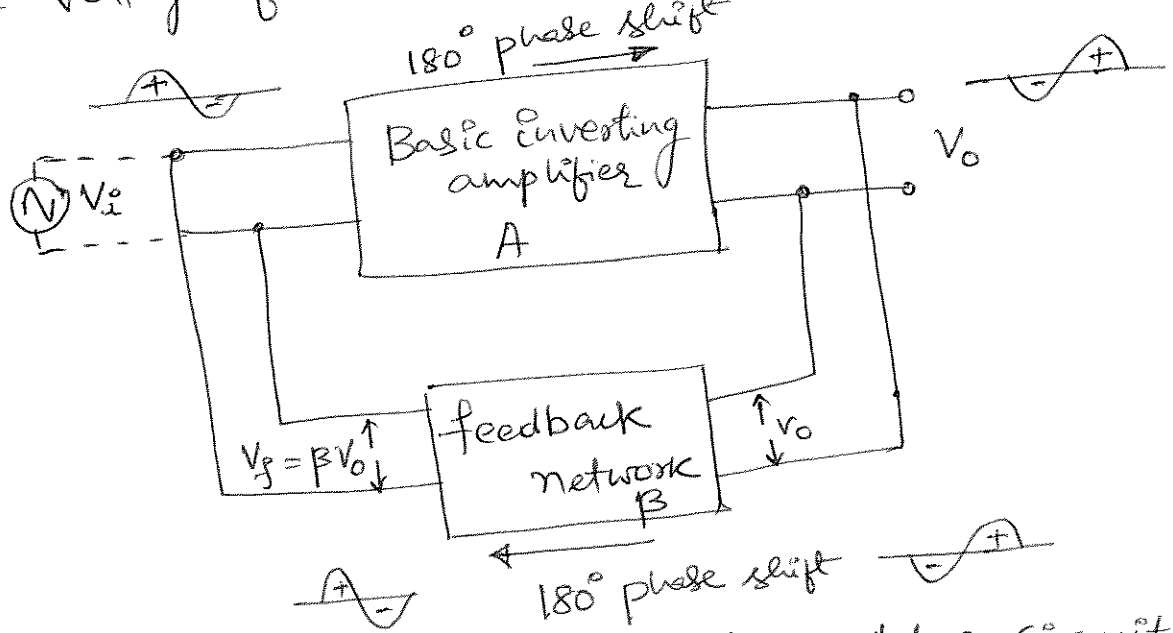
Let us take a basic amplifier having an open-loop gain, A. The feedback network has feedback factor β is less than unity.

Here the amplifier is inverting, it produces a phase shift of 180° between input and output as shown in figure (1)



Fig(1). Inverting amplifier.

But the feedback must be positive, i.e., the voltage derived from the output using feedback network must be in phase with V_i. Thus the feedback network must introduce a phase shift of 180° while feeding back the voltage from output to input as shown in figure (2).



Fig(2). Block diagram of oscillator circuit.

Consider a voltage V_i applied at the input of the amplifier.

$$V_o = A\, V_i \quad \rightarrow (1)$$

The feedback factor β determines the feedback given to the input.

$$V_f = \beta V_o \quad \rightarrow (2)$$

Substitute (2) in (1) we get

$$V_f = A\beta V_i \quad \rightarrow (3)$$

For the oscillator, it is necessary that the feedback should drive the amplifier and hence V_f must act as V_i.

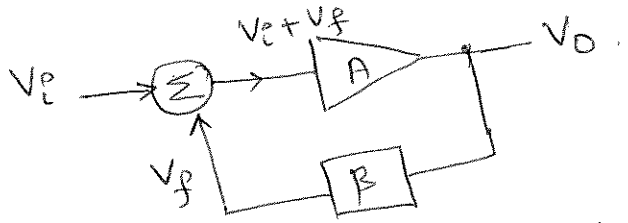


Fig (3) : oscillator.

From Fig (3)
Here we can write

$$V_o = A\cdot(V_i - V_f)$$

$$V_o = A\cdot V_i - A\beta V_o$$

$$V_o + A\beta V_o = A V_i$$

$$\frac{V_o}{V_i} = \frac{A}{(1+A\beta)}$$

Here for gain to be 'A' the

we can say that V_f is sufficient to act as V_i when

$$|A\beta| = 1$$

Also, the phase of V_f is the same as the phase of V_i, i.e., the feedback network should introduce 180° phase shift in addition to the 180° phase shift introduced by the inverting amplifier. This ensures positive feedback. Hence the total phase shift around the loop is 360°.

Under such circumstances, V_f drives the circuit and with out any external input, this circuit works as an oscillator.

The two conditions discussed above, necessary for the circuit to function as an oscillator are called the Barkhausen Criterion for oscillation.

The Barkhausen criterion states that:

1. The total phase shift around a loop, as the signal proceeds from the input through the amplifier, feedback network, back to the input again, completing a loop is precisely 0° or 360°.

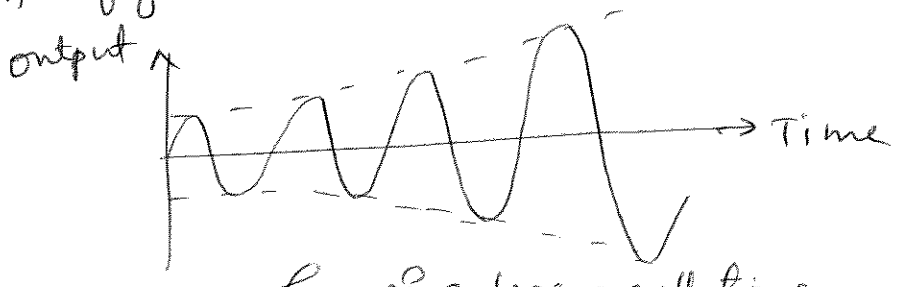
2. The magnitude of the product of the open-loop gain of the amplifier (A) and the magnitude of the feedback factor β is unity i.e. $|A\beta| = 1$.

In reality, no input signal is needed to start the oscillations. In practice, $A\beta$ is made greater than 1 to start the oscillations and then the circuit adjusts itself to get $A\beta = 1$, finally leading to self-sustained oscillations.

Effect of the magnitude of the product $A\beta$ on the nature of the oscillations.

① $|A\beta| > 1$.

When the total phase shift around a loop is 0° or 360° and $|A\beta| > 1$, then the output oscillates but the oscillations are of the growing type. The amplitude of the oscillations keeps on increasing as shown in figure.



Growing type oscillations.

So that to start the oscillations without input $|A\beta|$ is kept higher than unity and the circuit adjusts itself to get $|A\beta| = 1$. to result in sustained oscillations.

problems..

(2) $|A\beta| = 1$

As stated by Barkhausen Criterion, when the total phase around a loop is 0° or 360° ensuring positive feedback and $|A\beta| = 1$, then the oscillations are with constant frequency and amplitude called sustained oscillations. Such oscillations are shown in figure below.

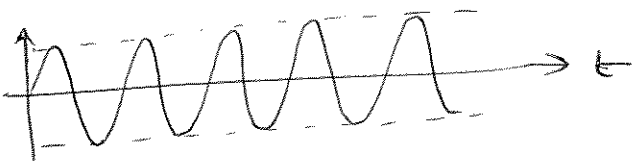


Figure. Sustained oscillations.

(3) $|A\beta| < 1$.

When the total phase shift around a loop is 0° or 360° but $|A\beta| < 1$, then the oscillations are of the decaying type, i.e., the amplitude of such oscillations decreases exponentially till they finally die out. In such cases the circuit works as an amplifier without oscillations. The decaying oscillations are shown in figure.

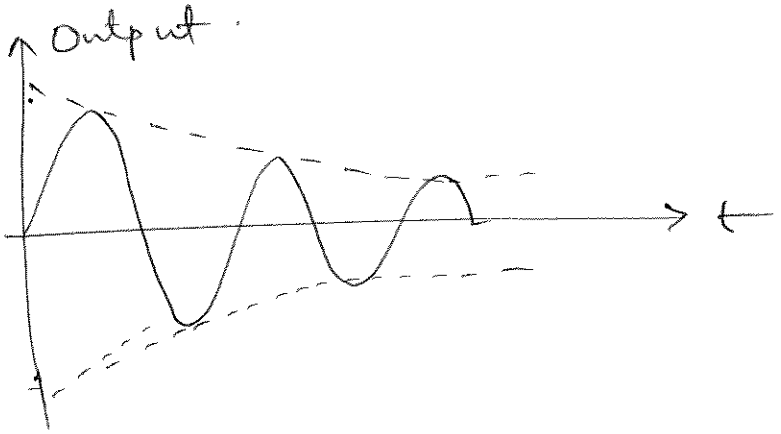


Figure. Exponentially decaying oscillations.

Oscillators.

Rc phase shift oscillator

Figure (2) shows the Rc phase shift oscillator, Here the phase shift is achieved by RC-network. Because of loading effect, three RC-stages are needed.
It is used to produce sustained well shaped sine wave oscillations.

Applⁿ :- Local oscillator for synchronous receivers.
Musical instruments.

The main part of an RC phase shift oscillator is an op-amp inverting amplifier with its output fed back into its input using a regenerative feedback RC filter network.
The RC phase shifting filter network is shown in figure (1).

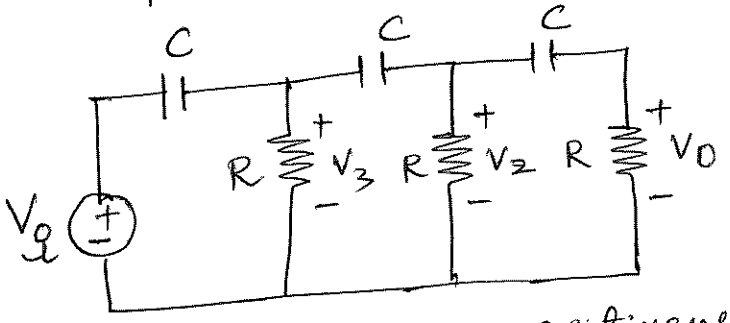


Fig (1). RC phase shifting network.

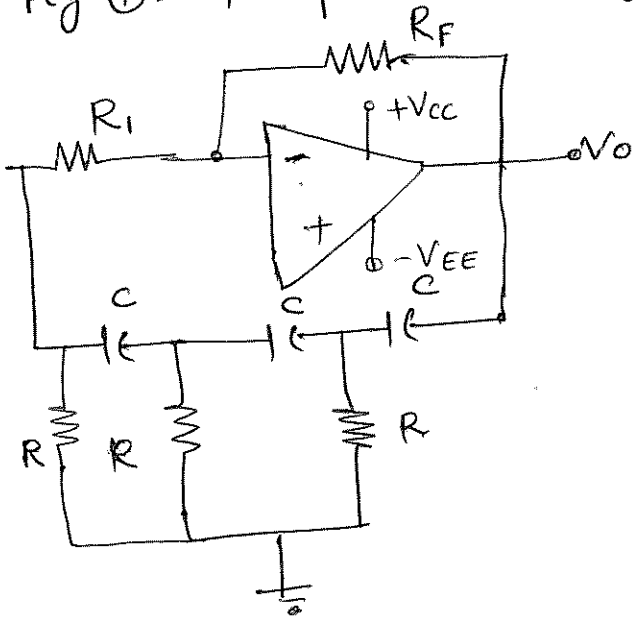


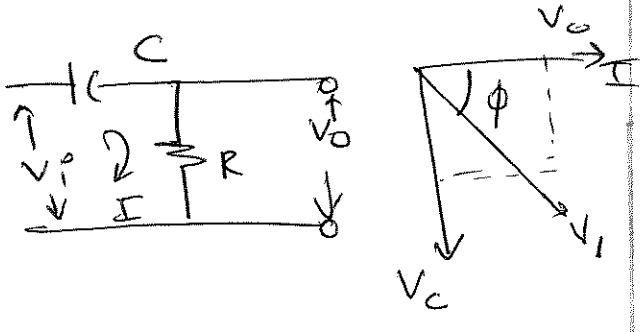
Fig. (2). phase shift Oscillator.

For the RC phase shifting network. we can write feedback factor

$$\beta = \frac{\vec{V_o}(j\omega)}{\vec{V_i}(j\omega)}.$$

For Example by Considering on RC network we derive the frequency of operation. Let a current I flow through both R and C. V_o is in phase I, whereas the voltage across the capacitor ; C lags behind by 90°.

The vector sum of V_c and V_o is V_1.



$$V_o = IR \quad V_c = IX_c$$

$$\& \tan\phi = \frac{V_c}{V_o}$$

$$\tan\phi = \frac{IX_c}{IR} = \frac{X_c}{R}$$

$$X_c = \left(\frac{1}{2\pi fC}\right), \quad \tan\phi = \frac{1}{2\pi fCR}$$

$$f = \frac{1}{2\pi RC\tan\phi}.$$

as there are three RC sections in the phase shift network, each one Contributes a phase shift $\phi = 60°$.

$$\therefore \tan\phi = \tan 60° = \sqrt{3}$$

$$f = \frac{1}{2\pi RC\sqrt{2\times 3}}$$

$$f = \frac{1}{2\pi RC\sqrt{6}}.$$

$$\boxed{\omega = \frac{1}{RC\sqrt{6}}} \qquad \boxed{\omega = 2\pi f}$$

& $\beta\omega = -\frac{1}{29}$; 180° phase shift

For oscillation to occur. $|\beta| > \frac{1}{29}$.

The feed back resistor required to maintain sustained oscillations is

$$R_f = 29 \cdot R \qquad \text{when } R_1 = R_2 = R_3 = R$$

$$C_1 = C_2 = C_3 = R.$$

we know that gain of opamp is given by. [Inverting op-amp is used]

$$A = -\frac{R_f}{R}$$

$$A = -\frac{29R}{R}.$$

$$\boxed{A = -29} \qquad |A| = 29.$$

$$A\bar{\beta} = \left(-\frac{1}{29}\right)\left(-\frac{R_f}{R}\right).$$

$$A\bar{\beta} = \frac{R_f}{29R} > 1.$$

hence $\boxed{R_f = 29R}$

Problem:- For a RC phase shift oscillator, the phase-shift network uses resistance $R = 2.2\,K\Omega$ & a capacitor $C = 0.47\,\mu F$. Find the frequency of oscillations.

The frequency of oscillation is given by

$$f = \frac{1}{2\pi RC\sqrt{6}} \qquad R = 2.2\,K\Omega$$

$$C = 0.47\,\mu F$$

$$\therefore f = \frac{1}{2\pi \times \sqrt{6} \times 2.2 \times 10^{3} \times 0.47 \times 10^{-6}}$$

$$= 63\,Hz.$$

working of RC phase shift oscillator

A RC phase-shift oscillator circuit produces a sine wave output. It consists of op-amp as amplifier element. This inverting amplifier output is fed back to its input through a phase-shift network. Consisting of capacitor and resistor in a ladder network.

The feedback network shifts the phase of the amplifier output by 180° at the oscillation frequency to give positive feedback.

Appl^n: audio oscillator.

(2). A three section ladder type phase shift oscillator has 3 similar phase-advancing sections, each containing a 100KΩ resistor and 0.0005 μF capacitor. Calculate the frequency of oscillations.

Solution:- $R = 100K\Omega$ & $C = 0.0005\ \mu F$.

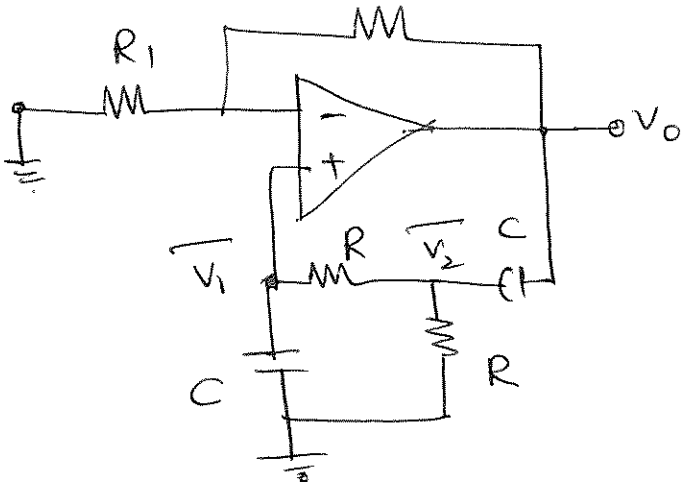
$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$= \frac{1}{2\pi * 100\times10^3 * 0.0005\times10^{-6}\sqrt{6}}$$

$$= 1300Hz$$

$$\boxed{f = 1.3\ KHz}$$

(3) For the feedback op-amp circuit of figure determine the condition for oscillation and the oscillation frequency



At node 2,

$$j\omega C(\bar{V}_2 - \bar{V}_0) + \frac{\bar{V}_2}{R} + \frac{\bar{V}_2 - \bar{V}_1}{R} = 0 \quad \longrightarrow (1)$$

At node 1,

$$\frac{\bar{V}_1 - \bar{V}_2}{R} + j\omega C\bar{V}_1 = 0$$

$$(V_1 - V_2) + j\omega RC V_1 = 0$$

$$V_1 + j\omega RC)V_1 = V_2$$

$$V_2 = (1 + j\omega RC)V_1 \quad \longrightarrow (2)$$

Substitute eq^n (2) in (1)

$$\Rightarrow j\omega C\left[\left[(1 + j\omega RC)V_1 - \bar{V}_0\right)\right] + \frac{(1+j\omega RC)V_1}{R} + \left[\frac{(1+j\omega RC)*V_1 - V_1}{R}\right] =$$

$$\Rightarrow j\omega CV_1 + \omega^2 RC^2 V_1 - j\omega_c V_0 + \frac{1}{R}\cdot V_1 + \frac{j\omega RCV_1}{R} + \frac{j\omega RCV_1}{R} = 0$$

$$j\omega C V_1 + \omega^2 RC^2 V_1 + \frac{1}{R} V_1 + 2\frac{j\omega RC V_1}{R} = j\omega_c V_0$$

$$\beta = \frac{V_1}{V_0} = \frac{1}{3 + j(\omega RC - \frac{1}{\omega RC})}$$

For β to be real, the j-term should be zero.

This happen when.

$$\omega = \frac{1}{RC} \Rightarrow f = \frac{1}{2\pi RC}$$

then $\beta = \frac{1}{3}$ possitive feedback

Foowrard gain $A = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}$

For oscillations to occur.

$$A\beta = \frac{1}{3}\left(1 + \frac{R_2}{R_1}\right) > 1$$

$$\boxed{\frac{R_2}{R_1} > 2}$$

(4) Estimate the values of R and C for an output frequency of 1 KHz in a RC phase shift oscillator.

$$\text{frequency of oscillation } f = \frac{1}{2\pi RC\sqrt{6}}$$

let $R = 100\,K\Omega$, & given $f = 1\,KHz$.

$$C = \frac{1}{2\pi * 100\times10^3 * 1*10^3 * \sqrt{6}}$$

$$\boxed{C = 0.00065\,\mu F}$$

Here $R = 100\,K\Omega$, $C = 0.0006\,5\,\mu F$.

Wien Bridge Oscillator

It is an audio frequency sine wave oscillator of high stability and simplicity.

It is a two stage RC amplifier circuit connected in wheat stone's bridge with an amplifier stage.

Wein Bridge oscillator uses non-inverting amplifier & hence does not provide any phase shift and no need of phase shift through the feedback network.

wein bridge oscillator is shown in figure. It consists of op-amp and RC bridge circuit, with the oscillator frequency set by the R and C components. Two RC combination using R_1, R_2, C_1 and C_2 and R_3 and R_4 form the bridge. The op-amp output is connected as the bridge input at points a and c.

The bridge circuit output at points b and d provide negative and positive inputs to the op-amp.

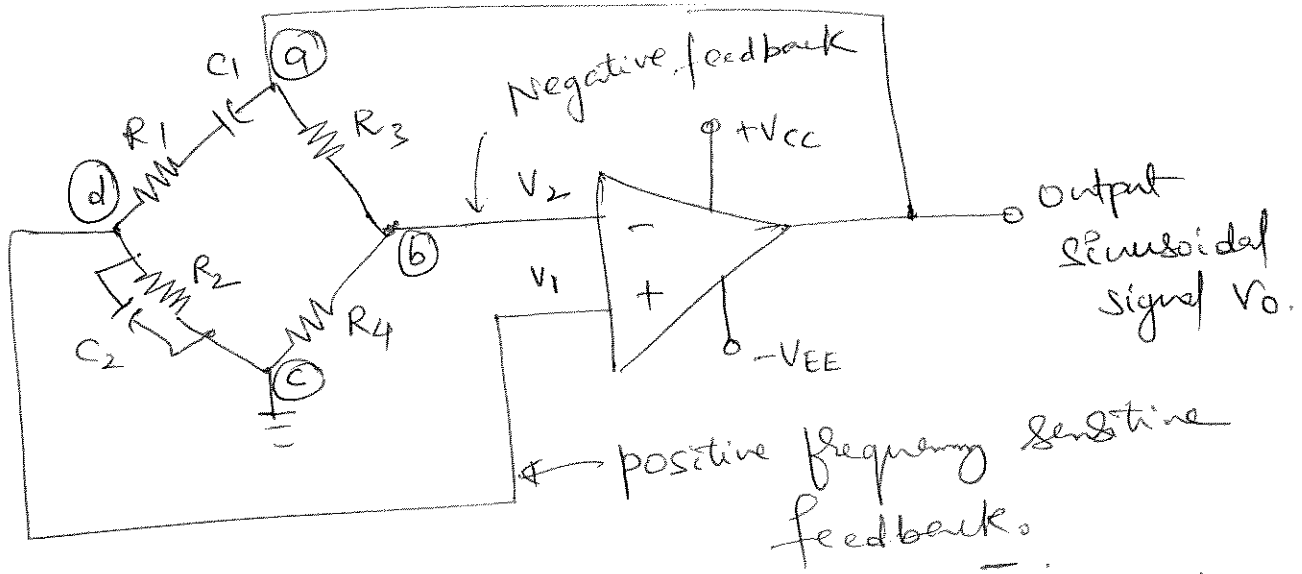
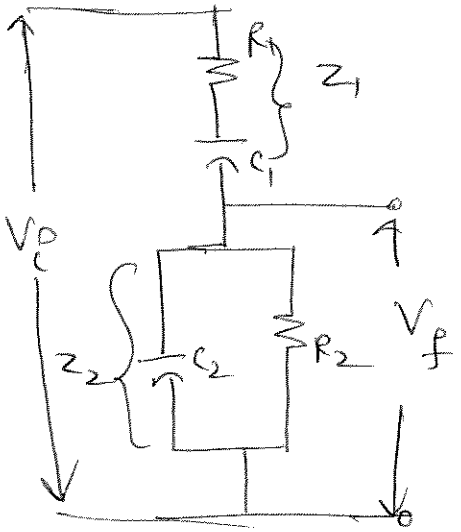


Figure: wein Bridge oscillator using an op-amp amplifier

The two RC network is responsible for determining the frequency of oscillation.

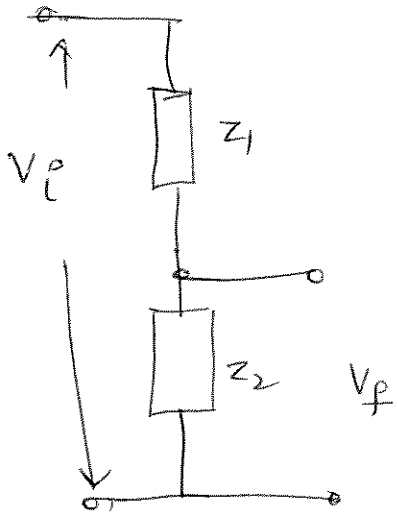
The two RC network arms i,e Series R_1C_1 and parallel R_2C_2 are called the frequency sensitive arms.

To understand the gain of the feedback network let's rearrange the circuit.



This Configuration is also called lead-lag network because it acts like a lead at very low frequency and lag network at very high frequencies.

To calculate the gain of the network Consider a series RC as Z_1 and parallel RC as Z_2.



Equivalent circuit.

where

$$Z_1 = R_1 + \frac{1}{j\omega C_1} \qquad Z_2 = R_2 \parallel \frac{1}{j\omega C_2}$$

$$= \frac{j\omega R_1 C_1 + 1}{j\omega C_1} \qquad = \frac{R_2}{1 + j\omega R_2 C_2}.$$

The simplified circuit is shown aside which is a voltage divider fig. circuit here

$$\beta = \frac{V_f}{V_i} = \frac{Z_2}{Z_1 + Z_2}$$ this is feedback gain at non-inverting terminal.

$$= \frac{R_2 \,/\, (1 + j\omega R_2 C_2)}{\frac{R_2}{(1 + j\omega R_2 C_2)} + \frac{(1 + j\omega R_1 C_1)}{j\omega C_1}}$$

$$= \frac{\frac{R_2}{(j\omega C_2 R_2 + 1)}}{\frac{R_2 j\omega C_1 + (1 + j\omega C_1 R_1)(1 + j\omega R_2 C_2)}{j\omega C_1 (1 + j\omega R_2 C_2)}}$$

$$= \frac{j\omega C_1 R_2}{j\omega C_1 R_2 + 1 + j\omega C_1 R_1 + j\omega R_2 C_2 + j^2 \omega^2 C_1 R_1 C_2 R_2}$$

$$= \frac{j\omega C_1 R_2}{(1 - \omega^2 C_1 R_1 C_2 R_2) + j\omega (R_1 C_1 + R_2 C_2 + R_2 C_1)} \qquad j^2 = -1$$

Rationalising the expression we get

$$\beta = \frac{V_o}{V_i} = \frac{j\omega C_1 R_2 \left[(1 - \omega^2 C_1 R_1 C_2 R_2) - j\omega (R_1 C_1 + R_2 C_2 + R_2 C_1)\right]}{(1 - \omega^2 C_1 R_1 C_2 R_2)^2 + \omega^2 (R_1 C_1 + R_2 C_2 + R_2 C_1)^2}$$

$$= \frac{\omega^2 C_1 R_2 (R_1 C_1 + R_2 C_2 + R_2 C_1) + j\omega R_2 C_1 (1 - \omega^2 C_1 C_2 R_1 R_2)}{(1 - \omega^2 C_1 R_1 C_2 R_2)^2 + \omega^2 (R_1 C_1 + R_2 C_2 + R_2 C_1)^2}$$

To have a zero phase shift of the feedback network its imaginary part must be zero.

$$\therefore \omega R_2 C_1 (1 - \omega^2 C_1 C_2 R_1 R_2) = 0$$

$$1 - \omega^2 R_1 R_2 C_1 C_2 = 0$$

$$\omega^2 R_1 R_2 C_1 C_2 = 1$$

$$\omega^2 = \frac{1}{R_1 R_2 C_1 C_2} \Rightarrow \omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\omega = 2\pi f \Rightarrow f = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

Hence the frequency of the oscillator shows that the components i.e. R_1, R_2, C_1, C_2 of the frequency sensitive arms are the deciding factors for the frequency

let $R_1 = R_2 = C$, $C_1 = C_2 = C$.

$$f = \frac{1}{2\pi\sqrt{R^2C^2}} = \frac{1}{2\pi RC}$$

The gain of the feedback network becomes.

$$\beta = \frac{V_o}{V_i} = \frac{\omega^2 CR(3RC) + j\omega RC(1-\omega^2R^2C^2)}{(1-\omega^2R^2C^2)^2 + \omega^2(3RC)^2}$$

substitute $\omega = \frac{1}{RC}$

$$= \frac{\frac{3}{R^2C^2}(RC)^2 + j\frac{1}{RC} \times RC\left[1 - \frac{1}{R^2C^2} \times R^2C^2\right]}{\left[1 - \frac{1}{R^2C^2}R^2C^2\right]^2 + \frac{1}{R^2C^2} \times R^2C^2}$$

$$\beta = \frac{3}{9} = \frac{1}{3}.$$

The positive sign of β indicates that the phase shift by the feedback network is zero.

For sustained oscillations.

$$|A\beta| \geq 1$$

$$|A| \geq \frac{1}{|\beta|} = \frac{1}{\frac{1}{3}} = 3$$

$$|A| \geq 3.$$

Forward gain at inverting terminal

$$A = -\frac{V_o}{V_2} = -\left[1 + \frac{R_3}{R_4}\right]$$

For oscillations, Barkhausen criterion

$$A\beta \geq 1 \qquad \beta = \frac{1}{3}$$

$$\left(1 + \frac{R_3}{R_4}\right)\left(\frac{1}{3}\right) \geq 1$$

$$\frac{R_3}{R_4} \geq 3 - 1 \quad \text{i.e.} \geq 2$$

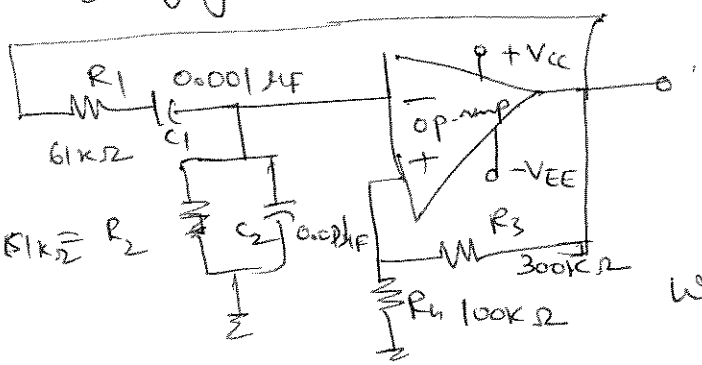
$$\boxed{R_3 = 2R_4}$$

Thus the ratio of R_3 & R_4 should be greater than or equal to 2 to provide sufficient loop gain for the circuit to oscillate at the frequency calculated as

$$f = \frac{1}{2\pi RC}.$$

Problems.

Calculate the resonant frequency of the wein bridge oscillator of figure.



Wein bridge oscillator circuit.

Soln:

$$f = \frac{1}{2\pi RC} = \frac{1}{2 * \pi * 61 * 10^3 * 0.01 \times 10^{-6}}$$

$$= 260.9\ Hz$$

(2) Design the RC elements of a wien bridge oscillator as in figure. for operation at $f = 10\,KHz$.

$$RC = \frac{1}{2\pi f} = \frac{1}{2 * \pi * 10 * 10^3}$$

choose

$R = 150\,K\Omega$ $\quad C = \dfrac{1}{6.28 * (10 * 10^3 * 150 * 10^3}$

$$C = 238.5\ F$$

we can use $R_3 = 300\,K\Omega$ & $R_4 = 100\,K\Omega$ to provide a ratio R_3/R_4, greater than 2 for oscillation to take place.

Clock and Timing Circuits.

Introduction :-

Heart of a computer is the clock which produces clock pulses with the precise cycle time. The clock pulses advance the various circuits of the computer one step at a time. The clock pulses are normally Rectangular; positive pulses followed by negative pulses as shown in fig ①.

The duty cycle could be other than 50% but the cycle time must be precise. All logic elements must complete their transition in one cycle.

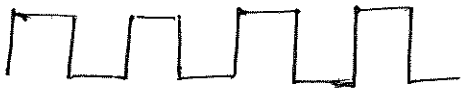


fig ①. Ideal clock pulses.

The clock pulses can be generated by IC-555 timer or by a crystal oscillator.

IC-555 Timer :-

It is an integrated circuit used in a variety of timer, pulse generation and oscillator applications. It is a highly stable device for generation of accurate time delays and oscillations.

The entire circuit is available in an 8-pin package as shown in fig ②. details are shown in fig ③.

① It consists of two op-amp comparator set at $2/3\ V_{cc}$ and $1/3\ V_{cc}$ respectively.

② A three resistor circuit, to obtain voltage $2/3\ V_{cc}$ and $1/3\ V_{cc}$ to set the comparators.

- The comparator's output sets or resets the FlipFlop (F/F) which feeds the output stage.

The FlipFlop operates as

R = 1, S = 0, Output = 0

R = 0, S = 1 Output = 1.

The FlipFlop also operates a transistor which when driven low, discharges a timing capacitor (external).

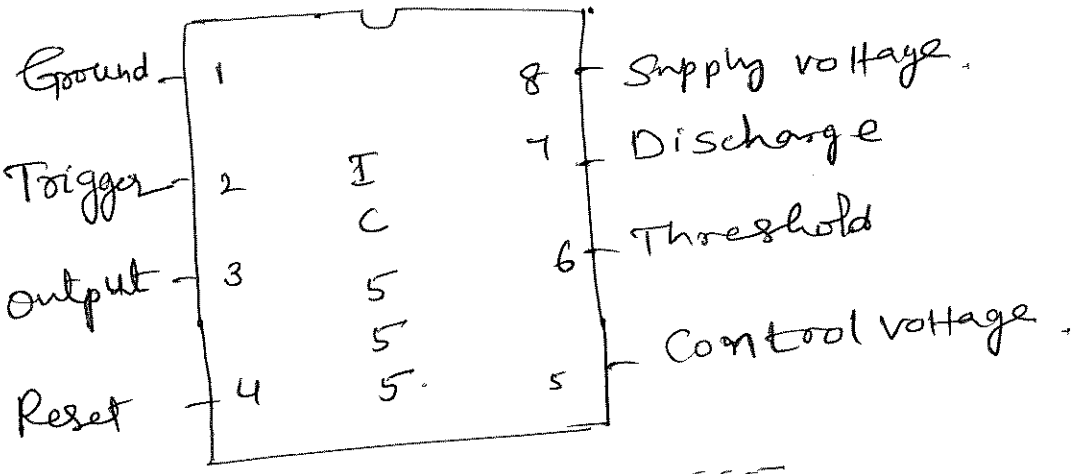
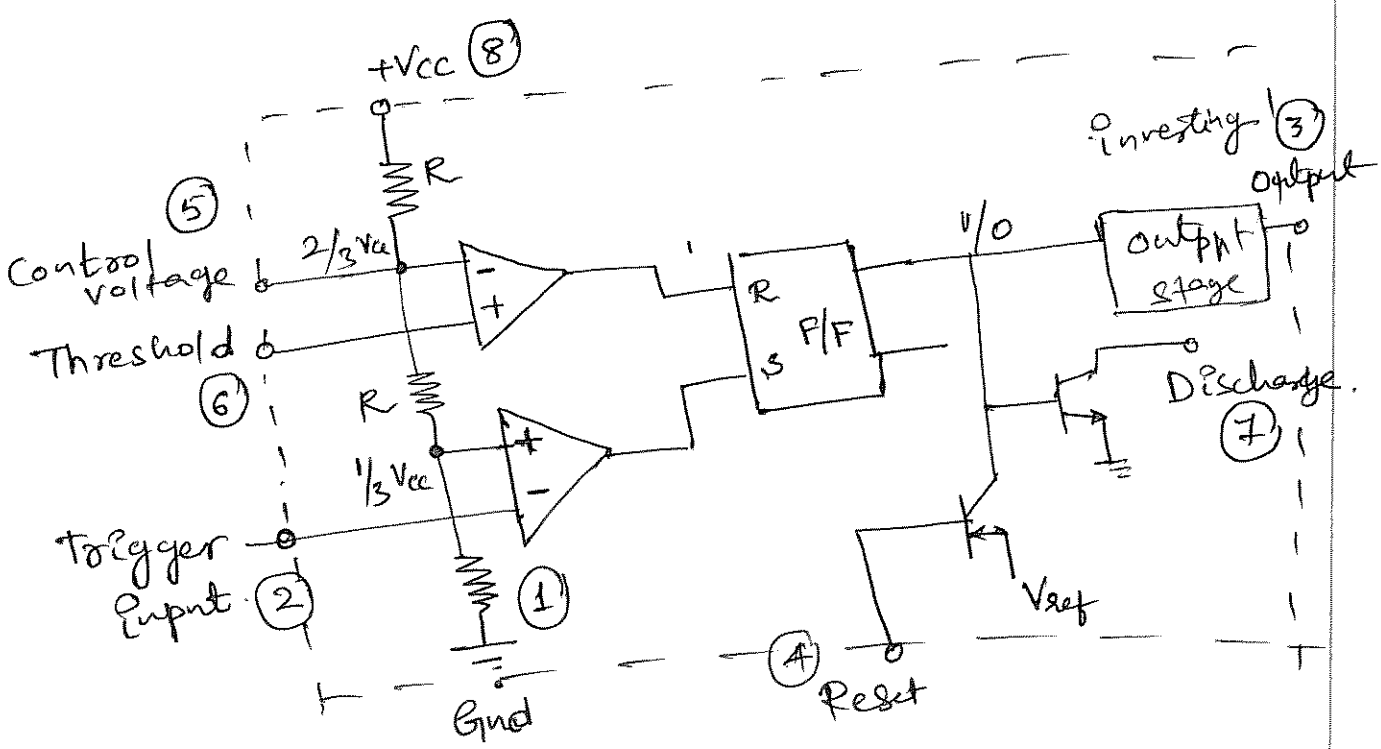


Fig ②. Pin details of IC 555.



Internal Details of IC 555 timer.

pin 1: Ground

It Connects the IC 555 timer to the negative (0V) Supply.

pin 2:- Trigger.

The negative input to Comparator 2. A negative pulse on this pin "Sets" the internal Flip-Flop when the voltage drops below 1/3Vcc causing the output to switch from a LOW to a HIGH state.

pin 3:- Output.

It can drive any Transistor Transistor logic [TTL] Circuit and is Capable of sourcing or sinking up to 200mA of current at an output voltage equal to approximately Vcc = 1.5V so Small Speakers, LED's or motor can be directly Connected to the output.

pin 4:- reset.

It is used to reset the internal FlipFlop Controlling the state of the output pin 3.

pin 5:- Control voltage.

It Controls the timing of the 555 by overriding 2/3Vcc Level of the voltage divider network.

We can vary RC Timing by applying voltage to this pin when not used Connected to ground through 10nF Capacitor to eliminate the noise.

pin 6:- Threshold.

The positive input to Comparator 1. This pin is used to reset the FlipFlop when the voltage applied to it exceeds 2/3 Vcc causing the output to switch from 'High' to 'Low' state. It Connats directly to RC Timing Circuits.

Pin 7 :- Discharge :-

It is directly connected to the Collector of an external NPN transistor which is used to 'discharge' the timing capacitor to ground when the output at pin 3 switches Low.

pin 8 : Supply +Vcc

This is the power supply pin for general purpose TTL 555 timer's is between 4.5V & 15V.

The three 5KΩ resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1.

Astable operation :—

A common application of the 555 timer is as astable multivibrator or clock circuit.

Fig 4. shows a stable circuit built using two external Resistors and a capacitor, which sets the timing interval of the output.

Astable multivibrator is also called free running or self triggering mode. It does not have any stable state, it ~~consists~~ of two quasi stable state (High & Low)

No external triggering is used here, it automatically interchange its two states on a particular interval, hence generates a rectangular waveform.

Astable mode works as a oscillator circuit, in which output oscillate at a particular frequency & generate pulses in rectangular waveform.

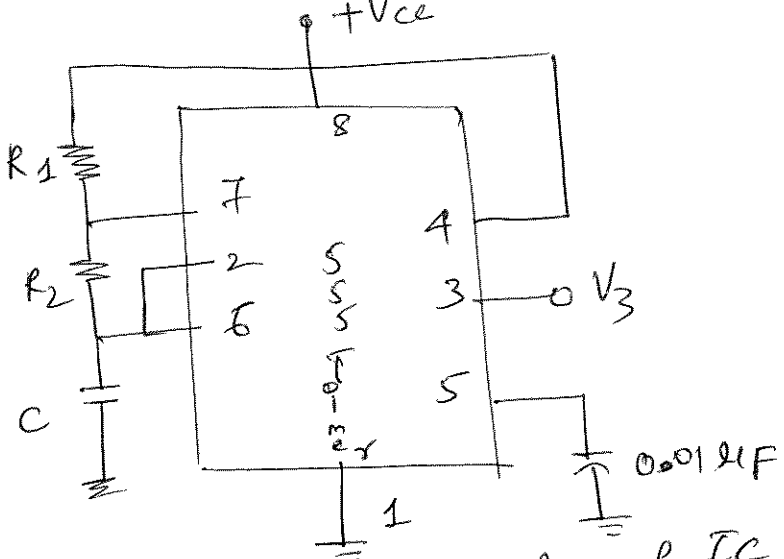


Fig (4). Astable operation of IC 555 timer.

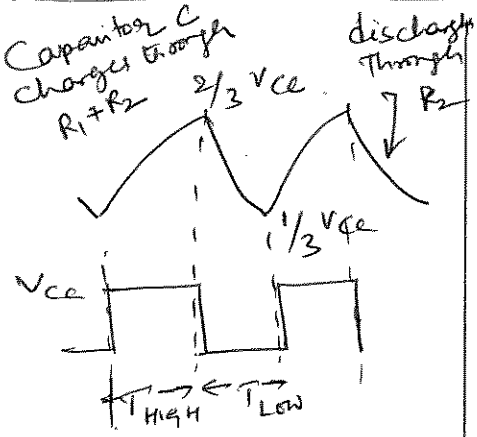
The capacitor begins to charge from the dc source Vcc when the voltage of the threshold pin 6 tends to increase beyond 2/3 Vcc, the comparator 1 saturates & its output triggers the flipflop and so the output at pin 3 goes low.

At the same time, the transistor becomes ON causing the output at pin 7 to discharge the capacitor through R_2 at time constant $\tau_2 = R_2 C$.

As the capacitor voltage which is the trigger input at pin 2 falls below (1/3) Vcc, the comparator 2 output causes the flip-flop to reset, the output at pin 3 becomes high & the transistor goes OFF.

The capacitor now begins to charge through R_1 & R_2 at time constant $\tau_1 = (R_1 + R_2) C$. The process then repeats continuously.

The output waveform & Capacitor charging & discharging are shown in fig. (5).



Fig(5) output waveform & Capacitor charging & discharging cycle.

The exponential expression for R_2C discharging and (R_1+R_2) charging from Vcc we can find T_{High} & T_{Low} periods.

Duty cycle of square wave is given by $D = T_{ON}/T$.

T is sum of charging time (T_{High}) & T_{OFF} discharging time.

The value of T_{High} or the charge time is given by

$$T_{High} = 0.693 * (R_1 + R_2) C$$

The value of T_{Low} or the discharge time is given by

$$T_{Low} = 0.693 * R_2 C$$

Therefore the time period for the cycle T is given by

The oscillation period

$$T = T_{High} + T_{Low} = T_{ON} + T_{OFF}.$$

The oscillation frequency $= 0.693 * (R_1+R_2)C + 0.693 R_2 C.$

$$T = 0.693 (R_1 + 2R_2) C.$$

$$f = \frac{1}{T} = \frac{1}{0.693 * (R_1+2R_2) C}.$$

$$= \frac{1.44}{(R_1+2R_2) \cdot C}.$$

Duty cycle is given by

$$D = \frac{T_{high}}{T} = \frac{T_{high}}{T_{high} + T_{low}}$$

$$= \frac{0.693 (R_1 + R_2) C}{0.693 (R_1 + 2R_2) C}$$

$$= \frac{R_1 + R_2}{R_1 + 2R_2} \text{ ; less than 50\%}$$

Derivation of charging and discharging Time

Discharging:- $V_c(t_1) = \frac{2}{3} V_{cc} e^{-t_1/\tau_1} = \frac{1}{3} V_{cc}$

$$2 e^{-t_1/\tau_1} = 1, \quad \log_e 2 - \log_e e^{-t_1/\tau_1} = \log_e 1$$

$$= \ln 2 - \frac{t_1}{\tau_1} = 0$$

OR $\boxed{t_1 = \tau_1 \ln 2}$

Charging:- $V_c(t) = V_{cc} + A \cdot e^{-t/\tau_2}$

At t_2, $V_c(t_2) = V_{cc} + A \cdot e^{-t/\tau_2} = \frac{1}{3} V_{cc}$

Substitute $A = -\frac{2}{3} V_{cc}$

$$V_c(t_2) = V_{cc} - \frac{2}{3} V_{cc} e^{-t/\tau_2} = \frac{2}{3} V_{cc}$$

$$1 - \frac{2}{3} e^{-t_2/\tau_2} = \frac{2}{3} \Rightarrow 1 - \frac{2}{3} = \frac{2}{3} e^{-t_2/\tau_2}$$

$$\frac{1}{3} = \frac{2}{3} e^{-t_2/\tau_2} \Rightarrow 2 e^{-t_2/\tau_2} = 1$$

$$= \ln 2 + \ln e^{-t_2/\tau_2} = \ln 1$$

$$\ln 2 - t_2/\tau_2 \ln e = 0$$

$$\ln 2 - t_2/\tau_2 \ln e = 0 \qquad \ln e = 1.$$

$$t_2/\tau_2 = \ln 2 \qquad \log_e e = 1.$$

$$\boxed{t_2 = \tau_2 \ln 2}$$

Module 5.

Digital Electronic Fundamentals:.

Difference between analog & digital signals
Number system - Binary Hexadecimal
Conversion - Decimal to Binary
Hexadecimal to decimal and vice-versa

Boolean algebra

Basic and universal gates

Half and Full adder

Multiplexer,

Decoder

SR & JK FlipFlops.

Shift Register, 3-bit Ripple Counter

(refer 10.1 - 10.7 of Text 1)

Basic Communication system

principle of operations of mobile phone

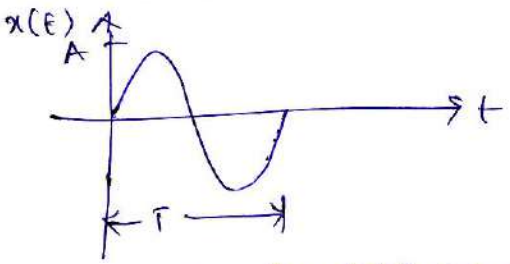
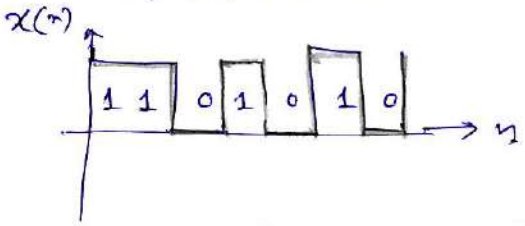
(refer 18.2 and 18.18 of Text 1).

RBT Levels: L1 & L2

Difference between Analog signals & Digital signals

Analog signal : An analog signal is a continuous signal they have infinite number of possible values.
Example sine wave. voice signal. vedio signal.

Digital signal :- These are the discrete & Non continuous signal has finite number of possible values. Example Computer Data. Data storage on memory. It has two possible values binary '1' and '0'.

Analog signal.	Digital signal.
1. An Analog signal is a signal that can have one of infinite number of possible values.	A digital signal is a signal that can have one of finite set of possible values at any time.
2. Analog signal is a continuous signal which represents physical measurements.	Digital signals are non-continuous & discrete in nature.
3. Denoted by sine wave. $x(t) = A\sin(2\pi ft + \phi)$. 	Denoted by square wave. 1 | 0 | 0 | 0 . 
4. uses continuous range of values to represent Information	uses discrete or discontinuous values to represent information.
5. Analog signals are more affected by Noise or distortion during transmission	Digital signals are less immune to Noise or distortion during transmission.
6. They are best suited for transmission of audio & vedio.	They are best suited for transmission of computer Data.

Introduction to Number system.

Number system is the Basis for Counting various items. The representation of Numerals in a specific way is called Number system. We already know the familiar decimal number system with its 10 digits . 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

Modern Computers Communicate and operate with binary numbers which use only the digits 0 & 1.

The representation of Decimal number, in binary format takes more digits. For large decimal number, the binary string is large. and ∴ They do not like working with binary numbers. This facts gives rise to three new number system namely. Octal, Hexadecimal and Binary Coded decimal.

Different Number systems

The different Number systems are

- Decimal System
- Hexadecimal Number System
- Binary Number System
- Octal Number System.

Decimal Number System.

Decimal Number can be expressed in terms of units, tens, hundreds, thousands & so on. Decimal Number 5678.9 can be written as $5000 + 600 + 70 + 8 + 0.9 = 5678.9$

The base of the Decimal number system is 10, d, or D. It written as a subscript. The position of a digit with reference to the decimal point determines its value/weight. In above Example the left most digit, which has greatest weight is called most significant digit (MSD). The right most digit, has least weight is called least Significant Bit (LSD).

(1). 5 6 7 8 . 9

In powers of 10 5×10^3 6×10^2 7×10^1 8×10^0 . 9×10^{-1}.

Any number in this decimal system is represented by using the symbols.

0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

Another Eg: $(5689.723)_{10}$

Number	5	6	8	9	.	7	2	3
position.	Digit 3	Digit 2	Digit 1	Digit 0	.	Digit -1	Digit -2	Digit -3.
weightage	10^3	10^2	10^1	10^0		10^{-1}	10^{-2}	10^{-3}

MSD. LSD.

Explain Binary number system.

Binary system with its two digits is a base-two system.
The binary digits (bits) are 0 & 1.
Each symbol that appear in the number is called a Bit.
Each bit has a weightage which depends on the position of the bit in the number.
. The right most bit is called least significant bit. weightage is 2^0. The weightage of bit one left hand side to the Least significant bit is 2^1. Thus as we move to the left the weightage of the bit increases by the multiple of 2.

Eg.

	MSB			LSB
Number	1	0	1	1
position.	bit 3	bit 2	bit 1	bit 0.
weightage.	2^3	2^2	2^1	2^0

$1\times2^3 + 1\times2^1 + 1\times2^0 = 8+2+1 = (11)_{10}$

for fraction.

Number	1	1	0	0	.	1	1
position	bit 3	bit 2	bit 1	bit 0	.	bit -1	bit -2
weightage	2^3	2^2	2^1	2^0	.	2^{-1}	2^{-2}

$1\times2^3 + 1\times2^2 + 1\times2^{-1} + 1\times2^{-2}$
$= 8+4+0.5+0.25 = (12.75)_d = (1100.11)_2$.

Octal number system:-

Any number in this number system is represented by using the symbols.

0, 1, 2, 3, 4, 5, 6, 7.

Consider Example of representing 2356 in octal representation.

- Each symbol in the number is called as Digit.
- Each digit has a weightage which depends on the position of the digit in the number.
- The right most digit is called Least Significant digit.
- The weightage of this digit is 8^0.
- The weightage of the digit on the left hand side of the LSD is 8^1.
- Thus as we move to the left the weightage of the digit increase by the multiple of 8.

Eg.

Number	2	3	4	1
position	Digit 3	Digit 2	Digit 1	Digit 0
weightage	8^3	8^2	8^1	8^0

The value of digit 2 is.

$= 3 \times 8^2 = 3 \times 64 = 192.$

number	1	2	3	.	4	3	1
position.	Digit 2	D-1	D-D	.	Digit -1	-2	-3
weightage	8^2	8^1	8^0	.	8^{-1}	8^{-2}	8^{-3}

The value of Digit 1 is

$= 2 \times 8^1 = 16.$

Digit 2 is

$1 \times 8^2 = 64.$

$= 1\times8^2 + 2\times8^1 + 3\times8^0 + 4\times8^{-1} + 3\times8^{-2} + 1\times8^{-3} = (83.548)_{10}$

Hexadecimal Number System

The hexadecimal number system has a base of 16 having 16 characters. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.

For Example. 32A.1B can be represented in power of 16 as shown below.

3	2	A	.	1	B
Digit 2	Digit 1	Digit 0	.	Digit -1	Digit -2
16^2	16^1	16^0	.	16^{-1}	16^{-2}

$$N = 3\times16^2 + 2\times16^1 + A\times16 + 1\times16^{-1} + B\times16^{-2}.$$

$$= 3\times256 + 2\times16 + 10\times16 + 1\times16^{-1} + 11\times16^{-2}.$$

$$= (960.1054688)_{10}. \quad = (960.1054688)_{10}.$$

Each symbol that appears in the number is called a digit. Each digit has a weightage which depends on the position of the digit in the number.

Number	2	3	5	6
position.	Digit 3	Digit 2	Digit 1	Digit 0.
weightage.	16^3	16^2	16^1	16^0

$$2\times16^3 + 3\times16^2 + 5\times16^1 + 6\times16^0.$$

The value of digit 2 is. $= 2\times16^2$

$= 3\times256$

$= 768.$

$$N = 2\times16^3 + 3\times16^2 + 5\times16^1 + 6\times16^0.$$

N	0	.	1	2	3
P	[illegible]	.	B^{-1}	-2	-3
W	[illegible]	.	16^{-1}	16^{-2}	16^{-3}

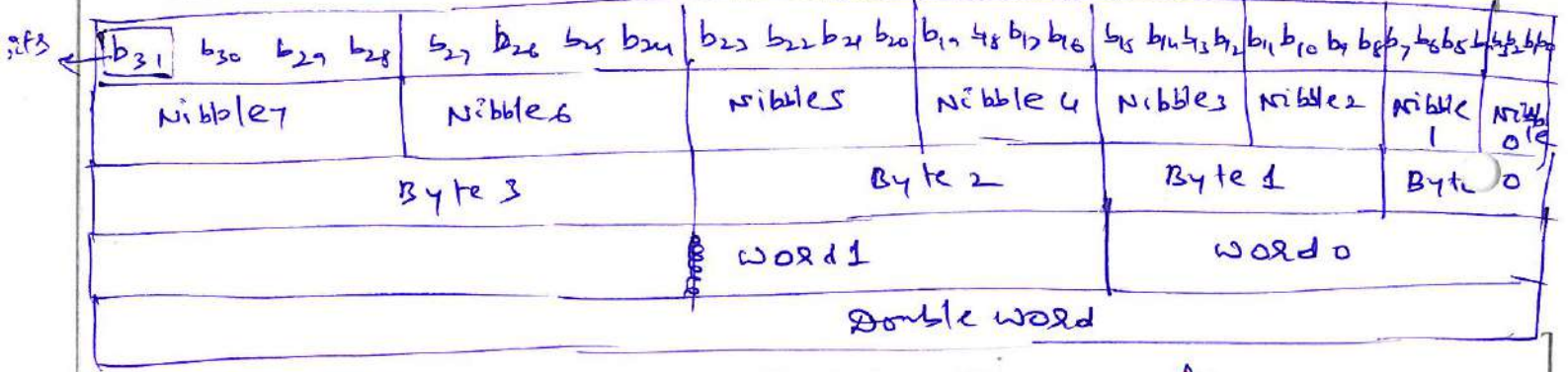
0+

$= (0.07104)_{10}.$

Relationship between decimal binary, Octal & Hexadecimal no.'s

Decimal	Binary	octal	Hexadecimal
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F.

What do you mean by bits, bytes, nibbles, word Doubleword.



A Number can be represented by the equation general equation.

$$N = d_n * R^n + d_{n-1} * R^{n-1} + \dots + d_2 * R^2 + d_1 * R^1 + d_0 * R^0$$

N → value of the entire number.

d_n → is the value of the n^{th} digit form the decimal point, and.

R → is the radix or base.

Number of digital $(n+1)$; $(0, 1, 2 \dots n)$

Conversion between Decimal, octal, Hexadecimal and Binary Numbers:-

general :- Conversion from any number system to Decimal.

step 1 : Identify the weightage of each digit in the number system.

step 2 : multiply each digit by the weightage of the digit.

step 3 : add all the products.

Binary to Decimal Conversion

(1) Convert the given binary number 11010 into decimal.

position.	Bit 4.	Bit 3	Bit 2	Bit 1	Bit 0
given Number :	1	1	0	1	0
Weightage :	2^4	2^3	2^2	2^1	2^0

$= 1\times2^4 + 1\times2^3 + 0\times2^2 + 1\times2^1 + 0\times2^0$

$= 16 + 8 + 0 + 2 + 0 = 26$

$\therefore (11010)_2 = (26)_{10}$

(2) $(1101101)_2$ to decimal.

position :	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
given No. :	1	1	0	1	1	0	1
weightage :	2^6	2^5	2^4	2^3	2^2	2^1	2^0

$= 1\times2^6 + 1\times2^5 + 0\times2^4 + 1\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0$

$= 64 + 32 + 0 + 8 + 4 + 0 + 1$

$= (109)_{10}$

Converting Binary Number 1011.110 to Decimal.

position	Bit 3	Bit 2	Bit 1	Bit 0 .	Bit -1	Bit -2	Bit -3
Binary No.	1	0	1	1	1	1	0
Weightage	2^3	2^2	2^1	2^0 .	2^{-1}	2^{-2}	2^{-3}

$= (1\times 2^3 + 0\times 2^2 + 1\times 2^1 + 1\times 2^0) + (1\times 2^{-1} + 1\times 2^{-2} + 0\times 2^{-3})$.

$= (8 + 0 + 2 + 1) + (0.5 + 0.25 + 0)$

$= (11.75)_{10}$

Convert given octal Number 212 into decimal.

position =	Digit 2	Digit 1	Digit 0
given No. =	2	1	2
weightage =	8^2	8^1	8^0

$N = 2\times 8^2 + 1\times 8^1 + 2\times 8^0$.

$= 2\times 64 + 1\times 8 + 2\times 1$

$= 128 + 10 = (138)_{10}$.

Convert $(235.67)_8 = (\ ?\ )_{10}$

position	Digit 2	Digit 1	Digit 0 .	Digit -1	Digit -2
Number	2	3	5 .	6	7
weightage	8^2	8^1	8^0	8^{-1}	8^{-2}

$= 2\times 8^2 + 3\times 8^1 + 5\times 8^0 + 6\times 8^{-1} + 7\times 8^{-2}$

$= 2\times 64 + 24 + 5 + 0.75 + 0.109375$

$= (157.8594)_{10}$

Convert given Hexadecimal No. to Decimal.

(i) $(285.A9)_{16} = (?)_{10}$

position	Digit2	Digit1	Digit0	.	Digit-1	Digit-2
No.	2	8	5	.	A	9
Weightage	16^2	16^1	16^0	.	16^{-1}	16^{-2}

$= 2\times16^2 + 8\times16^1 + 5\times16^0 + (10\times16^{-1}) + (9\times16^{-2})$.

$= 512 + 128 + 5 + 0.625 + 0.03516$

$= (645.66016)_{10}$

(ii). $(235)_{16} = (?)_{10}$.

position	Digit2	Digit1	Digit0.
Number	2	3	5
weigutage	16^2	16^1	16^0

$= 2\times16^2 + 3\times16^1 + 5\times16^0$

$= 2\times256 + 3\times16 + 5\times1$

$= (565)_{10}$.

Case 2:- Conversion of number in decimal Number system to any other Number System.

Integer part Conversion [successive division for Integer part]

- perform repeated division of given decimal value by the base of number system into which the conversion is required.
- After each division, the remainder is taken as one digit / bit in destination number system.
- For the next devision, take the quotient of the previous division as the dividend.

For fractional part Conversion [successive multiplication for fractional part]

perform the repeated multiplication of the fractional part of the decimal Number with the base of the number system. into which the conversion required.

- after each conversion, the integer part is taken as one digit / bit in the destination number system.
- For the next multiplication, take only previous fractional part
- repeat above steps till fractional part of the ~~previous~~ multiplication becomes '0'. (or until desired value we get.

Decimal to Binary:-

① $(25.625)_{10} = (?)_2$

Integer

2 | 25
2 | 12 - 1
2 | 6 - 0
2 | 3 - 0
1 - 1

LSB ↑ MSB

fractional.

0.625 × 2
1 ← 1.25
0.25 × 2
0 ← 0.5 × 2
1 ← 1.0

$= (11001.101)_2$.

② $(264.325)_{10} = (?)_2$.

2 | 264
2 | 132 - 0
2 | 66 - 0
2 | 33 - 0
2 | 16 - 1
2 | 8 - 0
2 | 4 - 0
1 - 0

LSB ↑ MSB

0.325 × 2
0.65 → 0.
× 2
1.3 → 1
0.3 × 2
0.6 → 0.
× 2
1.2 → 1
0.2 × 2
0.4 × 2 - 0
0.8 × 2 - 0
1.6 - 1

$(264.325)_{10} = (10001000.0101001)_2$

Convert the Decimal number 75.62 into octal. Approximate the Result to first four places.

(1) $(75.62)_{10} = (??)_8$.

8 | 75. Remainder.
8 | 9 - 3 ↑ LSD
8 | 1 - 1
0 - 1 MSD

$(113.4753)_8$.

0.62×8
$4.96 \rightarrow 4$
0.96×8
$7.68 \rightarrow 7$
0.68×8
$5.44 \rightarrow 5$
0.44×8
$3.52 \rightarrow 3$

(2). $(384.832)_{10} = (?)_8$.

8 | 384
8 | 48 - 0
6 - 0

$(600.6517)_8$

0.832×8
$6.656 \rightarrow 6$
0.656×8
$5.248 \rightarrow 5$
0.248×8
$1.984 \rightarrow 1$
0.984×8
$7.872 \rightarrow 7$

Solve $(658.825)_{10} = (?)_8$

(2). $(12.125)_{10} = (?)_2$.

Convert 5386.345 decimal into hexadecimal

Conversion of Integer part by successive division method.

16 | 5386
16 | 336 – A
16 | 21 – 0
1 – 5

$(150A.5851\ldots)_{16}$

0.345×16
$5.52 \rightarrow 5.$
0.52×16
$8.32 \rightarrow 8$
0.32×16
$5.12 \rightarrow 5$
0.12×16
$1.92 \rightarrow 1$

Convert $(196.284)_{10} = (?)_{16}$

16 | 196
16 | 12 – 4
D – C

$(C4)_{16}$

$(C4.48B)_{16}$

0.284×16
$4.544 \rightarrow 4$
0.544×16
$8.704 \rightarrow 8$
0.704
$11.264 \rightarrow 11$

Conversion from Binary into octal

Step 1: Arrange group of 3 bits starting from LSB for Integer part & MSB for fractional part, by adding 0's at the end, if required.

Step 2: Write equivalent octal No. for each group of 3-bits.

Decimal	Binary	octal
0	000	0
1	001	1
2	010	2
3	011	3
4	100	4
5	101	5
6	110	6
7	111	7
8	1000	10

Convert 1010110.0111 to octal equivalent

$(\boxed{0}10\ 101\ 101.011\ 1\boxed{00})_2$ → Adding Zero's to make a group of 3 bits.

Adding 0 to make a group of 3 bits.

$(255.34)_8$

Octal to Binary Conversion :-

Each octal No. is converted individually to its Binary equivalent to get binary conversion.

Convert $(125.62)_8$ to binary.

Step 1 : Write equivalent 3-bit binary no. for each octal digit.

Step 2 : Remove any leading or trailing zeros

$(1 \quad 2 \quad 5 \quad . \quad 6 \quad 2)_8$

$(\boxed{0}0 \quad 010 \quad 101 \quad . \quad 110 \quad 010)_2$

Leading zero. Trailing zero.

$= (1010101.11001)_2$

Conversion from binary into Hexadecimal the following table is used.

Decimal	binary	Hexadecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F
16	10000	10
17	10001	11

Convert 1101101.101011 into Hexadecimal

$\boxed{0}110 \quad 1101 . \quad 1010 \quad 1110$

$(6 \quad D \quad . \quad AE)_{16}$

Convert binary to Hexadecimal

$(1101101110.100110)_2 = (\quad)_{16}$

$0011 \quad 0110 \quad 1110 . \quad 1001 \quad 1010$

$(3 \quad 6 \quad E \quad . \quad 9 \quad A)_{16}$

HEXADECIMAL to Binary

Convert $(8A9.BA)_{16} = (?)_2$

Step 1 $1000 \quad 1010 \quad 1001 . \quad 1011 \quad 1010$

Step 2 $(100010101001.10111010)_2$

Convert given Hexa to binary.

$(345.AB)_{16} = (?)_2$.

0011 0100 0101 . 1010 1011

$(1101000101.10101011)_2$.

Octal to Hexadecimal ;—

1. Convert octal no. into binary
2. from binary no. convert to Hexadecimal

Convert $(615.25)_8$ to its Hexadecimal equivalent.

Step 1 : (110 001 101 . 010 101.)$_8$

0001 1000 1101 . 0101 0100.

$(1\ 8\ D\ .\ 5\ 4)_{16}$.

Convert Hexadecimal to octal Conversion.

Convert Hexa to binary

Convert binary no. to its octal equivalent.

Convert $(BC66.AF)_{16}$ to octal.

B C 6 6 . A F

Step 1 1011 1100 0110 0110 . 1010 1111

Step 2 001 011 110 001 100 110 . 101 011 110

Step 3 $(1\ 3\ 6\ 1\ 4\ 6\ .\ 5\ 3\ 6)_8$.

Binary representation of decimal Numbers from 0 to 15. is shown below in table. Binary digits in short form we call as bits. These numbers can take only one of the two values.

The primary advantage of using the binary number system as opposed to the 10 discrete line method in Decimal number system is that it minimises the number of lines required to two.

Binary numbers are used in digital systems.

A logic 1 can be represented by a saturated transistor, a light turned ON, a relay energised or a magnet magnetised in a particular direction.

A '0' can be represented as a cut-off transistor, a light turned off, a de-energised relay, or the magnet magnetised in the opposite direction.

Binary	Decimal
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

Converting Decimal to Binary

Decimal to Binary Conversion.

	power of 2	
n	2^n	2^{-n}
0	1	1.0
1	2	0.5
2	4	0.25
3	8	0.125
4	16	0.0625
5	32	0.03125
6	64	0.015625
7	128	0.0078125
8	256	0.00390625
9	512	0.001953125
10	1024	0.0009765625
11	2048	0.00048828125
12	4096	0.000244140625
13	8192	0.0001220703125
14	16348	0.0000 6103515625
15	32768	0.00003051757 8125
16	65536	0.000015258789 0623

Convert $(69)_{10}$ to Binary

From Table 64 is largest number without exceeding 65

$69 > 64$:

$64 = 1000000_2$, $69 - 64 = 5$.

From table 4 is largest number without exceeding 5

$4 = 100_2$ $\quad 5 - 4 = 1$ one is the largest number in the table.

$1 = 1_2$. $\quad 1000000$

100

1

$(69)_{10} = (1000101)_2$

Division method.

$(69)_{10} = (?)_2$

2 | 69

2 | 34 - 1

2 | 17 - 0

2 | 8 - 1

2 | 4 - 0

2 | 2 - 0

1 - 0

$(69)_{10} = (1000101)_2$

Binary Addition and Subtraction.

Similar to Decimal addition.

Binary addition.

The simple addition consists of Four possible elementary operations, namely.

$0+0=0$

$0+1=1$

$1+0=1$

$1+1=10_2$

In above case the first three operation produces a sum whose length is one digit, but when the last operation is performed sum is two digits. Higher significant Bit of this result is called Carry. Lower significant Bit is called Sum.
This operation is known as Half addition.

Full addition:-

The operation which performs addition of three bits {(two significant bits) and one Carry (previous)} is called a Full addition.

Table shows the truth table for Full addition.

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

① Add 10111_2 and 10111_2

Carry 1 1 1 1 1
Number 1 1 0 1 1 1 1
Number 2 1 0 1 1 1

$1\ 0\ 0\ 0\ 1\ 1\ 0_2$

② ADD. 1111 and 1111

Carry 1 1 1
Number 1 1 1 1 1
Number 2 1 1 1 1

$1\ 1\ 1\ 1\ 0_2$.

Binary Subtraction :-

① Subtract 1110 from 10000

Borrow
10000
1110.

$0\ 0\ 0\ 1\ 0_2$.

② Subtract 10101 from 101010.

Borrow
101010
10101

$0\ 1\ 0\ 1\ 0\ 1_2$.

Binary multiplication.

① Multiply 1111_2 by 101_2.

1111 * 101

1111
0000
1111

1001011_2.
Result is 8 bit.
$=(0100\ 1011)_2$

② Divide 110110_2 by 110_2.

```
      1001
   ------
110 ) 110110
      110↓↓↓
   ------
      000110
         110.
      ------
           0.
```

These two are called paper methods.

Computer uses. Different multiplication methods.

And different Division method. Such one Long division method is Explained Here

Computer Division method.

It is successive subtraction.

8 bit dividend is to be divided by the devisior in 4-bit representation.

dividend = 00110110 , divisor = 0110.

The Quotient will be formed in the right half of the MQ register and the remainder in the left half.

(1) MQ register = 00110110 D register = 0110.

(2) The divisor is then subtracted from the dividend.
if MSB = 0, then +ve number.
MSB = 1 then negative number.

(3) If the result is positive then the error has occurred for the quotient would be greater than four bits.

MQ : 0011 0110

Subtract D : 0110

→ 1101 0110 Result is negative, the division is valid.

MQ → 0110

Add D : 0110

MQ : 1 0011 0110

Shift MQ left 0110 1100

Subtract D 0110

MQ : 0000 1100 Result is positive

Add 1 to Quotient 0001 1100

MQ :

Shift MQ left 0001 1010

Subtract D 0110

1011 1010 Result is negative

Add D 0110

0001 1010 put a zero Quotient

MQ - 0001 1010

Shift MQ left 0011 0100

Subtract D 0110

1101 0100 Result is negative.

Add D 0110

1 0011 0100

Shift MQ left 0110 1000

Subtract D 0110

0000 1000 Result is positive.

Add 1 to Quotient 1

0000 1001 Final answer.

Remainder Quotient.

If the result is negative then the quotient will be four or less bits that is sufficiently small to be contained in a 4-bit register.

The MQ register is next shifted left one bit & the divisor subtracted from it.

If the result is positive, 1 is added to the LSB (least significant Bit) of the MQ register, which as quotient is accumulated.

If it is negative, the divisor is added to MQ & the MQ shifted left one bit.

This effectively puts a '0' in this bit of quotient.

The process is continued untill the MQ register has been shifted left four bits the number of bits in the D register.

The remainder is then in the left half of the MQ register & the quotient in the right half.

Complement of Binary numbers :-

In Digital computer arithmetic process is done not only with positive Numbers; we also do it with -ve(negative) number.

Processor manages the signed numbers and unsigned Numbers. The 1's & 2's Complement are useful in this case.

What is 1's Complement?

1's Complement of a binary number is just an inversion of individual bit's i.e 1 to 0, & 0 to 1.

1's Complement of $(1010101)_2$ is.

$$=(0101010)_2.$$

2's complemant

The 2's Complemant of binary number is addition of 1 to the 1's Complement of that binary number.

Eg. 2's complement of $(10101011)_2$.

1's Complement 01010100.

ADD 1 to LSB. 1

$(01010101)_2$.

It also holds to Decimal binary number.

Find 2's Complement of 0.1110100.

First 1's complement 0.0001011

ADD 1 to LSB. 1

$(0.0001100)_2$

2's Complement of Floating point Number

Eg ①. (010111.1100) Compute 2's Complement.

Step 1's Complement 101000.0011

ADD. 1 1

$(101000.0100)_2$.

Difference of Two positive Binary Number (m-n).

Consider two binary Numbers m & n. To subtract n from m. we can follow these steps.

1. ADD 2's complement of n to m.
2. Neglect (or Delete) the Carry at the left end, if Carry is present.
3. The result is (m-n).
4. If sum has no carry at the left End, take 2's complement of the sum. Attach a negative sign. The result is (m-n).

Example :-

given m = 11010110 n = 01000101.

Find (m-n) & (n-m).

① 2's Complement of n.

n = 01000101

1'scomp. 10111010.

ADD 1 1

10111011

111

m = 11010110.

10111011

1 10010001

(m-n) = $(10010001)_2$.

(b) n-m

2's complement of m.

m = 11010110.

1's comp. 00101001

Add 1' 1

00101010

n = 01000101

00101010

No carry. 01101111

1's comple. 10010000.

1

10010001

$(n-m) = -10010001$

Binary subtraction using 2's complent method.

$(28)_{10} - (19)_{10}$

Binary number $(28)_{10}$ 011100

$(19)_{10}$ 010011

Let 2's Complement of 19

010011

101100

1

101101

Carry 111

28 011100

19 101101

[1] 001001

Delete

Result = $(001001)_2 = (9)_{10}$.

$(19)_{10} - (28)_{10}$.

19 = 010011

28 = 011100.

2's complant of 28 ⇒ 011100

100011

1

100100.

19 010011

2's 28 100100

110111 → No Carry.

Result is -ve.

Then 2's complant of Result.

→ 001000

001001

The result = $-(001001)_2$.

Subtract using 2's Complement

(i). 4 - 9

4 - 0100

9 - 1001 → 2's complant

0110

1

0111

0100

0111

1011

No carry.

result -ve.

take 2's Complant

0100

1

$(0101)_2$

$-(0101)_2$ $(-5)_{10}$

(ii). 8 - 2

1000 → 8.

0010 → 2

Take 2's complement of 2.

1101.

1

1110

1000

1110

11 0110

neglect

result is +ve.

Result = 0110_2 $(6)_{10}$

Computer Division method.

It uses successive subtraction.

dividend is 01101110.

divisor is 0110.

The Answer is 0000 1001

8 bit Number.

① Add $(28)_{10}$ and $(15)_{10}$ Converting them into binary

$(28)_{10} = 11100$

$(15)_{10} = 1111$

Carry 1 1

11100 — 28

1111 — +15

$(101011)_2$ — 43

2 | 28

2 | 14 — 0

2 | 7 — 0

2 | 3 — 1

1 — 1

Subtraction using 1's Complement Method.

operation M-n using 1' Complement.

1. Take 1's complement of n
2. Result ← M + 1's complement of n.
3. If carry is generated, result is +ve, add in the true form, Add carry to the result to get the final result.
4. If carry is not generated then the result is -ve and in the 1's Complant form.

perform: ① $(28)_{10} - (19)_{10}$ using 1's Complement

$(19)_{10}$ Binary 010011

1's 101100.

$(28)_{10}$ Binary 011100.

```
Carry   1 1 1
28      0 1 1 1 0 0
19  +   1 0 1 1 0 0
    -------------
    [1] 0 0 1 0 0 0
     |              1.
    -------------
    0 0 1 0 0 1   → Result (9)10.
```

② $(19) - (28)_{10}$.

Binary equivalent of 19 = 010011

Binary equivalent of 28 = 011100

Take 1's complement of 011100

100011 → 1's comp 28.

```
Carry    1 1
         0 1 0 0 1 1
         1 0 0 0 1 1
    -------------
         1 1 0 1 1 0   No carry, Negative Result
                       Take 1's complement
         0 0 1 0 0 1
    -------------
```

$-(001001)_2 = (-9)_{10}$ Result.

Boolean Algebra Theorems

In 1854 George Boole invented a systematic treatment of logic for algebraic system.
Boolean algebra is a system of mathematical logic It differs from both ordinary algebra and the binary number system.

Variable :- The symbol which represent an arbitrary elements of an Boolean Algebra is known as variable variables is called biliteral, These can take on two values, binary 1 or 0. It may be any alphabet.

Constant :- The constant value may be '1' or 0.
For Example In Expression $Y = A + 1$ Here A is a variable, 1 is constant.

Complement : A Complement of a variable is represented by a bar over the letter.
Example: Complement of $A = \overline{A}$.
A prime symbol ' is also used instead of bar.

Literal :- Each occurrence of a variable in Boolean function either in a complemented or an uncomplemented form is called a **Literal.**

Boolean function :-
Boolean expressions are constructed by connecting the Boolean constants and variables with the Boolean operations. These Boolean expressions are called Boolean functions.
Example. (1). $f(A, B, C) = (A + \bar{B}) \cdot C$
$f = AB + BC + CA$

Boolean Laws.

AND Law - Multiplication Symbol (·)

$Y = A \text{ AND } B \Rightarrow Y = A \cdot B$.

In AND operation, the output is 1 only if both A and B are 1; otherwise it is zero.

Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Law - Addition symbol. (+).

$Y = A \text{ OR } B \Rightarrow Y = A + B$.

In the OR operation, the result is '1' if either A or B or both are 1.

Truth Table.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOT - Complement symbol (Super -, Super')

$Y = \bar{A}$

$Y = A'$

In NOT operation, the output is the result of input

Truth table

A	Y
0	1
1	0

Special Case;

AND operation : $A \cdot 0 = 0$ $A \cdot 1 = A$, $A \cdot A = A$ $A \cdot \bar{A} = 0$

OR operation $A + 0 = A$ $A + 1 = 1$ $A + A = A$ $A + \bar{A} = 1$

NOT operation $\overline{\bar{A}} = A$

$\overline{\overline{\bar{A}}} = \bar{A}$

$\overline{\overline{\overline{\bar{A}}}} = A$.

Identity Law: $1 \cdot A = A$ $\quad 0 + A = A$

Laws of Boolean Algebra.

Three Basic algebra laws.

- Communicative Laws.
- Associative laws.
- Distibutive Law.

Communicative Laws.

Law I : $A + B = B + A$. This states that the order in which the variables are ORed makes no difference in the output.

Proof. Law 1.

$A + B = B + A$.

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

B	A	B + A
0	0	0
0	1	1
1	0	1
1	1	1

Law 2:

$AB = BA$.

The commutative law of multiplication states that the order in which the variable are ANDed makes no difference in the output.

A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

B	A	BA
0	0	0
0	1	0
1	0	0
1	1	1

Associative Laws.

This law states that in the oRing of several variables the result is the same regardless of the grouping of the variables.

Law 1: $A + (B + C) = (A + B) + C$.

Idempotent law.

Idempotent Law is shown below.

$A + A = A$

$A \cdot A = A$

Redundance law (absorpane law)

$A + AB = A$

$A(A + B) = A$.

Inverse law

$A + \bar{A} = 1$

$A \cdot \bar{A} = 0$.

Null Law

$0 \cdot A = 0$ $\quad 1 + A =$

Law 2 :- $(AB)C = A(BC)$. The associative law of multiplication states that it makes no difference in what order the variable are grouped when ANDing several variables.

Distributive Law :-

Law : $A(B+C) = AB+AC$

The distributive law states that ORing several variables and ANDing the result with a single variable is equivalent to ANDing the result with a single variable with each of the several variables & then ORing the products.

Some identities of Boolean algebra

Name	AND form	OR form.
(1) Identity law	$1 \cdot A = A$	$0 + A = A$
(2) Null Law	$0 \cdot A = 0$	$1 + A = 1$
(3) Idempotent law	$A \cdot A = A$	$A + A = A$
(4) Inverse law	$A \cdot \bar{A} = 0$	$A + \bar{A} = 1$
(5) Commutative law	$A \cdot B = B \cdot A$	$A + B = B + A$
(6) Associative law	$(A \cdot B) \cdot C = A(B \cdot C)$	$(A+B)+C = A+(B+C)$.
(7) Distributive law	$A + BC = (A+B) \cdot (A+C)$	$A(B+C) = A \cdot B + A \cdot C$.
(8) Absorption law	$A \cdot (A+B) = A$	$A + AB = A$
(9) Demorgan's law	$\overline{A \cdot B} = \bar{A} + \bar{B}$	$\overline{A+B} = \bar{A} \cdot \bar{B}$

Proof. Distributive law.

$$\begin{aligned}(A+B)(A+C) &= A \cdot A + AB + AC + BC \\ &= A + AB + AC + BC \\ &= A[1 + (B+C)] + BC \\ &= A + BC \quad \text{as } 1+(B+C) = 1.\end{aligned}$$

Absorption Law

$$\begin{aligned}A(A+B) &= AA + AB \\ &= A + AB \\ A(1+B) &= A.\end{aligned}$$

Demorgan's Theorem :-

$$\overline{A+B} = \overline{A} \cdot \overline{B} \quad \text{and} \quad \overline{A \cdot B} = \overline{A} + \overline{B}$$

It states that any logical binary expressions remains unchanged if we.

1. Change all Variables to their complements.
2. Change all AND operations to ORs.
3. Change all OR operations to ANDs and
4. Take the complemant of the entire expression.

Truth table to prove Demorgan's theorems.

A	B	$\overline{A}$	$\overline{B}$	$\overline{A \cdot B}$	$\overline{A} + \overline{B}$	$\overline{A+B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1	1	1
0	1	1	0	1	1	0	0
1	0	0	1	1	1	0	0
1	1	0	0	0	0	0	0

Slove :-

$x + \overline{x} \cdot y = x + y$

$1 \cdot x + \overline{x} \cdot y$

$x \cdot (1+y) + \overline{x} y$

$x + xy + \overline{x} y$

$x + y(x + \overline{x})$

$x + y$

prove that.

$x \cdot y + y \cdot z + \overline{y} \cdot z = x \cdot y + z$

Consider LHS.

$x \cdot y + y \cdot z + \overline{y} z \cdot = xy + z(y + \overline{y})$

$= xy + z \cdot 1$

$= xy + z \cdot$ RHS

prove that

$x + y \cdot z = (x+y)(x+z)$

$x + yz$

$1 \cdot x + yz \cdot$

$x \cdot (1+y) + yz$

$x + xy + yz$

$x \cdot 1 + xy + yz$

$x(1+z) + xy + yz$

$= x \cdot 1 + xz + xy + yz$

$= x \cdot x + xy + xz + yz$

$= x(x+y) + z(x+y)$

$= (x+z)(x+y).$

Digital circuits

Digital circuit are divided into two major categories.

- Combinational circuits
- Sequential circuits.

Combinational circuits are circuits where output depends on the present input only.

The sequential circuit produces the output on the basis of both present & previous inputs. Sequential ckts have memory.

Logic gates: are the building blocks of digital circuits.

A logic gate is an electronic device with a single output having one or many inputs. The output is controlled by the input. gates used to create digit ckts & complex IC.

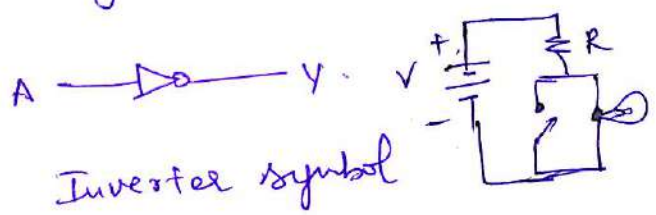
Complex Integrated circuits used to perform several functions

Eg. Microprocessor & Microcontoller.

① Not gate :-

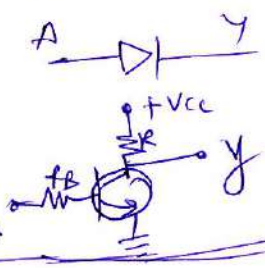
It is also known as an inverter, because it changes the input to its opposite.

A Low voltage input (0) is converted to a high voltage output; a high voltage (1) is converted to low voltage (0).

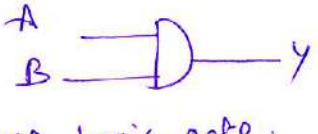


Input A.	o/p. Y
0	1
1	0

Truth table

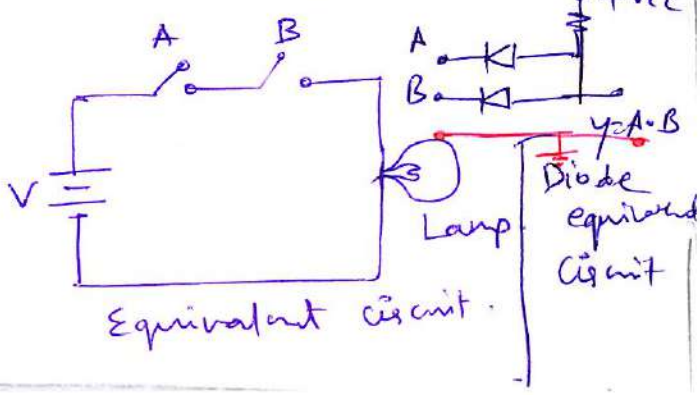


② AND gate :-



Input A	Input B	o/p. Y
0	0	0
0	1	0
1	0	0
1	1	1

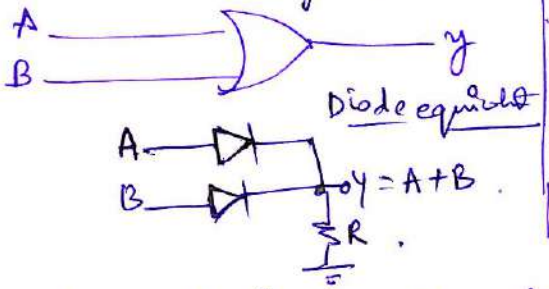
Truth table



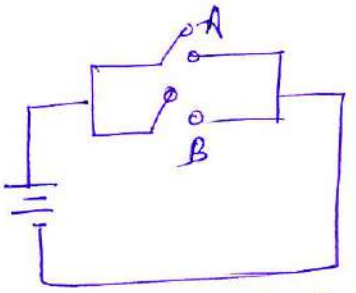
The Output of AND is gate is 1, only when all its Inputs are also '1'. otherwise, its output will be '0'.

OR gate

Symbol



A	B	y
0	0	0
0	1	1
1	0	1
1	1	1

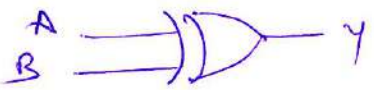


Equivalent circuit.

The output of OR gate will be '0' when all its Inputs are also '0'. otherwise its output will be '1'.

XOR gate:-

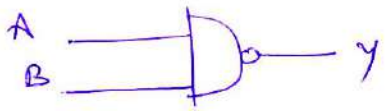
XOR stands for Exclusive OR. An XOR gate compares two Values & if they are different.
So its output will only be at '1' when all its inputs have the same value. otherwise, its output will be '1'.



A	B	y.
0	0	0
0	1	1
1	0	1
1	1	0

NAND gate:-

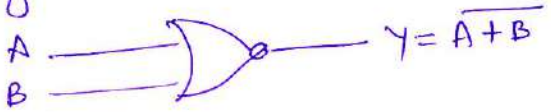
This is an AND gate with the output inverted. The output is high when either of inputs A or B is high. low if neither is high.



A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

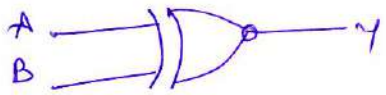
NOR gate:-

The OR gate with the output inverted is called NOR operation. The output is high only when neither A nor B are high.



A	B	y.
0	0	1
0	1	0
1	0	0
1	1	0

XNOR gate:- It is the complement of XOR gate. Its output is 1 when both inputs are equal i.e (0,0) or (1,1). XNOR operation is represented as $Y = A \odot B$.



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Non-inverter or buffer

The value entered on its input will be found on its output. A typical appln for a buffer is to increase the fan-out of a given logic gate.

Fan out is the maximum number of gates capable of being connected to a given integrated ckt is

A	Y
0	0
1	1

Algebraic simplification.

factorize the following equations.

(a) $Y = A\bar{B} + AB$

(b) $Y = AB + AC + BD + CD$

(c) $Y = (B + CA)(C + \bar{A}B)$

(d) $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$

(a) $Y = A\bar{B} + AB$.

$= A(\bar{B} + B)$

$= A \cdot 1$

$= A$

(b) $Y = AB + AC + BD + CD$

$= A(B + C) + D(B + C)$

$= (A + D)(B + C)$.

(c) $Y = (B + CA)(C + \bar{A}B)$

$= BC + CCA + \bar{A}BB + \bar{A}ABC$

$= BC + CA + \bar{A}B + 0$; $A\bar{A} = 0$ $B \cdot B = B$ $CC = C$

$= BC + \bar{A}B + AC$.

(d) $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}\bar{D} + A\bar{B}\bar{C}D$

$= \bar{A}\bar{B}\bar{C}(\bar{D}+D) + AB\bar{C}(\bar{D}+D)$

$= \bar{A}\bar{B}\bar{C}\cdot 1 + AB\bar{C}\cdot 1$

$= \bar{B}\bar{C}(\bar{A}+A)$

$= \bar{B}\bar{C}\cdot 1$

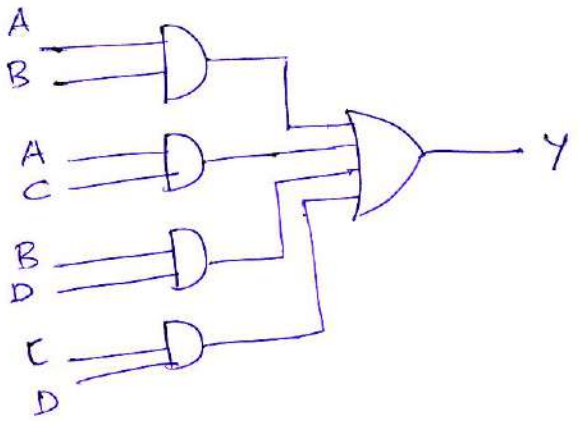
$= \bar{B}\bar{C}$

Compare the AND/OR gate realisation of the Boolean function of Example given below & its reduced form.

$Y = AB + AC + BD + CD$

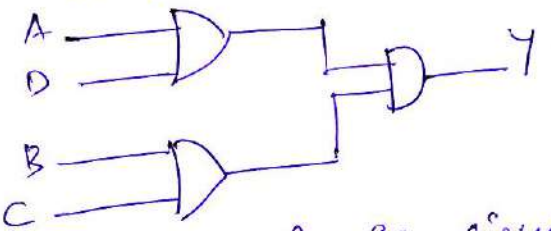
$= A(B+C) + D(B+C)$

$= (A+D)(B+C)$

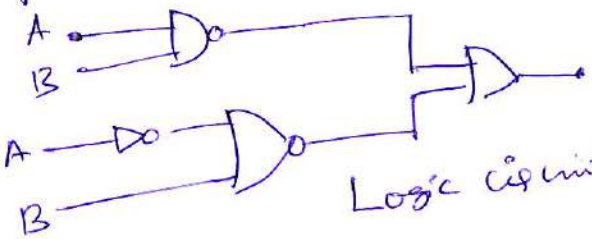


4 AND gates & 1 OR gate necessary implement the above Expression.

The simplified expression consists of only two AND and one OR gate.



Analyze the logic circuit of figure below and show that it can be replaced by a single NAND gate.



Logic circuit analysis.

$f = \overline{AB} + \bar{A} + B$

$= (\bar{A}+\bar{B}) + A\bar{B}$

$= \bar{A} + [\bar{B}(1+A)] = \bar{A} + \bar{B}\cdot 1 = \bar{A} + \bar{B} = \overline{A\cdot B}$ = Demorgan's law

Hence the above circuit is simply equivalent to NAND gate.

Sum-of product (SOP).

It is widely used for the canonical form i.e a OR (disjunction) of minterms. Its De morgan dual is a product of Sum (POS).

POS for the canonical form is a conjunction (AND) of maxterms.

minterms are called products because they are the logical AND of a set of variables.

Maxterms are called the sums because they are the logical OR of set of variable.

Example of SOP.

$$F = AB + C\bar{D} + \bar{B}C$$

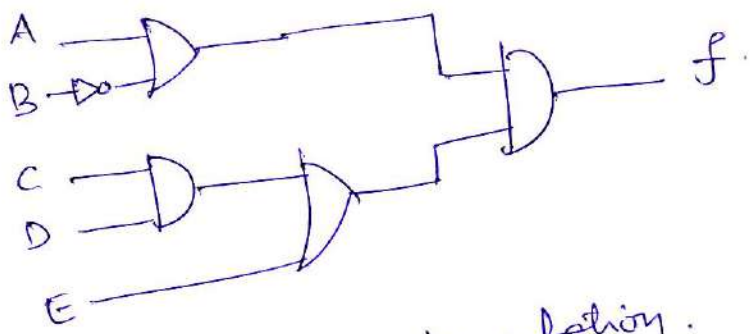
$$Y = A\bar{B} + \bar{A}B$$

POS

$$F = (A+B)(\bar{B}+C)(\bar{C}+D+E).$$

$$Y = (A+B)(C+D).$$

(1). For the Boolean function $f = (A+\bar{B})(CD+E)$. Obtain the AND-OR Implementation.



AND-OR Implementation.

Simplify and realize using basic gates

$Y = A + \bar{A}B + AB\bar{C}$

$= A(1 + B\bar{C}) + \bar{A}B$

$= A \cdot 1 + \bar{A}B$

$= A + \bar{A}B$

$= (A + \bar{A})(A + B)$

$A + BC = (A + B)(A + C)$

$A + \bar{A} = 1$

$= 1 \cdot (A + B)$

$Y = A + B$

Simplify -

$Y = A + \bar{A}B + ABC + A\bar{C} + AB$

$= A \cdot A + \bar{A}B + ABC + A\bar{C} + 0 + AB$

$= A \cdot A + \bar{A}B + ABC + A\bar{C} + A\bar{A} + AB$

$= A \cdot A + \bar{A}B + A\bar{A} + \bar{A}B + ABC + A\bar{C}$

$= A(A + B) + \bar{A}(B + A) + ABC + A\bar{C}$

$= (A + \bar{A})(A + B) + ABC + A\bar{C}$

$= 1 \cdot (A + B) + A(BC + \bar{C})$

$= 1 \cdot (A + B) + A[(B + \bar{C})(C + \bar{C})]$

$= (A + B) + A(B + \bar{C})$

$= A + A(B + \bar{C}) + B$

$= A[1 + B + \bar{C}] + B$

$= A + B$

Simplify

(i) $Y = \bar{A}C + A\bar{C}$

$= \bar{A}C + \bar{A} + \bar{C}$

$= \bar{A}(C+1) + \bar{C}$

$Y = \bar{A} + \bar{C}$

(ii) $Y = \overline{AB + \bar{A}B + A}$

$Y = \overline{AB} \cdot \overline{\bar{A}B} \cdot \bar{A}$

$= (\bar{A} + \bar{B}) \cdot AB \cdot \bar{A}$

$= 0.$ $\quad | \bar{A} \cdot A = 0.$

(iii) $Y = \overline{(\bar{A}+C)(B+\bar{D})}$

$= \overline{(\bar{A}+C)(B+\bar{D})}$

$= \overline{(\bar{A}+C)} + \overline{(B+\bar{D})}$

$= (A \cdot \bar{C}) + \bar{B}D$

$\boxed{Y = A\bar{C} + \bar{B}D}$

Combinational Circuit

These are the circuits whose output is dependent only on the state of its inputs. The output is a pure function of the present input. Does not depends on past values.

Examples of these circuits are

Half adder

Full adder

Multiplexer

Decoder

The following example will be further discussed.

Half adder

It is a simple functional digital circuit built from two logic gates. The half adder adds two one-bit binary numbers (A and B). The output is the sum of the two bits (S) and the carry (C).

The truth table & schematic diagram is shown in figure below

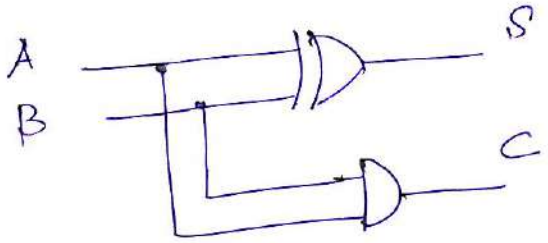
Logic symbol

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table.

$S = \bar{A}B + A\bar{B} = A \oplus B$

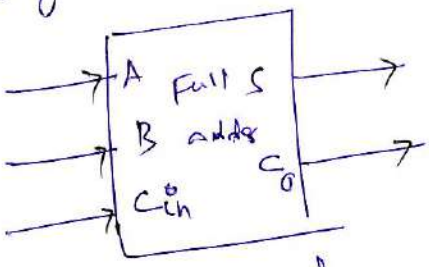
$C = AB$



Full adder

The full adder circuit adds three one-bit binary number (A, B, C), and outputs two one-bit binary numbers, a sum (S) and a Carry (C_o).

The Full adder is simply two half adder joined by an OR gate. The Logic symbol, Truth table & Circuit diagram is shown below.



Logic Symbol

A	B	C_{in}	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table: Truth Table

From Truth Table

$$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$= (\bar{A}\bar{B} + AB)C + (\bar{A}B + A\bar{B})\bar{C}$$

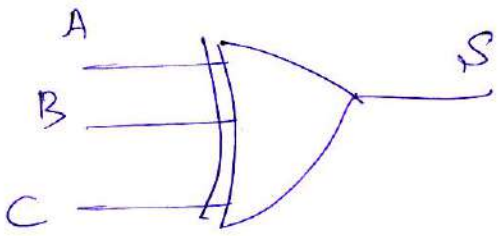
$$= (\overline{A \oplus B})C + (A \oplus B)\bar{C}$$

$$= \text{let } x = A \oplus B$$

$$= \bar{x}C + x\bar{C}$$

$$= x \oplus C$$

$$S = A \oplus B \oplus C$$



$S = A \oplus B \oplus C$

Sum using logic gates is shown in fig

$$\text{Carry} = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC + ABC + ABC$$

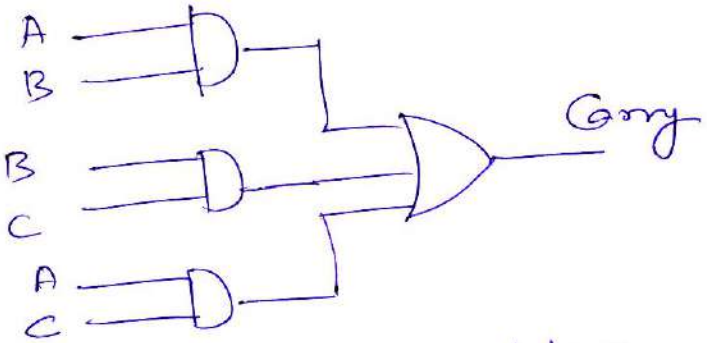
$$= \bar{A}BC + ABC + A\bar{B}C + ABC + AB\bar{C} + ABC$$

$$= (\bar{A} + A)BC + (\bar{B} + B)AC + (\bar{C} + C)AB$$

$$= BC + AC + AB$$

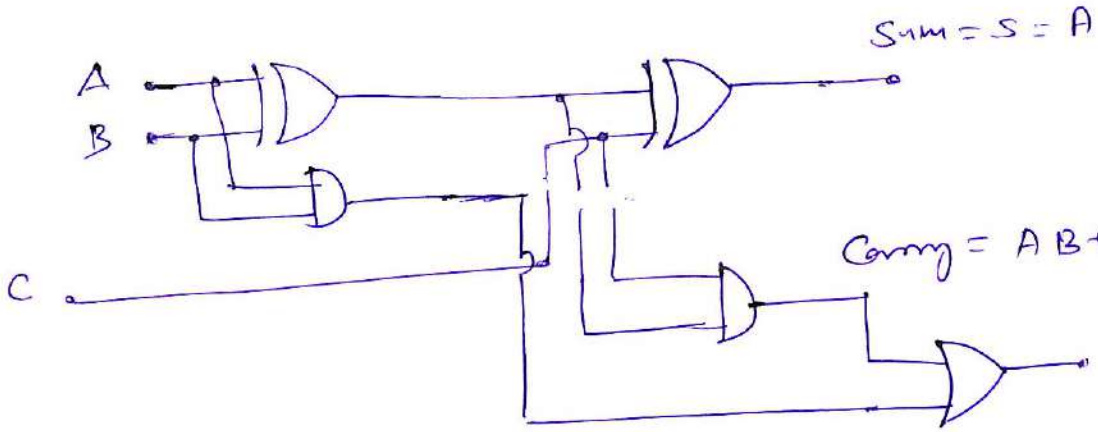
$$\text{Carry} = AB + AC + BC.$$

It can be implemented by three AND gate & one OR gates.



Carry of Full adder

Realizing Full adder using Half adder & OR gates.



$$\text{Carry} = AB + C(A \oplus B)$$

$$= AB(C + \bar{C}) + C(\bar{A}B + A\bar{B})$$

$$\text{Carry} = ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C.$$

Ripple - carry - adder

A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage.

The full adder is a component in a cascade of adders, which adds 8, 16, 32 bit etc binary numbers.

A n-bit adder can be designed by connecting the carry out and carry in lines of n-full adders. Fig shows the 4-bit adder. This adder is called ripple-carry adder. Further, four 4-bit adders can be connected to form a 16-bit adder, etc.

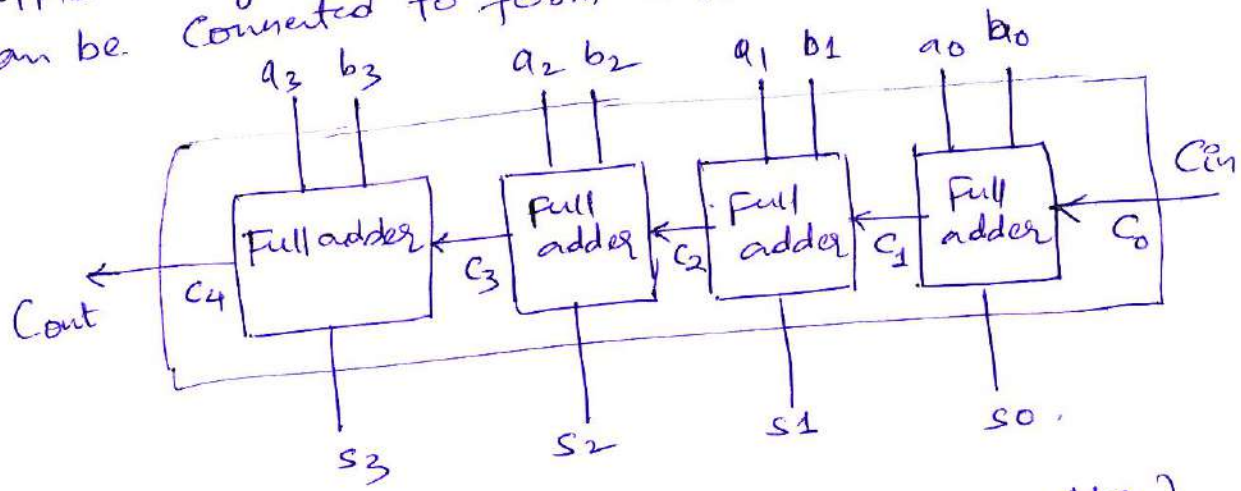


Fig: 4-bit adder (ripple carry adder)

Example ①.

$0 = C_{in}$

$1\ 1\ 1\ 1 = A$

$0\ 0\ 0\ 1 = B$

$1\ 0\ 0\ 0\ 0$

Cout $S_3\ S_2\ S_1\ S_0$

Example ②

$C_{in} = 1$

$A = 1\ 1\ 1\ 1$

$B = 1\ 1\ 1\ 1$

$1\ 1\ 1\ 1\ 1$

Cout $S_3\ S_2\ S_1\ S_0$

Multiplexers

It is a logical circuit that selects one of several analog or digital input signals and forwards the selected input into a single lines.

Multiplex means many to one. Digital multiplexers provide the digital equivalent of an analog selector switch.

A digital multiplexer connects one of '2^n' inputs to a single output line, so that the logical value of the input selected is transferred to the output with the help of select lines.

The objective of a multiplexer is to select one signal from a group of 2^n inputs, to be an output on a single output line.

Block diagram or black box representation of multiplexer (mux) is shown below in figure.

The Data lines $D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7$ are the data input lines & F is the output line. Lines A, B, and C are called the select lines.

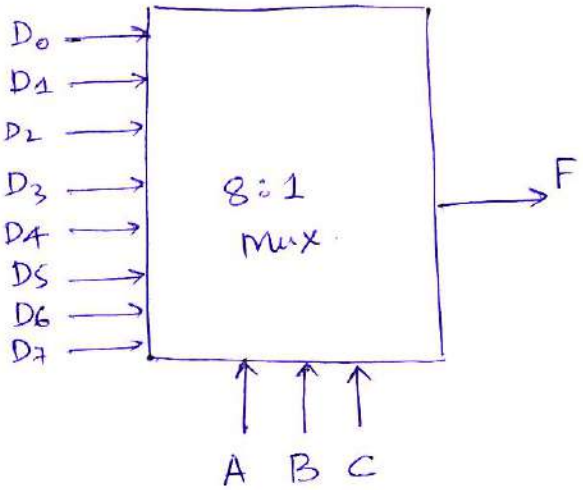
The select lines are interpreted as a three-bit binary number, which is used to choose one of the D-lines to be output on the line F.

The $2^3 = 8$ input lines selected with 3 select lines & one data line is output at one time based on select lines.

Implementation:

mux is designed with a regular pattern of AND and OR gates, as shown in figure.

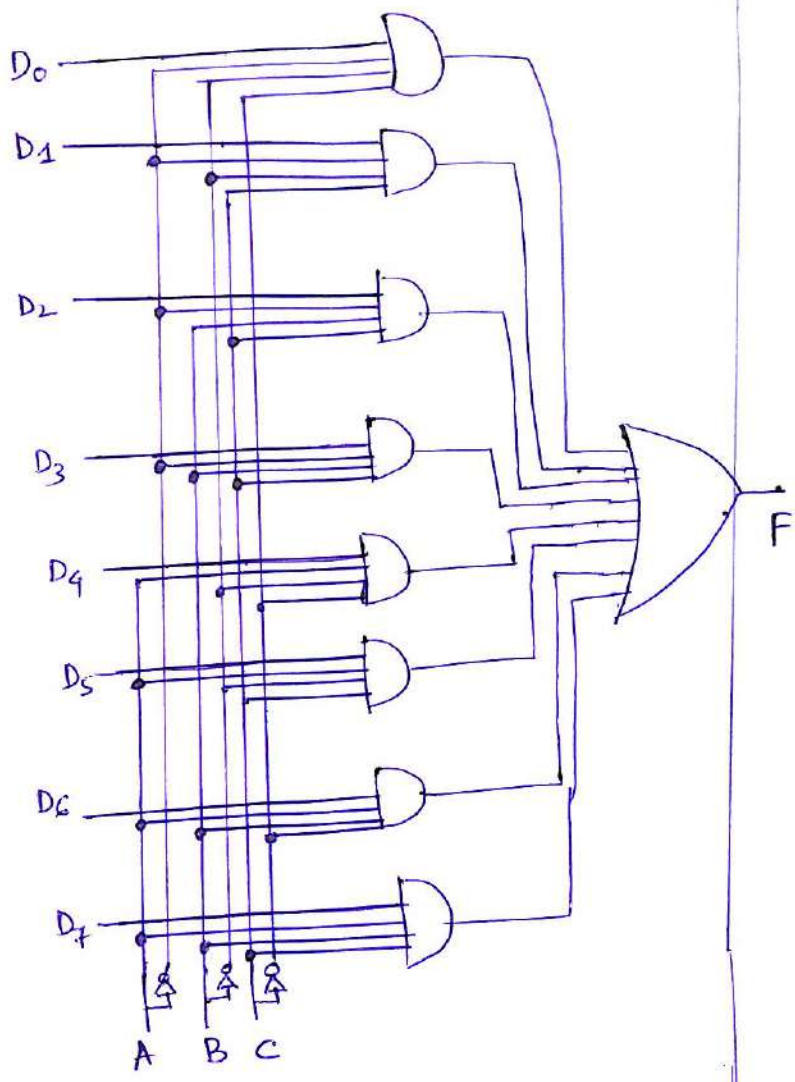
Truth table is shown below.



8-to-1 Multiplexer

select lines			output
A	B	C	F
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7.

Truth Table.



Implementation of an 8-to-1 Multiplexer.

For Example,
Suppose we want to output $Y = D_5$, then the three inputs to the corresponding AND gate should be 101. Then

if $D_5 = 0$, $F = 0$
$D_5 = 1$, $F = 1$
} $F = D_5$.

The corresponding select inputs are
$5 \rightarrow 101$ or $A\bar{B}C$

Application :-

Choose one of several registers to be used as ALU (Arithmatic Logic unit) input. A 2^n-to-1 multiplexer can be used to implement an arbitrary Boolean function of n variables, by associating each input line of the multiplexer with a row of the truth table for the function.

Decoder :-

A decoder is a multiple-input, multiple output logic circuits which converts coded inputs into coded outputs, where the input and the output codes are different. The input code has lesser bits than the output code. A binary decoder generally has n inputs and 2^n outputs. The binary decoder activates one of the 2^n outputs based on the input applied.

The objective of the decoder is to decode an n-bit binary number, producing a signal on one of 2^n output lines. Figure shows an 3-to-8 decoder.

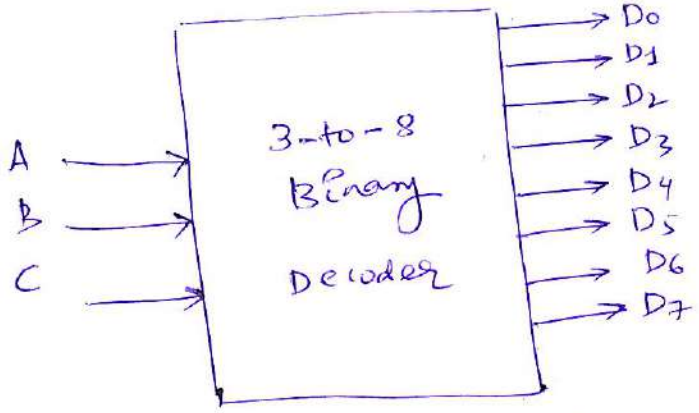


Fig: 3-to-8 decoder

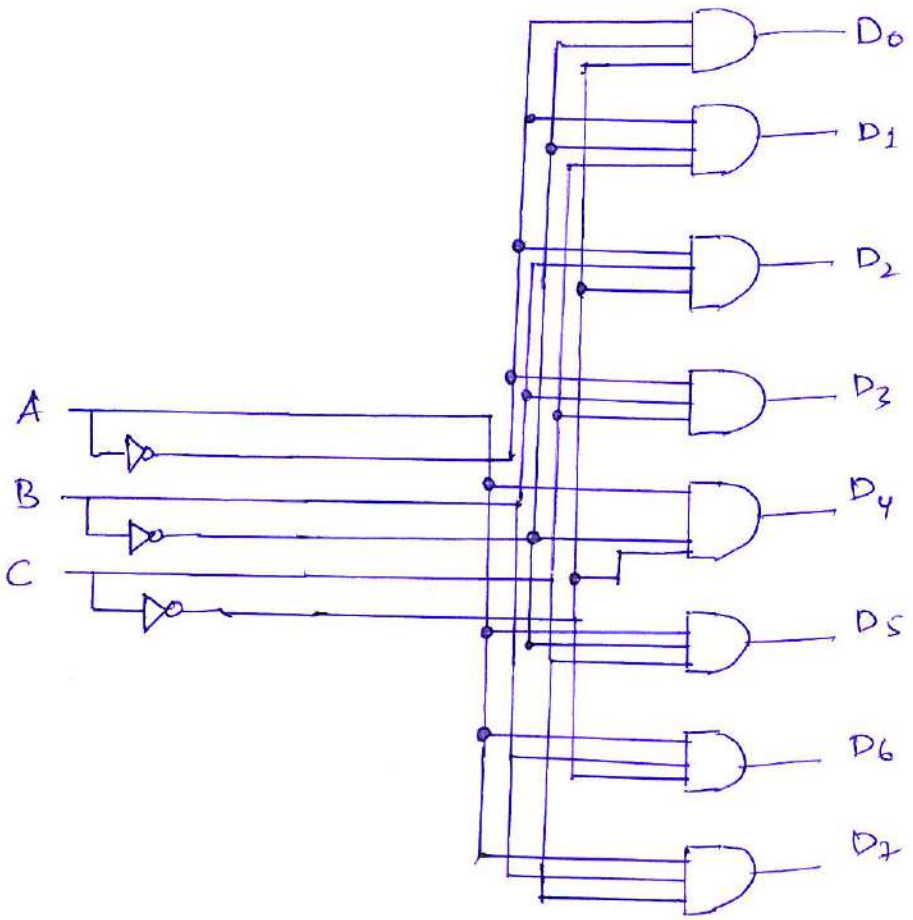
Implementation :-

A decoder is often implementated with an additional input called an "enable" line. When the line is enabled, the circuit is a decoder. When it is disabled, all the outputs are '0'.

The same circuit can be used as a de-multiplexer, which directs a single data input line to one of 2^n output lines, depending on the values of n select lines.

Figure . shows one 3-to-8 decoder implementation.

A B C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0 0 0	1	0	0	0	0	0	0	0
0 0 1	0	1	0	0	0	0	0	0
0 1 0	0	0	1	0	0	0	0	0
0 1 1	0	0	0	1	0	0	0	0
1 0 0	0	0	0	0	1	0	0	0
1 0 1	0	0	0	0	0	1	0	0
1 1 0	0	0	0	0	0	0	1	0
1 1 1	0	0	0	0	0	0	0	1



3 to 8 decoder.

SR FlipFlop / SR Latch.

The simplest memory ckt and example of Sequential ckt is SR FlipFlop / SR latch.

A FlipFlop is an electronic ckt which has memory. It is used to store one bit memory. If its output is 1/0, it remains same unless input changes on change in input, its output changes (flips) to 0/1 and then remains constant.

A FlipFlop is a basic element of all sequential system.

Operation :-

A NOR gate produces output 1 only when both inputs are 0, otherwise the output is 1.

Latch is ckt that has two stable states & can be used to store state information.

It holds one bit of data. Latches are example of sequential ckts and are memory elements.

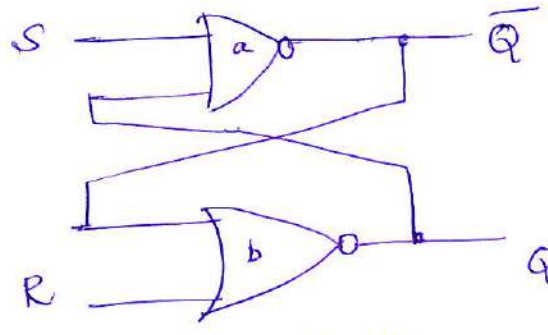
SR latch using NOR gate is explained below.

S means set state output $Q = 1$ and $\overline{Q} = 0$

R means Reset state output $Q = 0$ and $\overline{Q} = 1$.

Previous values are very important here.

Assume SR latch / Flipflop is in **set state**.



SR FlipFlop

Inputs S	Inputs R	present state Q_n	next state Q_{n+1}	
0	0	0	0	} No change
0	0	1	1	
0	1	0	0	} reset
0	1	1	0	
1	0	0	1	} set
1	0	1	1	
1	1		Not allowed	

Case ① . Let SR FF be in set state, we make S=0 and R=0. The input to 'a' NOR are (0,1); So $\bar{Q}=0$, & inputs to 'b' NOR (0,0); SO Q=1. Therefore SR FlipFlop remains in set state i.e no State change.

It similarly shows that when the SR FF in reset state we make S=0, R=0 it remains in reset hence this state is called No change & inputs are S=0, R=0.

Case ②.

If output is in set state (Q=1, $\bar{Q}=0$.) we input S=0, R=1, gate b conduct first (1,0) results in Q=0. hence the output changes from set to reset state. But If the output was in reset state (Q=0, $\bar{Q}=1$) and S=0, R=1, gate 'b' conducts first produces the output Q=0. hence the result is for S=0, R=1. Q=0 hence this state is called Reset state

Case ③.

If the output is in Reset state (Q=0, $\bar{Q}=1$) & S=1, R=0, then gate 'a' conducts first & produces output $\bar{Q}=0$ later gate 'b' produces output Q=1. hence For S=1, R=0, the value of Q=1 (set). if the output is in set state, (Q=1, $\bar{Q}=0$) & S=1 and R=0, then also the output Q=1, $\bar{Q}=0$. hence this state output is called as set state.

Case ④

Both S=1 and R=1 are not permitted as this would cause a conflict, & outcome would be uncertain.

The above operations of SR Flipflop are given in table.

Clocked SR Flip Flop.

Within a digital Computer, a clock is used to synchronise changes in the contents of memory elements. A clock is a signal which oscillates between 0 and 1 as shown in figure.

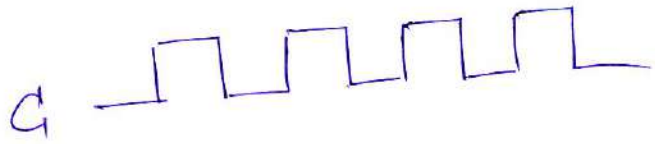


Fig: clock signal.

The clock can be applied to a latch so that change in the latch's value can only occur when the clock is in the '1' (high) state.

The clocked SR latch/FF is shown below.

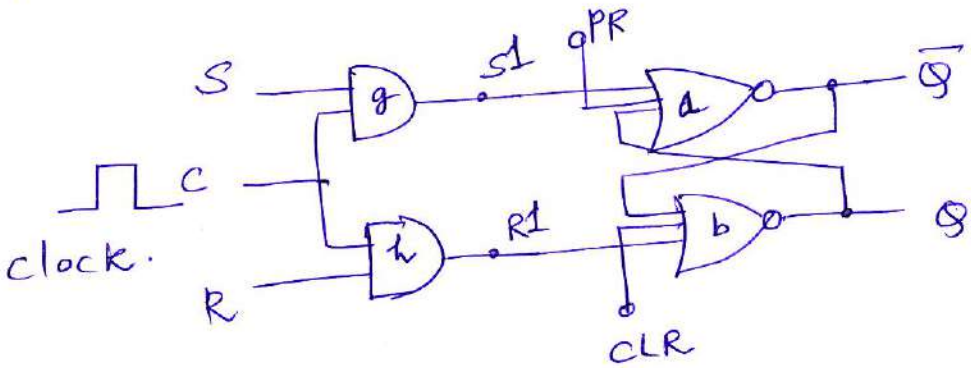


Fig. Clocked SR Flip Flop

When C = 0, the output of both AND gate g and h are zero. So Q cannot change. The latch is non-operational.

When C = 1, output of gate g is 1 then S1 = S & output of gate h is 1. R1 = R, the latch is now operational. The operational procedure is same as discussed in previous section.

The term Level triggered is applied to latches to indicate that its ability to change value depends on the level (low or high) of the clock signal.

The term edge triggered is used with clocked Flip Flop we have positive edge triggering and Negate edge triggering also.

positive edge triggering  The state change from Zero to One ie Low to high.

Negative edge triggering  The output changes when the a clock signal change from high to low.

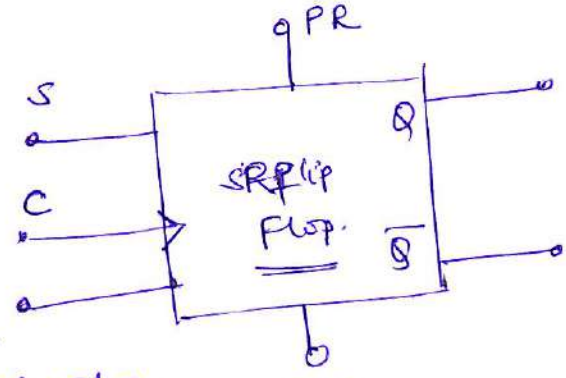
preset and clear:

In figure one additional input is provided to each NOR gate; CLR on Q side NOR and PR on $\bar{Q}$ side NOR. When CLR = 0, PR = 0, the circuit behaves as an SR Flipflop. The block representation is shown below.

In absence of a clock pulse (C=0). the output input to NOR gates are zero. making CLR = 1 & PR = 0. results in Q = 0. $\bar{Q}$ = 1 these by clearing the Flip Flop.

for PR = 1 and CLR = 0, the FF produces Q = 1. $\bar{Q}$ = 0. these by presetting the Flipflop.

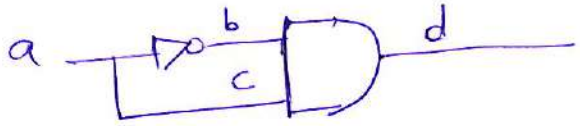
These are asynchronous inputs as this action does not need a clock pulse.



symbol of SR Flip Flop.

FlipFlops.

FlipFlop are used for more precise synchronization. They are edge-triggered. That means they can change with change in the value of the clock signals; that is on its rising or falling edge. This is done by the use of a small circuit, called a pulse generator, as shown in below figure.



pulse generator (edge triggering).

When a is connected to a clock signal, a short pulse will be generated on d, whenever a makes a transition from 0 to 1 and 1 to 0.

There are four commonly used flip-flop.

D-FlipFlop
T-FlipFlop
Rs FlipFlop and
JK FlipFlop.

The behaviour of each of them can be described by a state table. The state table shows one how the values of the FlipFlop changes in response to its inputs.

State table of SR FlipFlop / RS FlipFlop.

Rs (Reset-Set)		
R	S	Qnext
0	0	Q
0	1	1
1	0	0
1	1	undefined

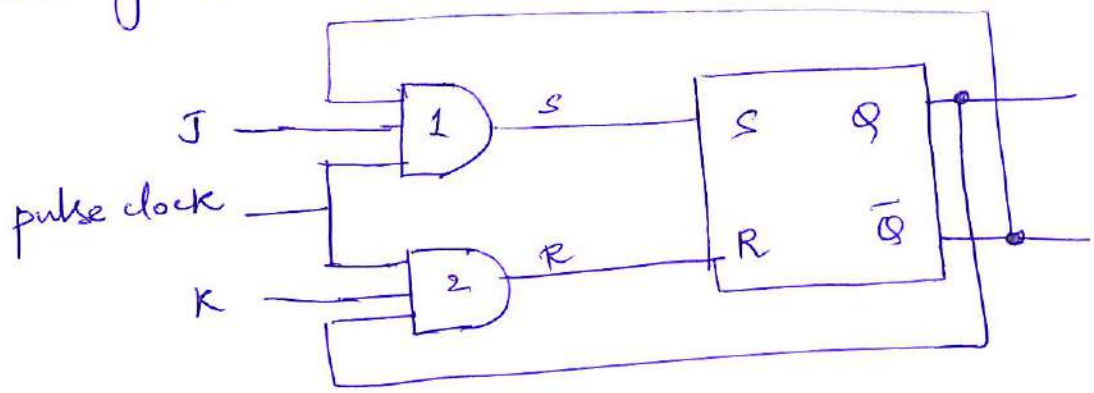
D (Data)	
D	Qnext
0	0
1	1

T (Toggle)	
T	Qnext
0	Q
1	$\overline{Q}$ (Toggle)

JK FlipFlop		
J	K	Qnext
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

JK FlipFlop.

The undefined state of SR FlipFlop is overcome by converting SR FlipFlop to JK FlipFlop by feeding $\overline{Q}$ to the upper AND & Q to lower AND gate.



JK FlipFlop.

The SR FlipFlop determines the output of JK FlipFlop. The values of S, R are governed by the input J, K and Q.

The outputs for various combinations of inputs (J, K). When a clock pulse is applied is explained.

clock pulse may be positive edge Triggered [PT] or Negative edge triggered).

(i)
(a) when J=0, K=0, Q=0 & $\bar{Q}$=1

Then S=0, R=0 produced by two AND gates, these are inputs to SRFlipflop. The output of SRFF is.

Q_{next}=0, $\bar{Q}_{next}$=1. hence this state is No change.

(b) when J=0, K=0, Q=1. & $\bar{Q}$=0

Here also S=0, R=0 ⇒ Q_{next} = 1, $\bar{Q}_{next}$ = 0, No change

(ii) (a) when J=0, K=1, Q=0 and $\bar{Q}$=1

First AND gate produces S=0. and second AND gate also produces R=0. hence Q_{next}=0, $\bar{Q}_{next}$=1. (No change)

(b) when J=0, K=1 Q=1 and $\bar{Q}$=0.

AND gate 1 produces S=0,
AND gate 2 produces R=1
when S=0, R=1 Then Q_{next} changes to 0 & $\bar{Q}_{next}$ = 1
hence this state is called Reset state.

(iii) (a) when J=1, K=0. Q=0 and $\bar{Q}$=1

First AND gate produces S=1 and AND gate 2 produces R=0, then the output of SR latch Q_{next}=1 (set state) and $\bar{Q}_{next}$=0.

(b) when J=1, K=0, Q=1 and $\bar{Q}$=0

AND gates produces S=0, R=0. hence this state is Nochange because SR latch produces output as Q_{next}=1, & $\bar{Q}_{next}$=0.

all these are shown in table.

Now consider (1,1) = (J,K) inputs which were entries not permitted in an SR-FlipFlop.

(IV)

(a) J=1, K=1, Q=0 ⇒ S=1, R=0, Q_{next} = 1, $\overline{Q}$. Set state

(b) J=1, K=1, Q=1 ⇒ S=0, R=1 Q_{next} = 0, $\overline{Q}$. reset state

This state is called Toggle state because the output toggles ie the state changes from 0 to 1, or 1 to 0.

JK master slave FlipFlop

The toggle state of JK FlipFlop causes the problem. If any clock pulse is too long, the output state will change more than once and the final state of the FlipFlop will be indeterminate. To avoid this problem, a JKFF is constructed with two SR FlipFlops in master slave connection as shown in figure.

In JKFF output is feedback to the input, therefore any changes in the output results in corresponding changes in the input due to this in the positive half of the clock pulse when J & K are both high (1) the output toggles continuously. This condition is known as race around condition.

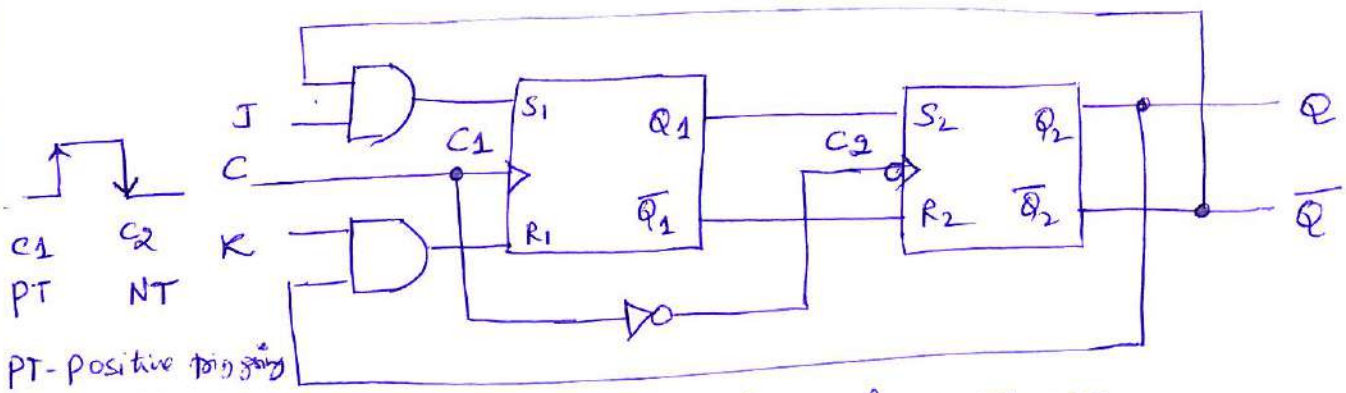


Fig: JK master slave FlipFlop.

Operation of JK masler slave flip flop

In masler slave JKFF : By virtue of masler to slave connection, $S_2 = Q_1$, $R_2 = \overline{Q_1}$.
It means that input to the slave is always 0/1 or 1/0.
∴ As pulse C goes low, $C_2 = 1$ and slave transfers the output of the masler to the system output $Q_1 = Q_2 = Q_1$.

Consider when $J=1, K=0$ and $Q=0$. Then
$S_1 = 1, R_1 = 0$ when clock pulse $C_1 = C = 1$ then
$Q_1 = 1$ (set) $= S_2$. Its connected to slave at negative triggering i.e $C=0, C_2 = 1$ the output $Q_2 = Q = 1$ (set).

(i)
$J=1\ K=0, Q=0 \Rightarrow S_1=1, R_1=0 \xrightarrow{C=C_1=1} Q_1 = 1 = S_2 \xrightarrow{C=0, C_2=1} Q_2 = Q = 1$
$J=1\ K=0, Q=1 \Rightarrow S_1=0, R_1=0 \xrightarrow{C=C_1=1} Q_1 = 1 = S_2 \xrightarrow{C=0, C_2=1} Q_2 = Q = 1$

(ii)
$J=0, K=0$, $Q=0$.
masler & slave Flipflop remains in previous state have this state is called Nochange state

Set

Nochange

(iii)
$J=0, K=1, Q=1 \Rightarrow S_1=0, R_1=1 \xrightarrow{C=C_1=1} Q_1=0 \Rightarrow S_2 \xrightarrow{C=0=C_2=1} Q_2 = Q = 0.$
$J=0, K=1\ Q=0 \Rightarrow S_1=0, R_1=0 \Rightarrow Q_1=0 \Rightarrow S_2 \xrightarrow{C=0=C_2=1} Q_2 = Q = 0.$
This state is called Reset state.

Reset state

(iv). For $J=1, K=1$ toggling should happen at output without any indeterminate solution.

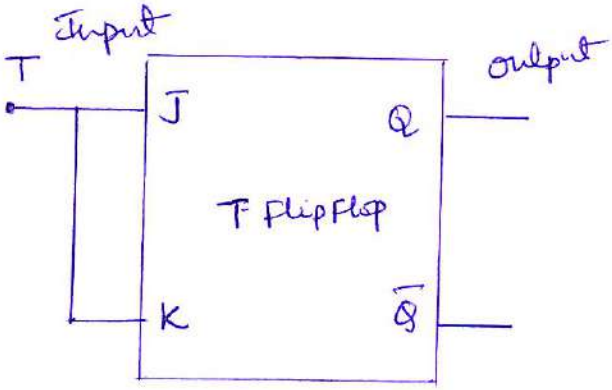
$J=1, K=1, Q=1 \Rightarrow S_1=0, R_1=1 \xrightarrow{C=C_1=1} Q_1=0 \Rightarrow S_2=0, R_2=1 \xrightarrow[C_2=1]{C=0} Q=0=\overline{Q}$
$J=1, K=1, Q=0 \Rightarrow S_1=1, R_1=0 \xrightarrow{C=C_1=1} Q_1=1 \Rightarrow S_2=1, R_2=0 \xrightarrow[C_2=1]{C=0} Q=1=\overline{Q}$

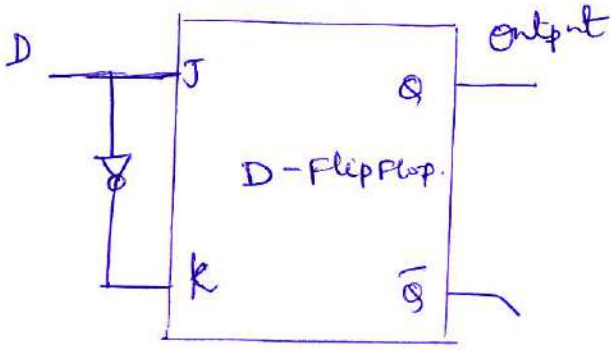
Thus confirms the toggle operation of the the JK masler-slave Flip-flop. The masler FF operates when $C=1$ & slave operates when $C=0$. when slave operates masler is inoperative and unwanted toggling cannot occur. hence JK masler slave avoids race-around condition of JK Flipflop.

The sequential action of slave (after master has become inoperative) and C goes low, the JK master-slave FF is also called as trailing edge triggered Flip Flop.

T-(Toggle) Flip Flop

In this Flip Flop J and K inputs are tied together. when T=0 with the application of the clock pulse the output Q remains in the same state. When T=1 output toggles from 0 to 1 or 1 to 0 state with every clock pulse.





D-(Data) Flip Flop

D Flip Flop also called Data flip-flop has one input D. with the application of each clock pulse the data (0 or 1) is transferred to the output Q. The modified JK FF as D FF is shown above. also Refer Truth Table on previous pages.

Shift register

The shift register is a sequential circuit that can be used for the storage or the transfer of binary data.

shift register is digital circuit constituted by cascade of flipFlops, sharing the same clock, in which the output of each FlipFlop is connected to the data input of the next flip-Flop in the chain, results in shifts of data.

In Figure. shift register consists of two RS FlipFlops when a clock pulse occurs, the value of the left FlipFlop is copied to the right FlipFlop. This is known as a shift register.

FlipFlops are used within a CPU (central processing unit) to implement register. A register is an ordered group of n-FlipFlops.

For Example, in the Intel architecture, EAX is a 32-bit register. It can hold a 32-bit binary register.

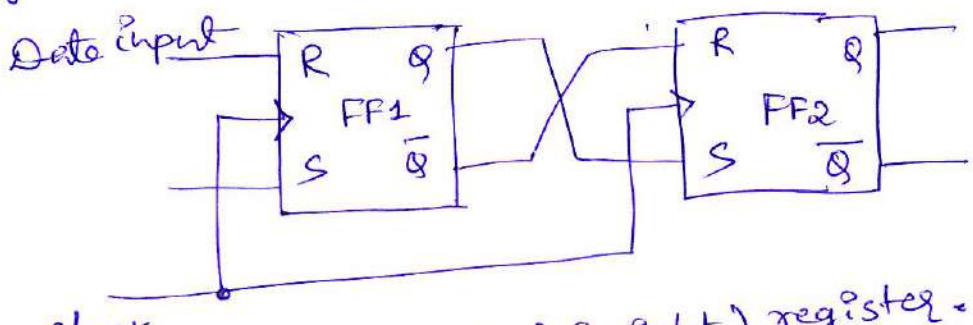


Fig. shift (right) register.

Simple shift register, the date string presented at Data in & is shifted right one stage each time. The bit from FF1 is shifted into FF2 input and upon clock pulse shifted at output of FF2.

The binary information in a register can be moved from stage to stage within the register or into or out of register upon application of clock pulses.

This type of movement or shifting is essential for certain arithmetic and logic operations used in processors. Shift register applications involves storage and transfer of data in a digital system.

Figure shows a four bit shift register employing D as flipflops, which trailing edge triggered indicated by a small circle at the back of the clock triangle.

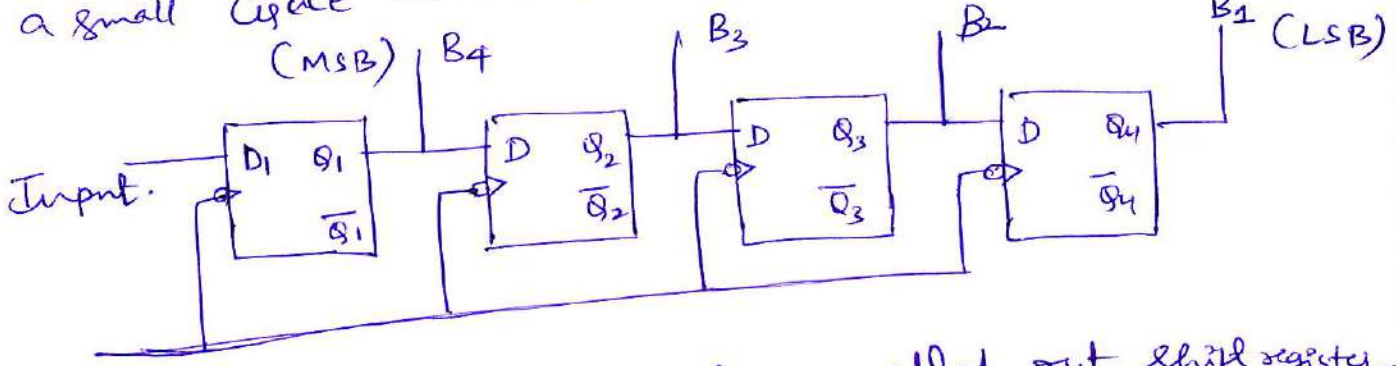


Figure: Serial input - parallel out shift register

Let the input sequence be $A_4 A_3 A_2 A_1$ and initial state of the register be $Q_1 = Q_2 = Q_3 = Q_4 = 0$.

Before applying clock pulse, the four data (D) bits are.

$D_1 = A_1, D_2 = Q_1 = 0$, $D_3 = Q_2 = 0$. and $D_4 = Q_3 = 0$.

After the first pulse arrives, data (D) in all the FlipFlop shifts to Qs and the state of register read from left to right becomes A1,000. After the second pulse, the state of the register becomes $A_2, A_1 00$ and finally at the end of Fourth pulse it is $A_4 A_3, A_2, A_1$. The register state can be read simultaneously at $B_4, B_3 B_2 B_1$. This is called Serial-in parallel-out shift register. After four more clock pulses, the output can be read serially at B1.

The fourth Table is shown below.

Serial I/p Data	shift pulse	Q_1	Q_2	Q_3	Q_4
–	–	x	x	x	x
0	T1	0	x	x	x
1	T2	1	0	x	x
0	T3	0	1	0	x
1	T4	1	0	1	0
0	T5	x	1	0	1
x	T6	x	x	1	0
x	T7	x	x	x	1
x	T8	x	x	x	x
x					

Binary Counter :-

A Counter is a sequential circuit that counts the number of input pulses.

A Counter that counts in terms of binary is called a binary Counter. The count output of n-bit binary Counter is 2^n states.

Therefore, it can count from 0 to $(2^n - 1)$. The number of states of Counter is called as it modulus (m).

For n-bit Counter, $m \leq 2^n$.

Based on the concept of applying inputs to FF to start Counting we have two types of Counter.

- Asynchronous Counter
- Synchronous Counter.

In Asynchronous Counter, the FF are clocked sequentially while in a Synchronous Counter, they are clocked simultaneously.

In Asynchronous Counter, time delay of each FF get added & this Count action is slower than in Synchronous Counter.

Asynchronous Counters (ripple Counters)

T FlipFlops are used in these counters. A 3 bit binary ripple counter is shown in figure below.

The small circles at the back of the clock input stand for the fact that these FF are triggered by trailing edge of the input pulse (1 going 0).

For Toggling, all T inputs are kept high (1).

From left to right, the first T-FlipFlop receives pulses from the counter. The other two receive pulses from the output of the preceding T-FlipFlop.

The pulses kind of ripple through & hence, the name ripple counter. 3-bit ripple counter is presented in table. At 8th pulses, the counter resets to 0.

The Timing diagram of the counter is shown below in figure. It is observed that pulse frequency gets divided by 2 at each stage.

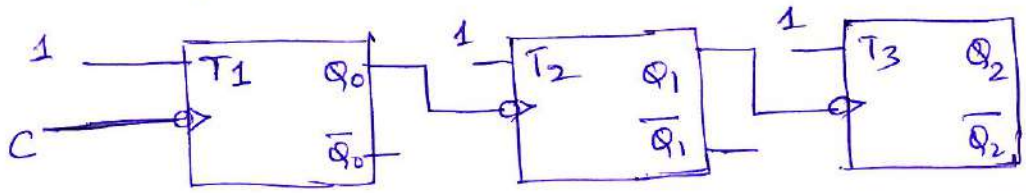


Fig:- 3 bit (modulo 8) ripple counter.

Truth table of 3-bit ripple Counter

Q_2	Q_1	Q_0	Input pulse Count.
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	8

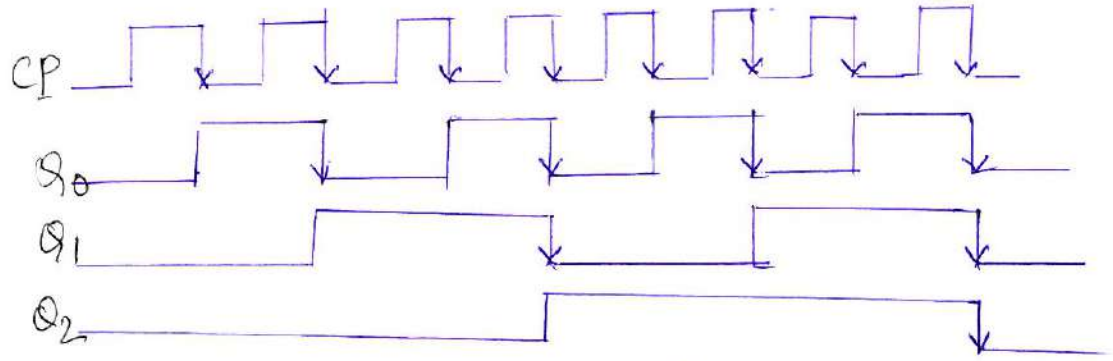
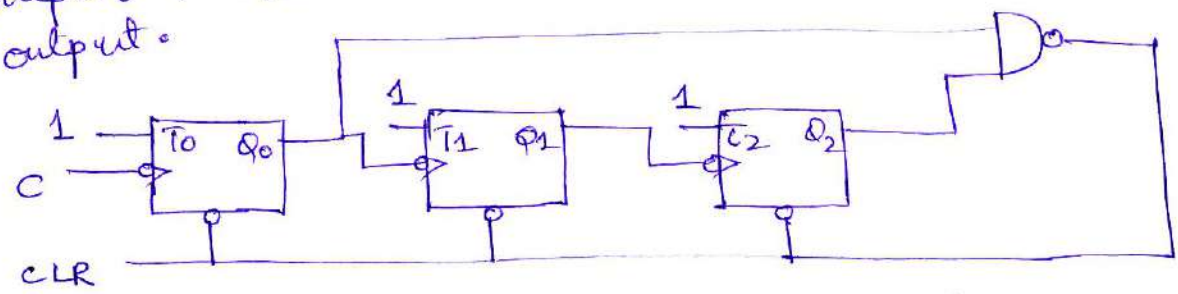


Fig. Timing diagram of 3-bit ripple counter.

Modulo-5 ripple Counter

It is possible to design modulo-5 ripple counter. As $2^3 = 8 > 5$ we need 3 T-FlipFlops. The counter circuit is shown in figure. where the CLR (clear) terminals are also shown. As the pulse count reaches $5 \rightarrow 101$. The counter must reset to zero (000). As outer 1's combination is unique to count 5, these are fed to a NAND gate, which produces 0 output to clear the three FlipFlops & produces 000 as output.



modulo-5 ripple counter.

C	Q_2	Q_1	Q_0
↓	0	0	0
↓	0	0	1
↓	0	1	0
↓	0	1	1
↓	1	0	0
↓	0	0	0

Synchronous Counter

In an asynchronous counter, as the pulse ripples through all the flipflops, the time delay adds up.

In synchronous counter, the clock pulse is applied to all the flip-flop simultaneously and so the time delay is that of one counter. Counters are fast in opelation.

For modulo -16 Synchronous Counter, Four Flip-Flop are needed. Constonted by using T-FlipFlop.

The Truth table for 4-bit Synchronous Counter is shown below.

Truth Table.

Input clock.	Q_3	Q_2	Q_1	Q_0	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1	1
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	1	1	1
4	0	1	0	0	0	0	0	1
5	0	1	0	1	0	0	1	1
6	0	1	1	0	0	0	0	1
7	0	1	1	1	1	1	1	1
8	1	0	0	0	0	0	0	1
9	1	0	0	1	0	0	1	1
10	1	0	1	0	0	0	0	1
11	1	0	1	1	0	1	1	1
12	1	1	0	0	0	0	0	1
13	1	1	0	1	0	0	1	1
14	1	1	1	0	0	0	0	1
15	1	1	1	1	1	1	1	1
0	0	0	0	0				

From Table we find that

Q_0 continuously toggles, therefore $T_0 = 1$

Q_1 toggles when $Q_0 = 1$, therefore $T_1 = Q_0$

Q_2 toggles when $Q_0 = Q_1 = 1$ therefore $T_2 = Q_1 Q_0$

Q_3 toggles when $Q_0 = Q_1 = Q_2 = 1$ therefore $T_3 = Q_2 Q_1 Q_0$

The corresponding $T = 1$ are indicated in the same table. To generate T_2 & T_3, two AND gates are needed. To meet these requirements, the circuit diagram of the synchronous counter is drawn in figure.

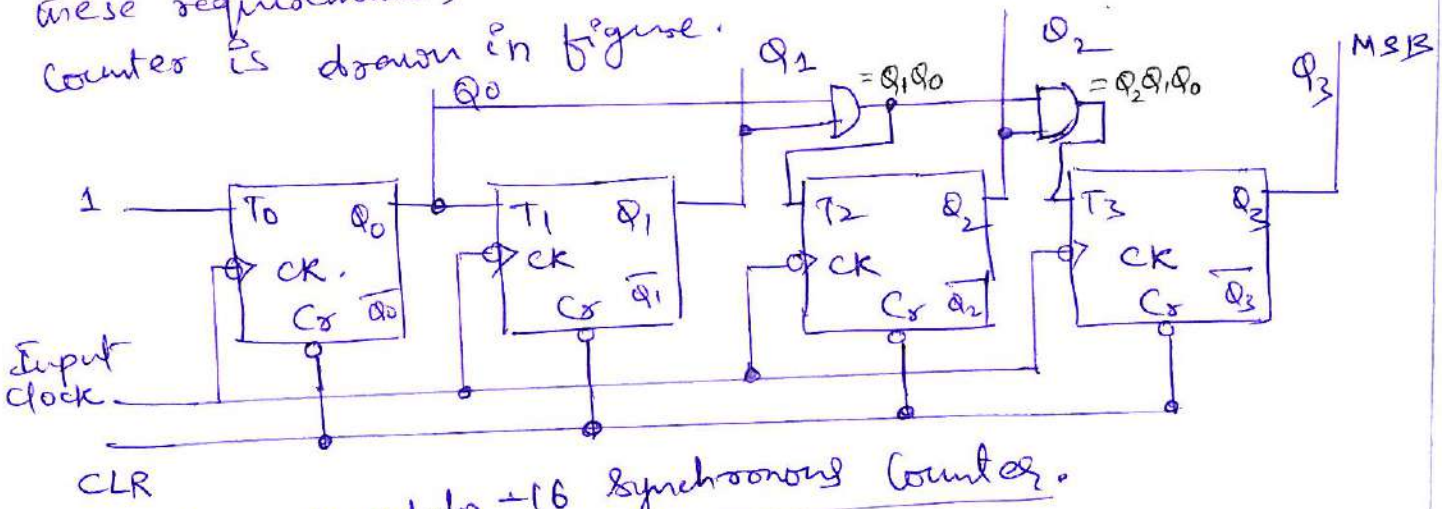


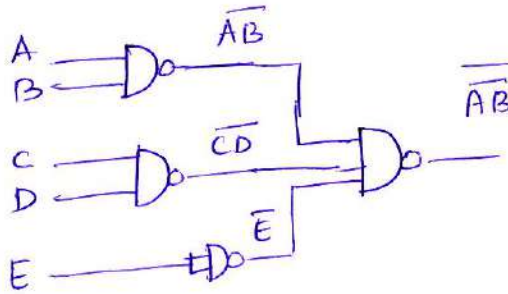
Fig. Modulo -16 Synchronous Counter.

(1) Consider the Boolean expression $Y = AB + CD + E$ Implement it using NAND gates.

$$Y = AB + CD + E$$

$$\overline{Y} = \overline{AB + CD + E}$$

$$= \overline{\overline{AB} \cdot \overline{CD} \cdot \overline{E}}$$



(2) Realise the following logic function using NAND gates only

$$Y = \overline{AB + \overline{A}\,\overline{B} + \overline{A}B}$$

$$\overline{Y} = \overline{AB + \overline{A}\,\overline{B} + \overline{A}B}$$

$$= \overline{\overline{AB + \overline{A}\,\overline{B} + \overline{A}B}}$$

$$= \overline{\overline{(AB + \overline{A}\,\overline{B})} \cdot \overline{\overline{A} \cdot B}}$$

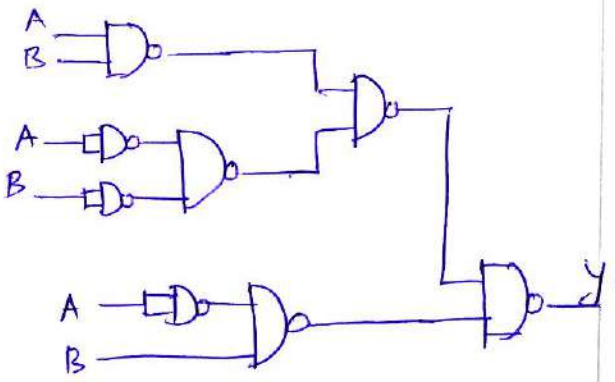
$$= \overline{(AB + \overline{A}\,\overline{B}) \cdot \overline{\overline{A} \cdot B}}$$

$$= \overline{(AB + \overline{A}\,\overline{B})} + \overline{\overline{\overline{A} \cdot B}}$$

$$y = \overline{\overline{AB} \cdot \overline{\overline{A}\,\overline{B}}} + \overline{\overline{A}B}$$

$$\overline{y} = \overline{\overline{AB} \cdot \overline{\overline{A}\,\overline{B}} + \overline{A}B}$$

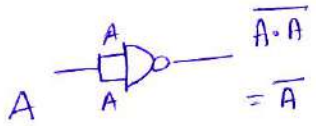
$$y = \overline{\overline{\overline{AB} \cdot \overline{\overline{A}\,\overline{B}} \cdot \overline{\overline{A}B}}}$$



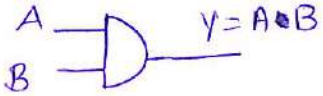
Realize Basic gate using NAND gate

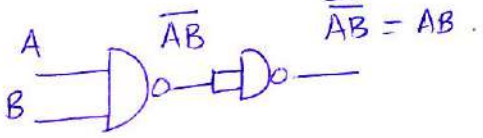
NOT gate

only NAND realization

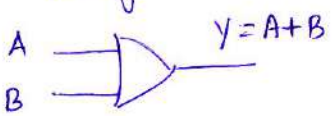


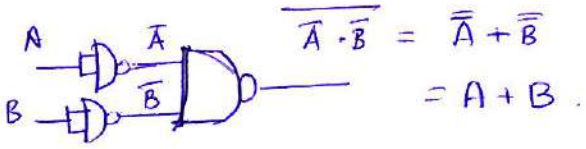
AND gate





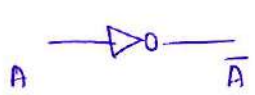
OR gate



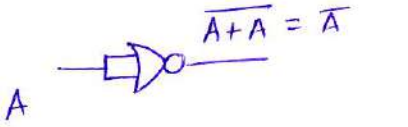


Realize Basic gate using NOR gate

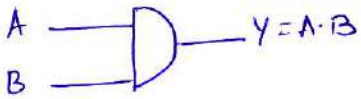
NOT gate

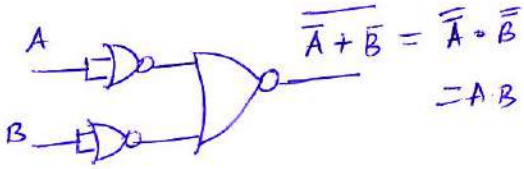


only NOR realization

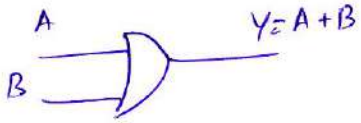


AND gate

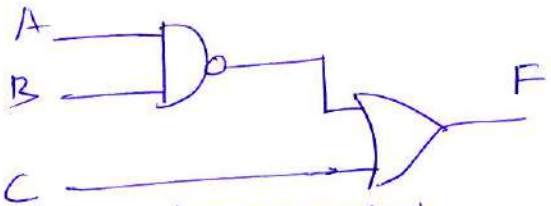




OR gate.



Write the truth table for the given circuit



Inputs A B C	output $\overline{A}B$	output $\overline{A}B + C = F$
0 0 0	1	1
0 0 1	1	1
0 1 0	1	1
0 1 1	1	1
1 0 0	1	1
1 0 1	1	1
1 1 0	0	0
1 1 1	0	1

Simplify the Boolean equation & then draw its logic circuit with appropriate gates.

$$Y = (\overline{A} + B + C)(A + B + \overline{C})$$

$$= \overset{0}{\cancel{A\overline{A}}} + AB + AC + \overline{A}B + B \cdot B + BC + \overline{A}\,\overline{C} + B\overline{C} + \overset{0}{\cancel{C\overline{C}}}$$

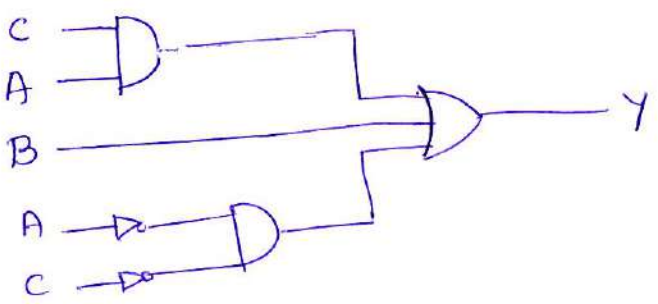
$$= AB + AC + \overline{A}B + B + BC + \overline{A}\,\overline{C} + B\overline{C}$$

$$= B + AB + \overline{A}B + BC + B\overline{C} + AC + \overline{A}\,\overline{C}$$

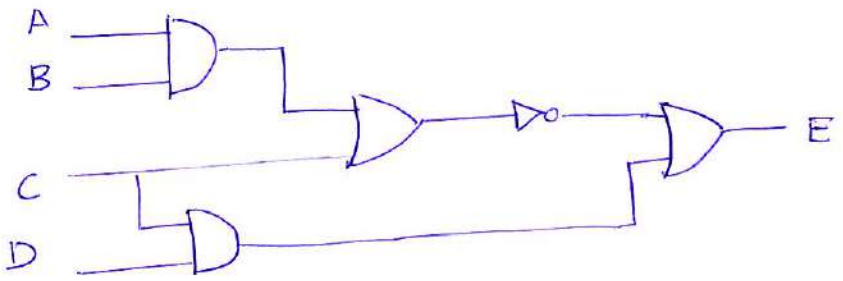
$$= B(1 + A + \overline{A} + C + \overline{C}) + AC + \overline{A}\,\overline{C}$$

$$= B \cdot 1 + AC + \overline{A}\,\overline{C}$$

$$= B + AC + \overline{A}\,\overline{C}$$

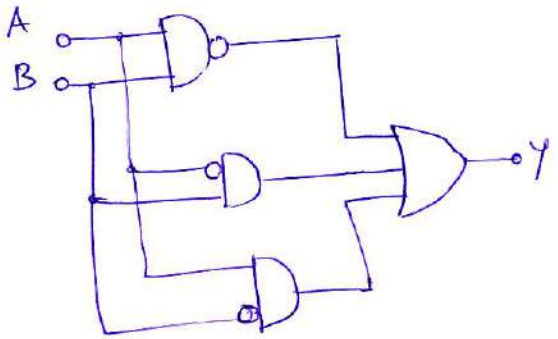


19. Write the Boolean expression for the given circuit in Fig. E = ?



$$E = (\overline{AB+C}) + CD$$

For the Logic circuit of Fig 10.32 write the Boolean expression for y in simple form



$$Y = \overline{AB} + \bar{A}\cdot B + A\bar{B}$$

$$= \bar{A} + \bar{B} + \bar{A}B + A\bar{B}$$

$$= \bar{A}(1+B) + \bar{B}(1+A)$$

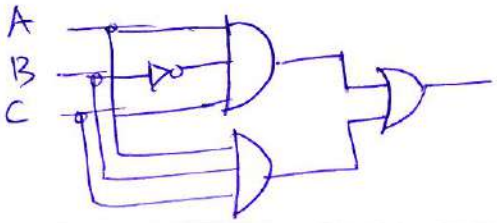
$$= \bar{A} + \bar{B}$$

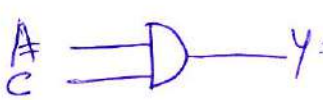
$$\boxed{Y = \overline{A\cdot B}}$$

Draw the Logic circuit for $Y = A\bar{B}C + ABC$ & then Simplify and draw the Simplified circuit

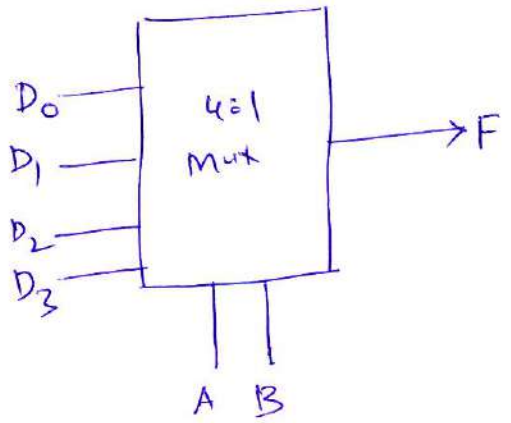
$$Y = A\bar{B}C + ABC$$

$$Y = AC(\bar{B}+B) = AC$$

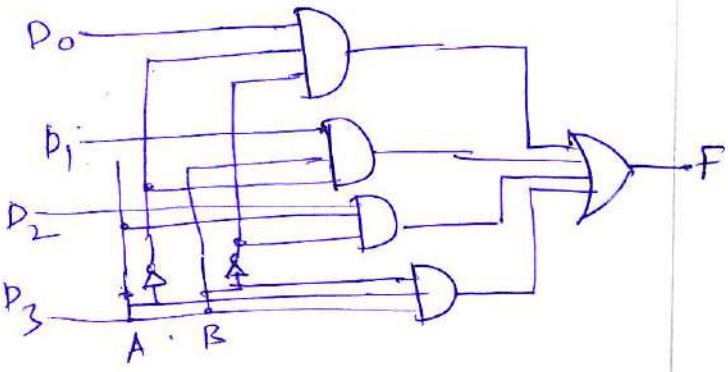




Implement the 4:1 multiplexer using basic gates.



4:1 multiplexer



Implementation of an 4:1 mux

6. Subtract the following into Decimal numbers in 8 bit 2's Complement form.

$+45 - 56$

$(1100001)_2 - (1111000)_2$

$m - n$

$m = (00110001)_2$

$n = (00111000)_2$

2's complement of n $\Rightarrow$ 1's n = 11000111

n = 00111000

$$\begin{array}{r} 11000111 \\ \quad\quad\quad 1 \\ \hline 11001000 \end{array}$$

$$\begin{array}{r} M = 00110001 \\ 2's\ n = 11001000 \\ \hline 11111001 \end{array}$$

$\rightarrow$ No Carry, result is negative.

$$\begin{array}{r} 00000110 \\ \quad\quad\quad 1 \\ \hline -(0000111)_2 \end{array} \quad (-7)_{10}$$

2 | 45
2 | 24 - 1
2 | 12 - 0
2 | 6 - 0
2 | 3 - 0
1 - 1

2 | 56
2 | 28 - 0
2 | 14 - 0
2 | 7 - 0
2 | 3 - 1
1 - 1

perform the indicated operations in binary.

(a) $\Rightarrow (32)_8 + (73)_8$

$32 = 011\ 010$

$\quad\ 111\ 011$

$1010\ 101$

$(125)_8$.

(b) $(175)_8 - (114)_8$

$175 = 001\ 111\ 101$

$114 = 001\ 001\ 100$

000110001

$(061)_8$.

(c) $(7E)_{16} + (AD)_{16}$

$\quad\ 11111$

$(7E)_{16} = 0111\ 1110$

$(AD)_{16} = 1010\ 1101$

100101011

$(12B)_{16}$

(d) $(BC)_{16} - (84)_{16}$

$(BC)_{16} = 1011\ 1100$

$(84)_{16} = 1000\ 0100$

$0011\ 1000$

$(38)_{16}$

Basic Communication System.

communication is application of Electrical Technology. we use satellite television, fax machine cellular phone etc. Communication systems include the generation, storage and transmission of information. The basic elements of Communication system are trasmitter, receiver and Communication channels.

Elements of Communication system

Communication systems are used to transfer information from a generation point to the place where it is needed/ processed.

- The information at the generation point is not in the form that can travel long distance through the channel. we use a device called modulator cum transmitter to modulate data for transmission.
- In the receiving end, the information must undergo the reverse process such as demodulation/decoding.
- The main elements are.

1. Source
2. Input transducer
3. modulator and transmitter
4. Communication channel
5. Demodulator and receiver
6. output transducer.
7. Destination.

The source is mostly analog & sometimes it may be digital. Fig① shows basic elements of a Communication Syslem

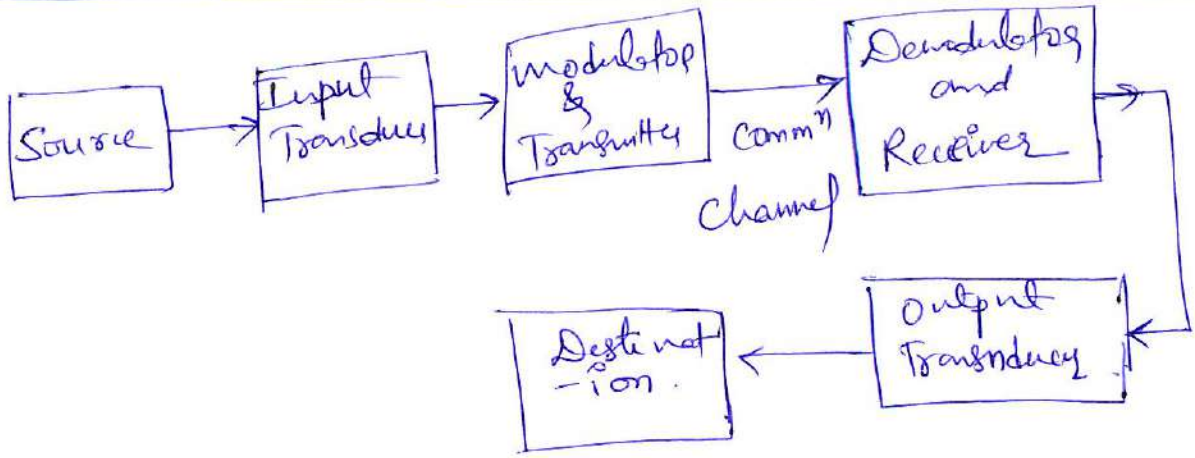


Figure ① : Communication System.

Source is the information we are sending the example of sources are analog audio, video, signals from measuring devices in the field, & Digital data.

Audio signal → range 20Hz to 20kHz.
Video signal → range from dc to 4.2MHz. Binary signal 1's & 0's.
Input transducer converts one form of signal into another. audio signal is converted to electrical signal using Mic or microphone.

Communication channel can be a pair of conductors, optical fiber or just free space.
The signal can be directly sent through a twisted pair telephone cable. But the radio link through free space cannot be used directly for audio signals; Instead an antenna of great height would be required.
A high frequency carrier signal is used to carry the message signal after performing modulation. At the receiver the information can be demodulated. The message is called modulating signal.
The output transducer converts Electrical signal back to audio signal (original message) Example is Speaker.

Principle of operation of Mobile phone

Most Commonly used device in Communication is a mobile phone. It is also called as Cellular phone.

A Cellular/mobile system provides standard telephone operation by full duplex (two way radio at remote locations.

It provides a wireless connection to the public switched telephone network (PSTN) from any user location within the radio range of the system.

The main purpose of the Cellular/mobile system is that it divides the entire geographical area into many small areas called Cells and they will be served by transmitter and receiver as shown in figure (1).

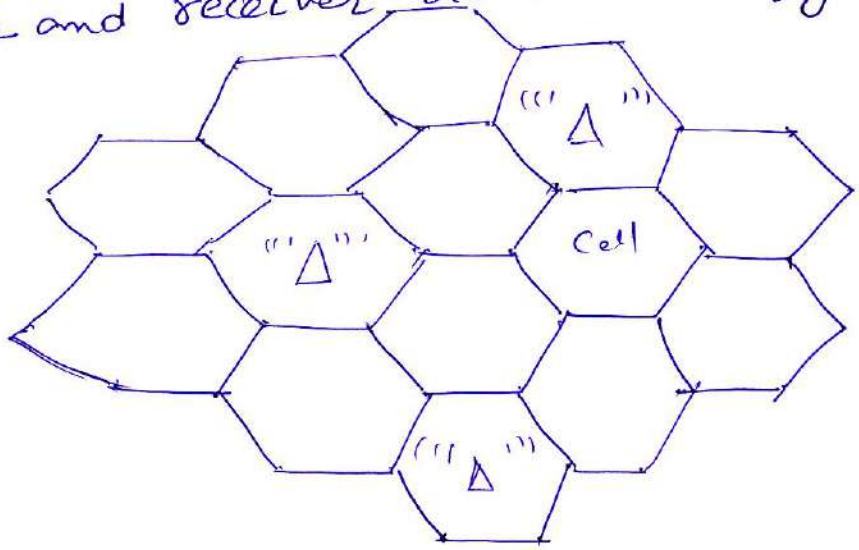


Fig (1). Cell Area in hexagon shape

A single cell covers several square kilometers Contains its own receivers and low power transmitter. The Cell shape is hexagon. If any shape such as triangle Square and Circle Considered results in overlap of areas.

Basic cellular system consists of

- mobile stations
- Base stations
- Mobile switching centre. [MSC]

The mobile switching centre is also known as mobile telephone switching office (MTSO). The MTSO controls the cells and provide the interface between each cell and main telephone office.

Here Each mobile communicates via radio with one of the base stations and may be handed off (switched from one cell to another) to any other base station throughout the duration of the call.

The mobile station commonly consists of

- A Transceiver
- An antenna
- Control unit

The base station consists of several transmitter and receiver which simultaneously handle full duplex communication and generally have towers which support several transmitting and receiving antennas.

The base station serves as a bridge between all mobile users in the cell and connects the simultaneous mobile calls via telephone lines or microwave link to the MSC.

The MSC coordinates the activities of all the base station and connects the entire cellular system to the PSTN. most of the cellular system also provides a service known as roaming.

The cellular system operates in the range 800-900MHz. newer digital cellular system operate at 1.7 - 1.8 GHz band & have greater capacity. Total of 832 channels can be used in the cell.

The block diagram shown in figure ① shows the working of mobile networks through GSM.

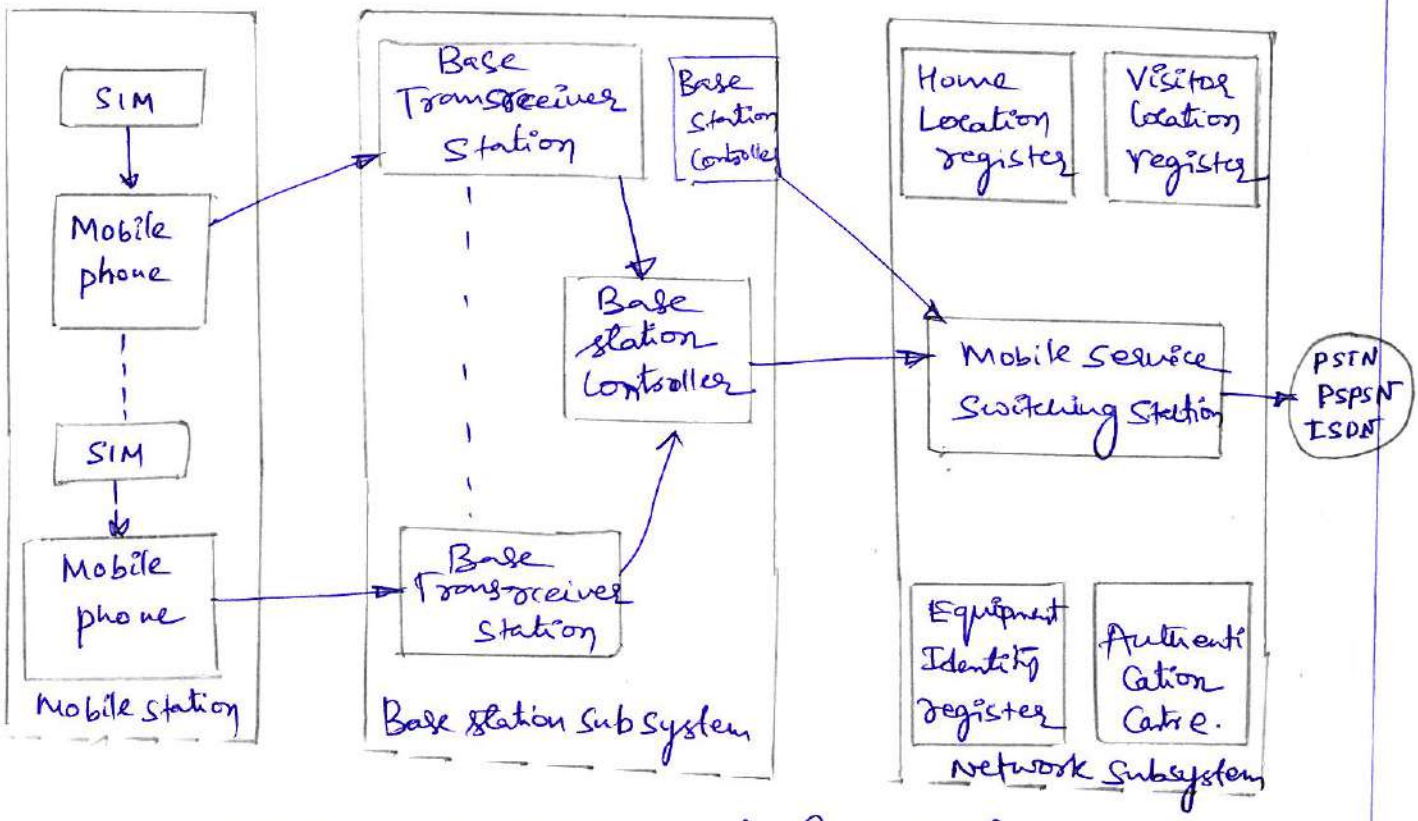


Fig ① Block diagram of GSM System.

The mobile station

It consists of mobile phone (terminal) and a smart card called Subscriber Identity module [SIM]. By inserting SIM card into Mobile phone, the user is able to receive calls at that terminal, make calls from that terminal, and receive other subscribed services. The mobile equipment is uniquely identified by the International Mobile Equipment Identity (IMEI). The SIM card contains the International mobile subscriber Identity (IMSI) used to identify the subscriber to the system, a secret key for authentication, & other information.

Mobile switching centre or Mobile service switching station is a central component of network subsystem. It acts like a normal switching node of the PSTN or ISDN. It provides all the functionality needed to handle a mobile subscriber, such as registeration, authentication, location updating, hand overs, & call routing to a roaming subscribes. The signalling system No. 7 is used for trunking signal in ISDN.

The Home Location Register (HLR) and Vistor Location Register (VLR). together with MSC, provides the call-routing and roaming capabilities of GSM.
HLR contains the administrative information of each subscriber & current location of mobile.

The equipment Identity Register (EIR) is a database that contains a list of valid mobile equipment on the network, where each mobile station is identified by its International mobile equipment Identity (IMEI).

An Authentication Centre is a protected database that stores a copy of the secret key stored in each subscriber's SIM card, which is used for authentication & encryption over the radio channel.

Base station subsystem :-

It composed of two parts, the Base Transceiver Station (BTS) and Base station Controller (BSC).

The BTS houses a radio transceivers that defines a cell and handles the radio-link protocol with the mobile station. In large urban Area more number of BTS will be deployed.

Base station Controller manages the radio resources for one or more BTS's. It handles radio-channel setup, frequency hopping, and hand overs. BSC is the connection between the mobile station and the mobile service switching centre (MSC).

Cellular Telephone unit

The block diagram of a cellular mobile radio unit. The unit consists following blocks.

1. Control unit
2. logic unit
3. Receiver
4. Frequency Synthesizer
5. Transmitter.

Control unit: It is a set of speaker, microphone with touch tone dialing facility and it stores the memory like numbers and dialing features.

Logic unit: - It is the microprocessor controlled master Control unit for cellular radio. It controls the Complete operation of Mobile Telephone switching office (MTSO) and mobile unit.

Receiver: - The cellular receiver consists of RF amplifier FM demodulator and filters. An RF amplifier boots the level of received cell site signal. Received signal is monitored by MTSO. If this is a week signal in the present cell then mobile unit is shifted to other site where the signal is strong.

Frequency Synthesizer: — It is used to generate various signals required for transmitter and receiver. It acts as a signal generator. When a mobile unit initates a call, MTSO identifies the user and assigns a frequency channel which is not used by any other mobile in the cell. MTSO sends a unique code for setting channel Frequencies.

Transmitter:- A low power FM transmitter operating at a frequency range of 825 to 845 MHz. There is a 66630 KHz transmit channel.

The Transmitter produces a deviation of ±12KHz. The modulated output is translated up to final transmitter frequency with the help of mixer, the second input to the transmitter comes from frequency synthesizer. The unique feature of high power translator is that it is controllable by cell site and MTSO. [Mobile Telephone Switching office].

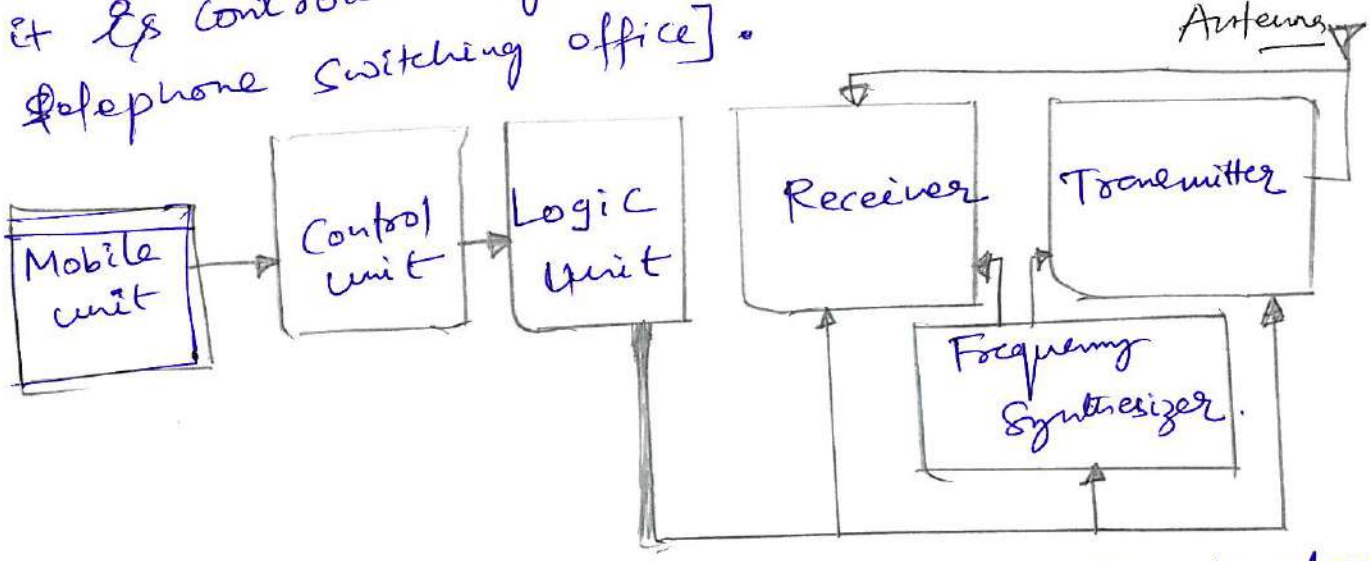


Fig (3): Block diagram of cellular mobile radio network