VISVESVARAYA TECHNOLOGICAL UNIVERSITY

Belgaum, Karnataka

BASIC ELECTRONICS

(18ELN14/18ELN24)

COURSE MATERIAL I/II

Semester

Prepared by

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K.R.Puram, Bangalore

BASIC ELECTRONICS

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I/II

Course Code	18ELN14/24	CIE Marks	40
Number of Lecture Hours/Week	03 (02 + 01 Tutorial)	SEE Marks	60
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

Credits – 03

Course objectives: This course will enable students to:

1. Understand characteristics, operation and applications of the diodes, bipolar junction transistors, field effect transistors, SCRs and operational amplifiers in electronic circuits.
2. Understanddifferent number systems and working of fundamental building blocks of digital circuits.
3. Understand the principle of basic communication system and mobile phones.

Modules	RBT Levels
Module-1	
Semiconductor Diodes and Applications: p-n junction diode, Equivalent circuit of diode, Zener Diode, Zener diode as a voltage regulator, Rectification-Half wave rectifier, Full wave rectifier, Bridge rectifier, Capacitor filter circuit (2.2, 2.3, 2.4 of Text 1). Photo diode, LED, Photocoupler. (2.7.4, 2.7.5, 2.7.6 of Text 1). 78XX series and 7805 Fixed IC voltage regulator (8.4.4 and 8.4.5 of Text 1).	L1, L2, L3
Module-2	
FET and SCR: Introduction, JFET: Construction and operation, JFET Drain Characteristics and Parameters, JFET Transfer Characteristic, Square law expression for I_D, Input resistance, MOSFET: Depletion and Enhancement type MOSFET- Construction, Operation, Characteristics and Symbols,(refer 7.1, 7.2, 7.4, 7.5 of Text 2), CMOS (4.5 of Text 1). Silicon Controlled Rectifier (SCR) – Two-transistor model, Switching action, Characteristics, Phase control application (refer 3.4 upto 3.4.5 of Text 1).	L1, L2, L3

Module-3	
Operational Amplifiers and Applications: Introduction to Op-Amp, Op-Amp Input Modes, Op-Amp Parameters-CMRR, Input Offset Voltage and Current, Input Bias Current, Input and Output Impedance, Slew Rate (12.1, 12.2 of Text 2). Applications of Op-Amp -Inverting amplifier,Non-Inverting amplifier, Summer, Voltage follower, Integrator, Differentiator, Comparator (6.2 of Text 1).	L1, L2, L3
Module-4	
BJT Applications, Feedback Amplifiers and Oscillators: BJT as an amplifier, BJT as a switch, Transistor switch circuit to switch ON/OFF an LED and a lamp in a power circuit using a relay (refer 4.4 and4.5 of Text 2). Feedback Amplifiers – Principle, Properties and advantages of Negative Feedback, Types of feedback, Voltage series feedback, Gain stability with feedback (7.1-7.3 of Text 1). Oscillators – Barkhaunsen's criteria for oscillation, RC Phase Shift oscillator, Wien Bridge oscillator (7.7-7.9 of Text 1). IC 555 Timer and Astable Oscillator using IC 555 (17.2 and 17.3 of Text 1).	L1, L2, L3
Module-5	
Digital Electronics Fundamentals: Difference between analog and digital signals, Number System-Binary, Hexadecimal, Conversion- Decimal to binary, Hexadecimal to decimal and vice-versa, Boolean algebra, Basic and Universal Gates, Half and Full adder, Multiplexer, Decoder, SR and JK flip-flops, Shift register, 3 bit Ripple Counter (refer 10.1-10.7 of Text 1). Basic Communication system, Principle of operations of Mobile phone (refer 18.2 and 18.18 of Text 1).	L1, L2

Course Outcomes: After studying this course, students will be able to:

1. Describe the operation of diodes, BJT, FET and Operational Amplifiers.
2. Designand explainthe construction of rectifiers, regulators, amplifiers and oscillators.
3. Describe general operating principles of SCRs and its application.
4. Explain the working and design of Fixed voltage IC regulator using 7805 and Astable oscillator using Timer IC 555.
5. Explain the different number system and their conversionsand construct simple combinational and sequential logic circuits using Flip-Flops.
6. Describe the basic principle of operation of communication system and

Proposed Activities to be carried out for 10 marks of CIE:

Students should construct and make the demo of the following circuits in a group of 3/4 students:

1. +5v power supply unit using Bridge rectifier, Capacitor filter and IC 7805.
2. To switch on/off an LED using a Diode in forward/reverse bias using a battery cell.
3. Transistor switch circuit to operate a relay which switches off/on an LED.
4. IC 741 Integrator circuit/ Comparator circuit.
5. To operate a small loud speaker by generating oscillations using IC 555.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

1. D.P.Kothari, I.J.Nagarath, "Basic Electronics", 2nd edn, McGraw Hill, 2018.
2. Thomas L. Floyd, "Electronic Devices", Pearson Education, 9th edition, 2012.

1. D.P.Kothari, I.J.Nagarath, "Basic Electronics", 1st edn, McGraw Hill, 2014.
2. Boylestad, Nashelskey, "Electronic Devices and Circuit Theory", Pearson Education, 9th Edition, 2007/11th edition, 2013.
3. David A. Bell, "Electronic Devices and Circuits", Oxford University Press, 5th Edition, 2008.
4. Muhammad H. Rashid, "Electronics Devices and Circuits", Cengage Learning, 2014.

Module-1

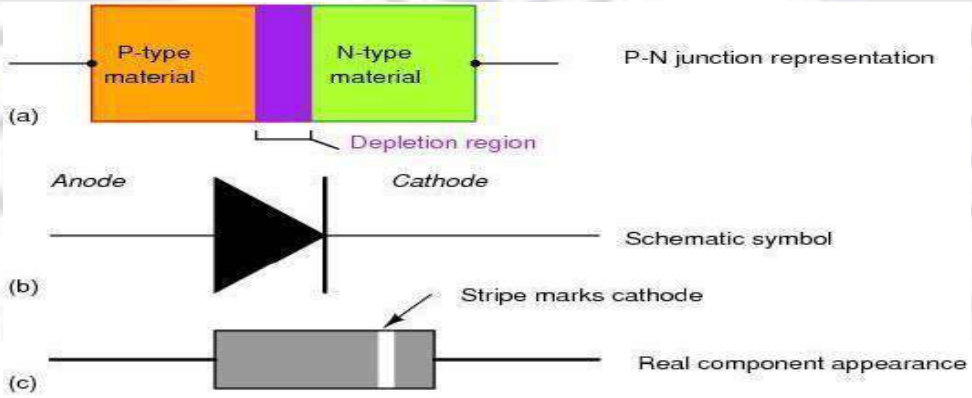
Semiconductor Diodes and Applications

The P-N junction diode is appeared in the year 1950. It is the most essential and the basic building block of the electronic device. The PN junction diode is a two terminal device, which is formed when one side of the PN junction diode is made with p-type and doped with the N-type material. The PN-junction is the root for semiconductor diodes. The various electronic components like BJTs, JFETs, MOSFETs (metal–oxide–semiconductor FET), LEDs and analog or digital ICs all support semiconductor technology. The main function of the semiconductor diode is, it facilitates the electrons to flow totally in one direction across it. Finally, it acts as a rectifier. PN junction diode in forward bias and reverse bias and the VI characteristics of PN junction diode

PN Junction Diode

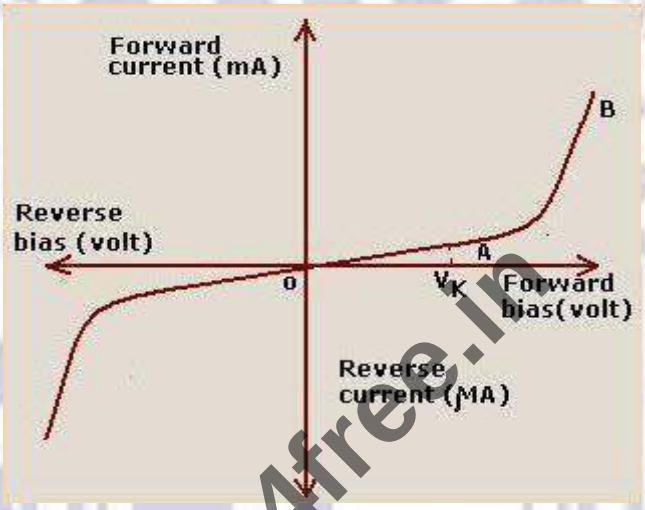
There are three possible biasing conditions and two operating regions for the typical PN-Junction Diode, they are: zero bias, forward bias and reverse bias.

When no voltage is applied across the PN junction diode then the electrons will diffuse to P-side and holes will diffuse to N-side through the junction and they combine with each other. Therefore, the acceptor atom close to the P-type and donor atom near to the N-side are left unutilized. An electronic field is generated by these charge carriers. This opposes further diffusion of charge carriers. Thus, no movement of the region is known as depletion region or space charge.



PN Junction Diode

If we apply forward bias to the PN-junction diode, that means negative terminal is connected to the P-type material and the positive terminal is connected to the N-type material across the diode which has the effect of decreasing the width of the PN junction diode. If we apply reverse bias to the PN-junction diode, that means positive terminal is connected to the P-type material and the negative terminal is connected to the N-type material across the diode which has the effect of increasing the width of the PN junction diode and no charge can flow across the junction



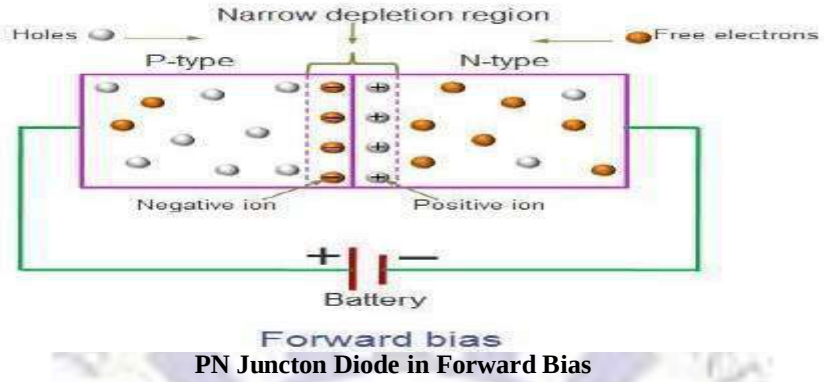
VI Characteristics of PN Junction Diode

Biasing: Connecting a p-n junction to an external d.c. voltage source is called biasing

1. Forward biasing
2. Reverse biasing

Forward Bias

When a PN-junction diode is connected in a forward bias by giving a negative voltage to the N-type and a positive voltage to the P-type material. If the external voltage becomes more than the value of the potential barrier (estimate 0.7 V for Si and 0.3V for Ge, the opposition of the potential barriers will be overcome and the flow of current will start. Because, the negative voltage repels electrons near to the junction by giving them the energy to combine and cross over with the holes being pushed in the opposite direction to the junction by the positive voltage.

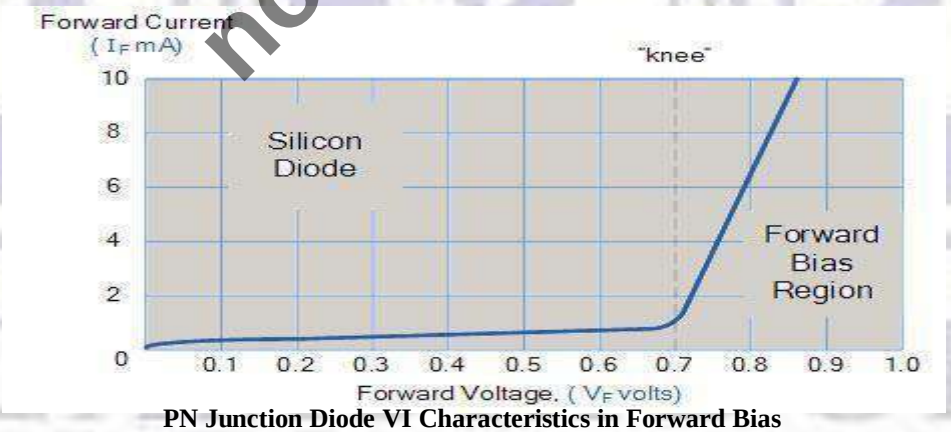


PN Juncton Diode in Forward Bias

The result of this in a characteristic curve of zero current flowing up to built in potential is called as "knee current" on the static curves & then a high current flow through the diode with a slight increase in the external voltage as shown below.

VI Characteristics of PN Junction Diode in Forward Bias

The VI characteristics of PN junction diode in forward bias are non linear, that is, not a straight line. This nonlinear characteristic illustrates that during the operation of the N junction, the resistance is not constant. The slope of the PN junction diode in forward bias shows the resistance is very low. When forward bias is applied to the diode then it causes a low impedance path and permits to conduct a large amount of current which is known as infinite current. This current starts to flow above the knee point with a small amount of external potential.

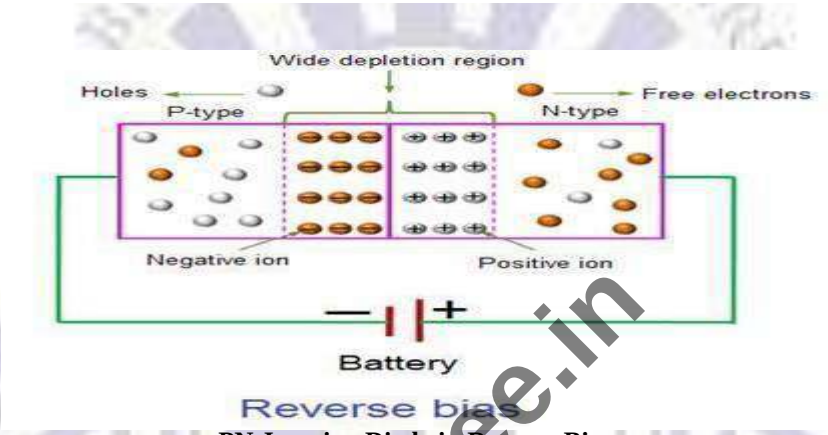


PN Junction Diode VI Characteristics in Forward Bias

The potential difference across the PN junction is maintained constant by the depletion layer action. The max amount of current to be conducted is kept incomplete by the load resistor, because when the PN junction diode conducts more current than the normal specifications of the diode, the extra current results in the heat dissipation and also leads to serve damage to the device.

Reverse Bias

When a PN junction diode is connected in a Reverse Bias condition, a positive (+ Ve) voltage is connected to the N type material & a negative (-Ve) voltage is connected to the P-type material. When the +Ve voltage is applied to the N-type material, then it attracts the electrons near the positive electrode and goes away from the junction, whereas the holes in the P-type end are also attracted away from the junction near the negative electrode.



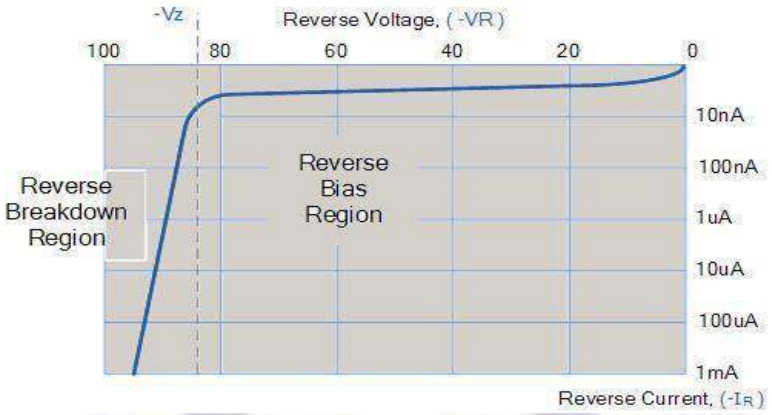
PN Junction Diode in Reverse Bias

In this type of biasing, current flow through the PN junction diode is zero. Though, the current leakage due to minority charge carriers flows in the diode that can be measured in a uA (micro amperes). As the potential of the reverse bias to the PN junction diode ultimately increases and leads to PN junction reverse voltage breakdown and the current of the PN junction diode is controlled by an external circuit. Reverse breakdown depends on the doping levels of the P & N regions. Further, with the increase in reverse bias the diode will become short circuited due to overheat in the circuit and max circuit current flows in the PN junction diode.

VI Characteristics of PN Junction Diode in Reverse Bias

In this type of biasing, the characteristic curve of diode is shown in the fourth quadrant of the below figure. The current in this biasing is low till breakdown is reached and hence the diode looks like as open circuit. When the input voltage of the reverse bias has reached the breakdown

n voltage, reverse current increases enormously.



PN Junction Diode VI Characteristics in Reverse Bias

Diode Relationship

The current in a diode is given by the diode current equation
$I = I0(e V/\eta VT -1)$
Where,

I ------diode current
I0------ reverse saturation current
V ------diode voltage
η ------ semiconductor constan=1 for Ge, 2 for Si.
VT ------Voltage equivalent of temperature= T/11,600 (Temperature T is in Kelvin)

Basic Definitions

1. Knee voltage or Cut-in Voltage.

It is the forward voltage at which the diode starts conducting.

2. Breakdown voltage

It is the reverse voltage at which the diode (p-n junction) breaks down with sudden rise in reverse current.

3. Peak-inverse voltage (PIV)

It is the max reverse voltage that can be applied to a p-n junction without causing damage to the junction. If the reverse voltage across the junction exceeds its peak-inverse voltage, then the junction exceeds its Peak-inverse voltage, then the junction gets destroyed because of excessive heat. In rectification, one thing to be kept in mind is that care should be taken that reverse voltage across the diode during –ve half cycle of a.c. doesnot exceed the peak-inverse voltage of the diode.

4. Maximum Forward current

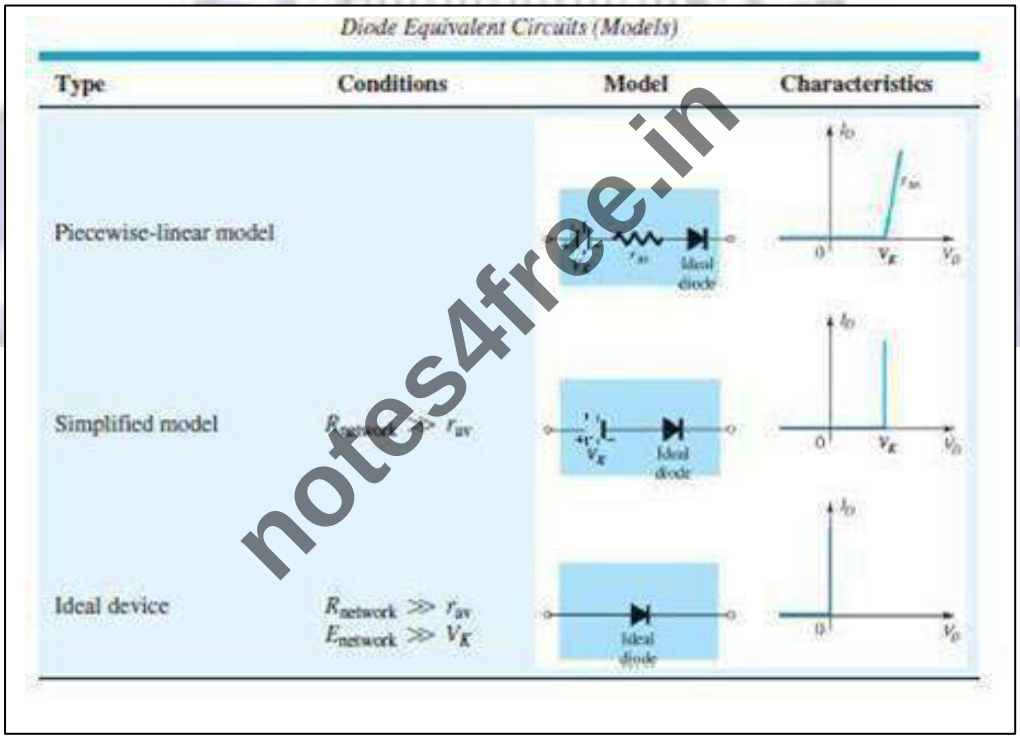
It is the Max. Instantaneous forward current that a p-n junction can conduct without damaging the junction. If the forward current is more than the specified rating then the junction gets destroyed due to over heating.

5. Maximum Power rating

It is the maximum power that can be dissipated at the junction without damaging it. The power dissipated across the junction is equal to the product of junction current and the voltage across the junction.

Diode equivalent Circuit:

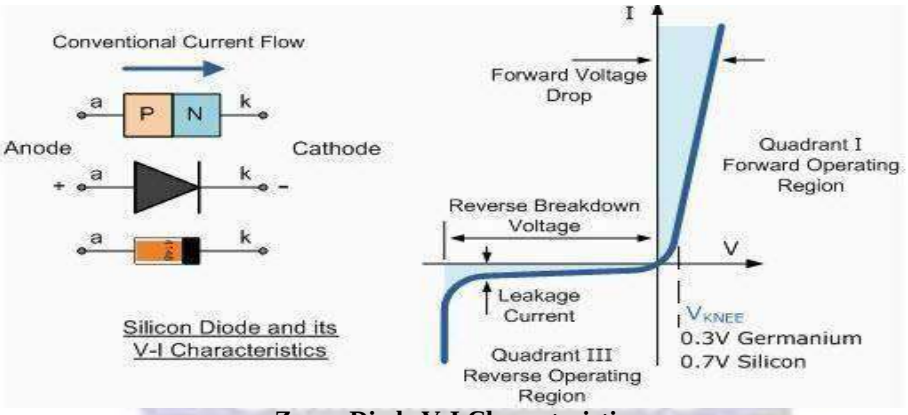
Equivalent circuit is a combination of element properly chosen to best represent the actual terminal characteristics of a device or system in a particular operating point.



Zener Diode

It is mainly a special property of the diode rather than any special type of equipment. The person named Clearance Zener invented this property of the diode that's why it is named after him as a remembrance. The special property of the diode is that there will be a breakdown in the circuit if the voltage applied across a reversely biased circuit. This does not allow the current to flow across it. When the voltage across the diode is increased, temperature also increases and the crystal ions vibrate with greater amplitude and all these leads to the breakdown of the depletion

layer. The layer at the junction of 'P' type and 'N' type. When the applied voltage exceeds an specific amount Zener breakdown takes place.

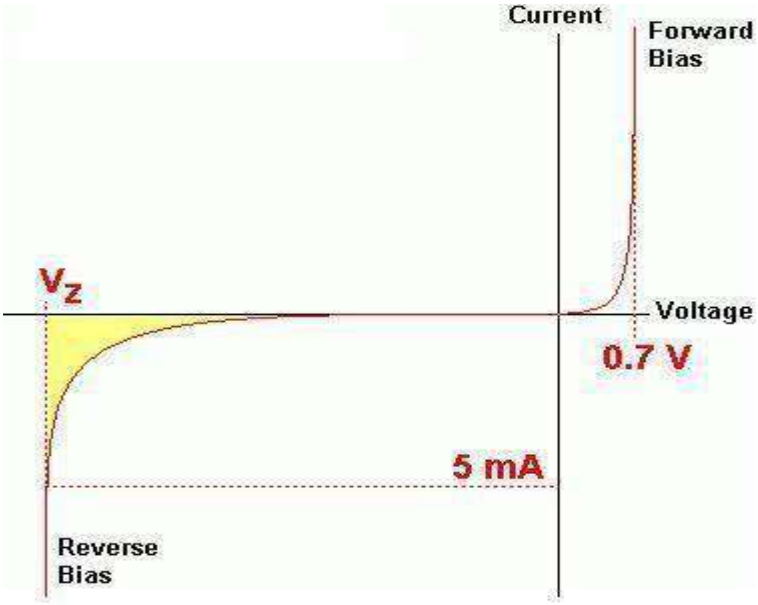


Zener Diode V-I Characteristics

Zener diode is nothing but a single diode connected in a reverse bias mode and Zener diode can be connected in reverse bias positive in a circuit as shown as picture.we can connect it for different applications. The circuit symbol of Zener diode is as shown in the figure. For convenience it is used normally. When discussing about the diode circuits we should look through the graphical representation of the operation of the Zener diode. It is called the V-I characteristics of a general p – n junction diode.

Characteristics of a Zener Diode

The above diagram shows the V-I characteristics of the Zener diode behavior. When the diode is connected in forward bias diode acts as a normal diode. When the reverse bias voltage is greater than a predetermined voltage then the Zener breakdown voltage occurs. To get breakdown voltage sharp and distinct doping is controlled and the surface imperfections are avoided. In the V-I characteristics above Vz is the Zener voltage. And also the knee voltage because at this point the current is the current is very rapid.

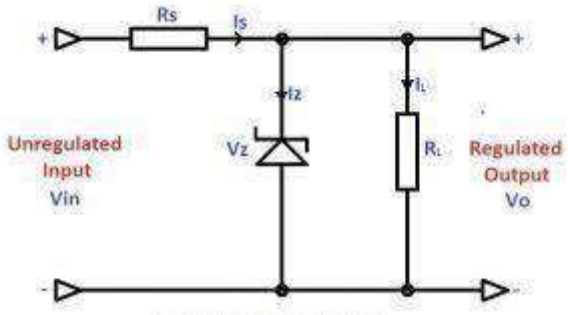


Zener Diode behavior

Zener Diode as Voltage Regulator

Zener Diodes are widely used as Shunt Voltage Regulators to regulate voltage across small loads. Zener Diodes have a sharp reverse breakdown voltage and breakdown voltage will be constant for a wide rang of currents. Thus we will connect the zener diode parallel to the load such that the applied voltage will reverse bias it. Thus if the reverse bias voltage across the zener diode exceeds the knee voltage, the voltage across the load will be constant.

Circuit Diagram



Zener Diode Voltage Regulator Circuit Diagram

In the above circuit diagram excess voltage (Vin – Vz) will drop across Rs thus by limiting the current through Zener. For the proper designing of the regulator we should know,

- Unregulated Input Voltage Range
- Required Output Voltage
- Max Load Current Required

The value of resistance Rs should satisfy the following conditions,

- The value of Rs must be small enough to keep the Zener Diode in reverse breakdown region. The minimum current required for a Zener Diode to keep it in reverse breakdown region will be given in its datasheet. For example, a 5.6 V, 0.5 W zener diode has a recommended reverse current of 5 mA. If the reverse current is less than this value, the output voltage Vo will be unregulated.
- The value of Rs must be large enough that the current through the zener diode should not destroy it. That is the maximum power dissipation Pmax should be less than IzVz.

Thus we should find $R_s$min and $R_s$max. To find the value of $R_s$min we should consider the extreme condition that Vin is minimum and load current is maximum.

$I_s = I_z$min+$I_L$max

$I_z$min=PleaseReferDatasheet $V_s = V_{in}$min–Vz

$R_s$min=Vs/Is

To find the value of $R_s$max we should consider the extreme condition that Vin is maximum and load current is minimum (ie, no load connected).

$I_s = I_z$max+$I_L$min

$I_z$max=Pmax/Vz

$V_s = V_{in}$max–Vz

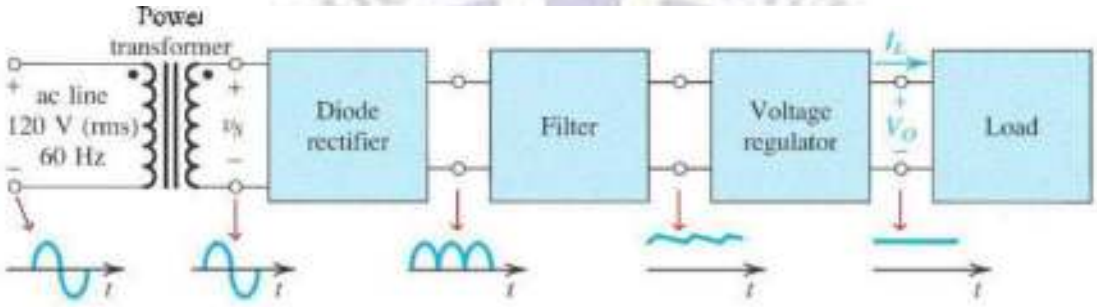
$R_s$max = Vs/Is

RECTIFIERS

An important application of "regular" diodes is in rectification circuits. These circuits are used to convert AC signals to DC in power supplies.

"Rectifiers are the circuit which converts ac to dc"

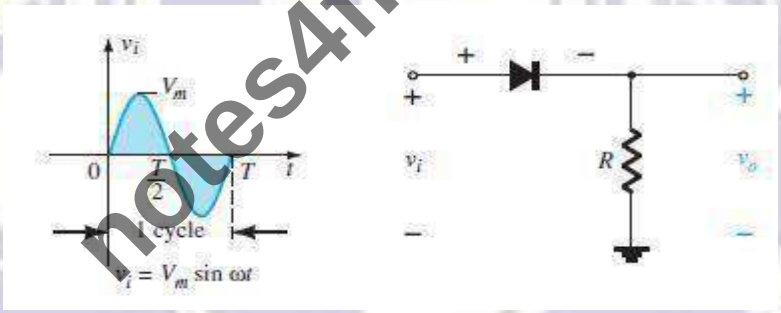
A block diagram of this process in a DC power supply is shown below.



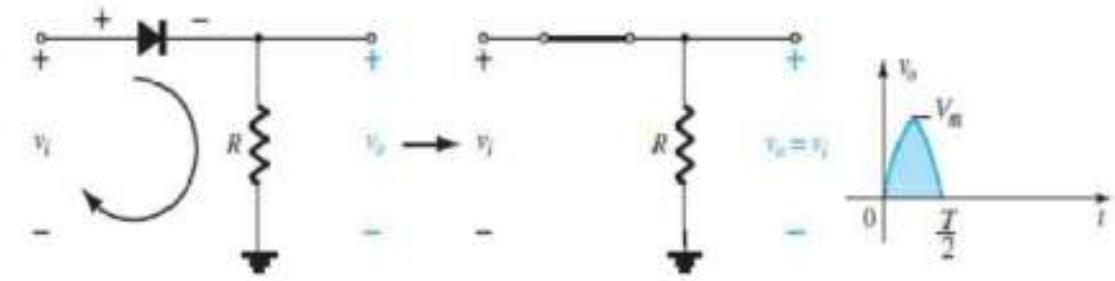
Rectifiers are grouped into two categories depending on the period of conductions.

1. Half-wave rectifier
2. Full- wave rectifier.

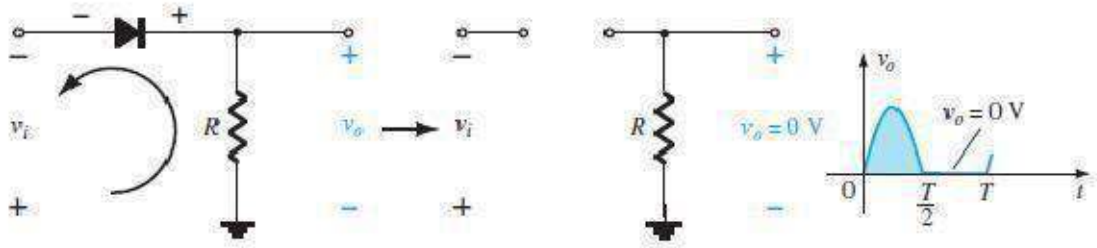
Half-Wave Rectifier:



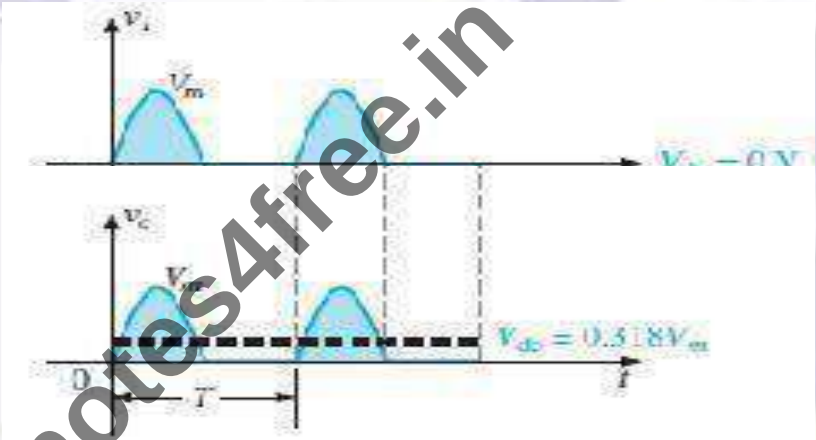
The above circuit is called as a Half -wave rectifier since it will generate a waveform v_o that will have an average value of particular use in the ac-to-dc conversion process.



During (Positive Half Cycle) the diode is ON. Assuming an ideal diode with no voltage drop across it the output voltage v_o will be $v_o=V_R=V_m$



During (Negative Half Cycle) the diode is OFF(Open Circuit). So the current flowing through the circuit will be 0. The output voltage v_o will be $v_o= V_R=i \times R = 0$
Figure shows the input and output waveform with output $V_{dc}=0.318V_m$.



Disadvantage:

1. The ac supply delivers power only half the time.
2. Pulsating current frequency is equal to the supply frequency.

Derivations

1. RMS output current

The value of the R.M.S. current is given by

$$I_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} i^2 d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2 \omega t . d(\omega t) + \frac{1}{2\pi}\int_{\pi}^{2\pi} .0 . d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{2\pi}\int_0^{\pi}\left(\frac{1-\cos\omega t}{2}\right) d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi}\left\{(\omega t) - \frac{1}{2}\sin\omega t\right\}_0^{\pi}\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi}\left\{\pi - 0 - \frac{\sin 2\pi}{2} + \sin 0\right\}\right]^{\frac{1}{2}}$$

$$= \left(\frac{I_m^2}{4}\right)^{\frac{1}{2}}$$

$$= \frac{I_m}{2}$$

$$\therefore I_{rms} = \frac{I_m}{2} \text{ (or) } I_{rms} = \frac{V_m}{2\ R_f + R_L}$$

Vout Calculation

$$v(t) = \begin{cases} V_m \sin \omega t & for\ t \le \frac{T}{2} \\ 0 & for\ \frac{T}{2} < t < T \end{cases}$$

2. Vdc or Vavg

We then compute the average voltage (dc voltage) Vavg or Vdc for one complete cycle

$$V_{av} = \frac{1}{T_o}\int_0^T v(t)dt$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin \omega t\, d\omega t + \int_{\pi}^{2\pi} 0\, d\omega t\right]$$

$$= \frac{V_m}{2\pi}[-\cos \omega t]_0^{\pi} = \frac{V_m}{2\pi}[-\cos(\pi) - (-\cos 0)]$$

$$= \frac{V_m}{2\pi}[-(-1) - (-1)] = \frac{V_m}{\pi} = 0.318V_m$$

$$= 0.318(\pi/2)V_m = 0.45V_m$$

3. Vrms at the Load Resistance

$$v(t) = \begin{cases} V_m \sin \omega t & \text{for } t \le \frac{T}{2} \\ 0 & \text{for } \frac{T}{2} < t < T \end{cases}$$

$$V_{rms} = \sqrt{\frac{1}{T_0}\int_0^T v^2(t)dt}$$

$$= \left[\frac{1}{2\pi}\left[\int_0^{T/2} V_m^2 \sin^2 \omega t\, d(\omega t) + \int_{T/2}^{T} 0\, d(\omega t)\right]\right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi}\int_0^{T/2} \sin^2 \omega t\, d(\omega t)\right]^{1/2}$$

$\sin^2 \omega t = \frac{1}{2}(1 - \cos 2\omega t)$, $\omega T = 2\pi$, $\theta = \omega t$

$$V_{rms} = \left[\frac{V_m^2}{4\pi}\int_0^{\pi} (1 - \cos 2\theta)d\theta\right]^{1/2}$$

$$= \left[\frac{V_m^2}{4\pi}\left(\theta - \frac{1}{2}\sin 2\theta\right)_0^{\pi}\right]^{1/2}$$

$$= \left[\frac{V_m^2}{4\pi}(\pi - \tfrac{1}{2}\sin(2\pi) - 0 + \tfrac{1}{2}\sin 2(0)\right]^{1/2}$$

$$= \left[\frac{V_m^2}{4\pi}(\pi - 0 - 0 + 0)\right]^{1/2}$$

$$= \frac{V_m}{2}$$

4. Compute Ripple Factor

Ripple Factor = RMS value of the AC component/DC value of the component

$$Ripple = \frac{Vr_{rms}}{V_{dc}}$$

$$= \frac{\sqrt{V_{rms}^{\ 2} - V_{dc}^{\ 2}}}{V_{dc}}$$

$$= \sqrt{\left[\frac{V_{rms}}{V_{dc}}\right]^2 - 1}$$

$$= \sqrt{\left[\frac{V_m / 2}{V_m / \pi}\right]^2 - 1}$$

$$= \sqrt{\left[\frac{\pi}{2}\right]^2 - 1}$$

$$= 1.2114$$

5. Efficiency

η = (dc output power/ac input power) x 100%

$$\eta = \frac{V_{dc}^{\ 2} / R_L}{V_{rms}^{\ 2} / R_L} = \frac{(V_m / \pi)^2}{(V_m / 2)^2} = \frac{4}{\pi^2} = 0.406$$

or

$$\eta = 40.6\%$$

6. Form Factor

FF = rms value / average value = (Vm/2)/(Vm/π)= π/2 = 1.57

7. Peak Factor

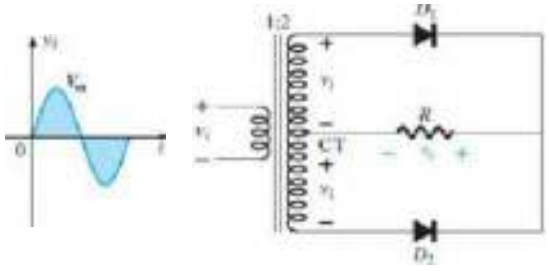
Peak value / rms value = Vm/(Vm/2) = 2

Full wave Rectifier:

The full wave rectifier utilizes both the positive and negative portions of the input waveform.
Types of full wave rectifier are

(a) Centre tapped configuration
(b) Bridge configuration

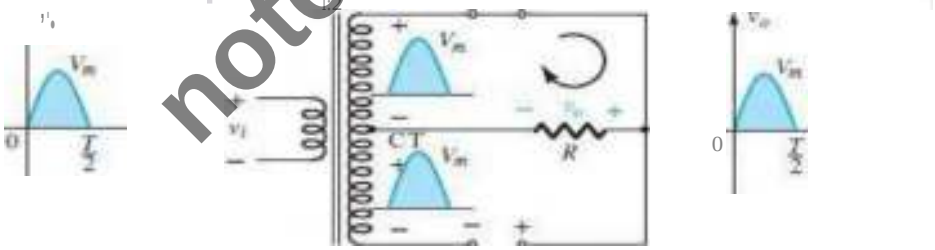
Centre tapped configuration:



- Current flows through the load resistance in the same direct n during the full cycle of the input signal.
- Centre tap transformer is used with the secondary winding.

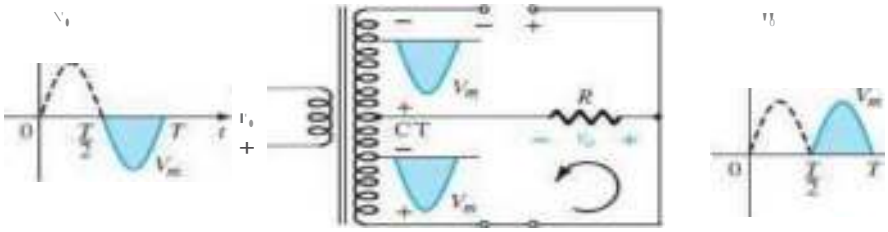
+ve Half Cycle:

- Diode D_1 is short circuited and D_2 is open circuited. Current flows through the upper half of the secondary winding.

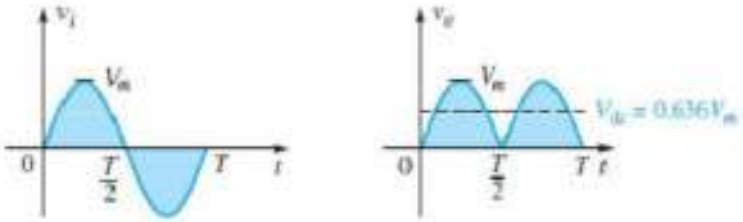


-ve Half Cycle:

Diode D_2 is short circuited and D_1 is open circuited. Current flows through the lower half of the secondary winding.



Complete input and output waveform can be shown as



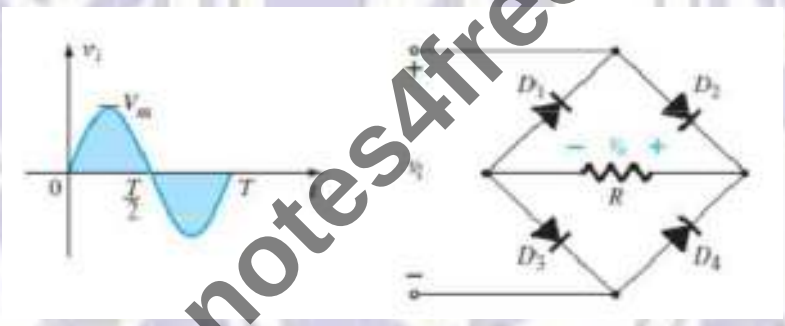
While this full-cycle rectifier is a big improvement over the half-cycle, there are some disadvantages.

Disadvantages:

- It is difficult to locate the centre tap on the secondary winging.
- The diodes must have high PIV.

BridgeRectifier:

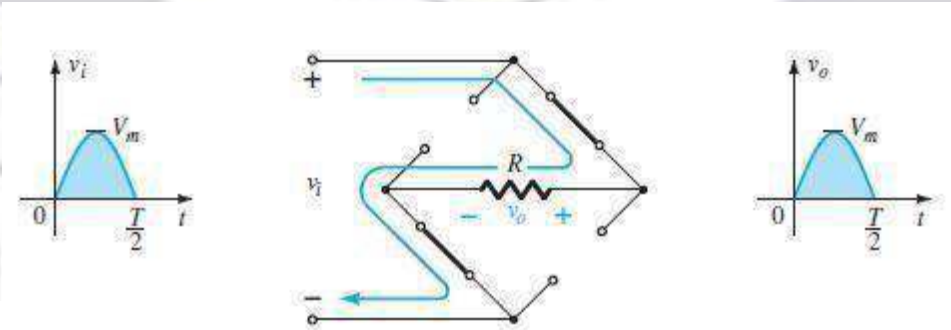
The bridge rectifier uses four diodes connected in bridge pattern.



The operation of the bridge rectifier can be summarized as:

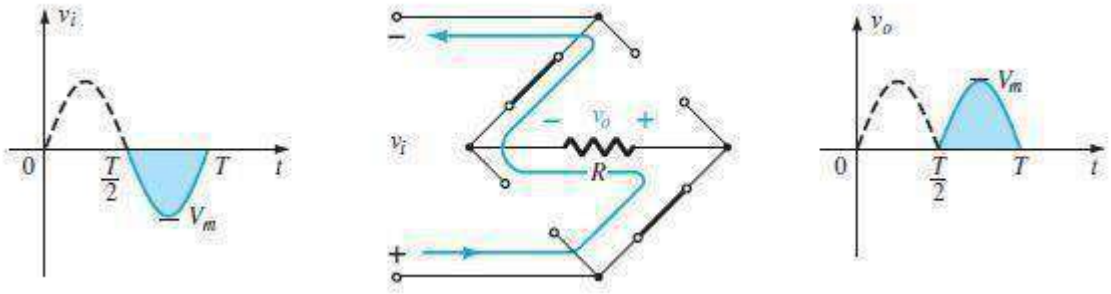
+ve Half Cycle:

Diode D_1 and D_3 are short circuited and D_2 and D_4 are open circuited. Current flows through D_1 and D_3 to give the output voltage across the resistor.

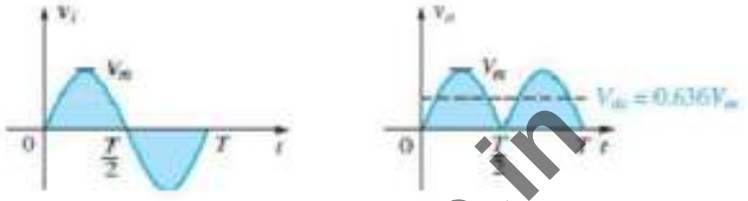


-ve Half Cycle:

Diode D_1 and D_3 are open circuited and D_2 and D_4 are short circuited. Current flows through D_2 and D_4 to give the output voltage across the resistor.



Complete input and output waveform can be shown as



Advantages:

- No centre tapped transformer is required.
- PIV is less.

Disadvantages:

It requires four diode and the power loss in the rectifier element is more.

Derivation for FWR

The average voltage or the dc voltage available across the load resistance is

$$V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \, d(\omega t)$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi} \quad and \quad I_{rms} = \frac{I_m}{\sqrt{2}}$$

RMS value of the voltage at the load resistance is

$$V_{rms} = \left[\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t \, d(\omega t)\right]^{\frac{1}{2}} = \frac{V_m}{\sqrt{2}}$$

Ripple Factor

The ripple factor for a Full Wave Rectifier is given by

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$\therefore \gamma = \sqrt{\left(\frac{V_m/2}{2V_m/\pi}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{8}\right)^2 - 1} = 0.482$$

Efficiency

Efficiency, η is the ratio of dc output power to ac input power

$$\eta = \frac{dc\ output\ power}{ac\ input\ power} = \frac{P_{dc}}{P_{ac}}$$

$$\frac{V_{dc}^2/R_L}{V_{rms}^2/R_L} = \frac{\left[2V_m/\pi\right]^2}{\left[V_m/\sqrt{2}\right]^2} = 8/\pi^2 = 0.812 = 81.2\%$$

The maximum efficiency of a Full Wave Rectifier is 81.2%.

Transformer Utilization Factor

Transformer Utilization Factor, TUF can be used to determine the rating of a transformer secondary. It is determined by considering

the primary and the secondary winding separately and it gives a value of 0.693.

Form Factor

Form factor is defined as the ratio of the rms value of the output voltage to the average value of the output voltage.

$$Form\ factor = \frac{rms\ value\ of\ output\ voltage}{average\ value\ of\ the\ output\ voltage}$$

$$= \frac{\left(V_m/\sqrt{2}\right)}{\left(2V_m/\pi\right)} = \frac{\pi}{2\sqrt{2}} = \underline{\underline{1.11}}$$

Peak Factor

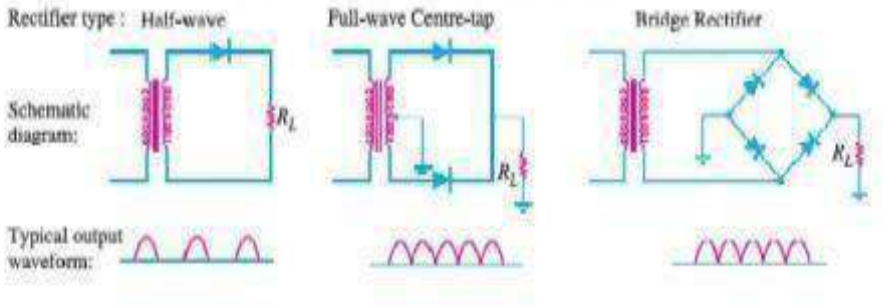
Peak factor is defined as the ratio of the peak value of the output voltage to the rms value of the output voltage.

$$Peak\ factor = \frac{peak\ value\ of\ the\ output\ voltage}{rms\ value\ of\ the\ output\ voltage} = \frac{V_m}{\left(V_m/\sqrt{2}\right)} = \underline{\underline{\sqrt{2}}}$$

Peak inverse voltage for Full Wave Rectifier is $2V_m$ because the entire secondary voltage appears across the non-conducting diode.

This concludes the explanation of the various factors associated with Full Wave Rectifier

Comparison Between HW, FW & FWB Rectifiers



S. No.	Parameter	HWR	CTFWR	BTFWR
1	No. of Diode	1	2	4
2	Output Frequency	f_i	$2f_i$	$2f_i$
3	DC load Current (I_{dc})	I_m/π	$2I_m/\pi$	$2I_m/\pi$
4	No load DC voltage (V_{dc})	V_m/π	$2V_m/\pi$	$2V_m/\pi$
5	RMS load current (I_{rms})	$I_m/2$	$I_m/\sqrt{2}$	$I_m/\sqrt{2}$
6	RMS load voltage (V_{rms})	$V_m/2$	$V_m/\sqrt{2}$	$V_m/\sqrt{2}$
7	Efficiency (η)	$\frac{P_{odc}}{Pi_{ac}}=\frac{I^2_{dc}R_L}{I^2_{rms}R_L}$ (40.6%)	$\frac{P_{odc}}{Pi_{ac}}=\frac{I^2_{dc}R_L}{I^2_{rms}R_L}$ (81.2%)	$\frac{P_{odc}}{Pi_{ac}}=\frac{I^2_{dc}R_L}{I^2_{rms}R_L}$ (81.2%)
8	TUF	$\frac{I^2_{dc}}{I_{2rms}V_{2rms}}$	$\frac{I^2_{dc}}{I_{2rms}V_{2rms}}$	$\frac{I^2_{dc}}{I_{2rms}V_{2rms}}$
9	Ripple factor	$\frac{V^2_{rms}-V^2_{dc}}{V_{dc}}$ (1.21)	$\frac{V^2_{rms}-V^2_{dc}}{V_{dc}}$ (0.482)	$\frac{V^2_{rms}-V^2_{dc}}{V_{dc}}$ (0.482)
10	PIV	V_m	$2V_m$	V_m
11	Ripple Frequency	f_i	$2f_i$	$2f_i$

FILTERS

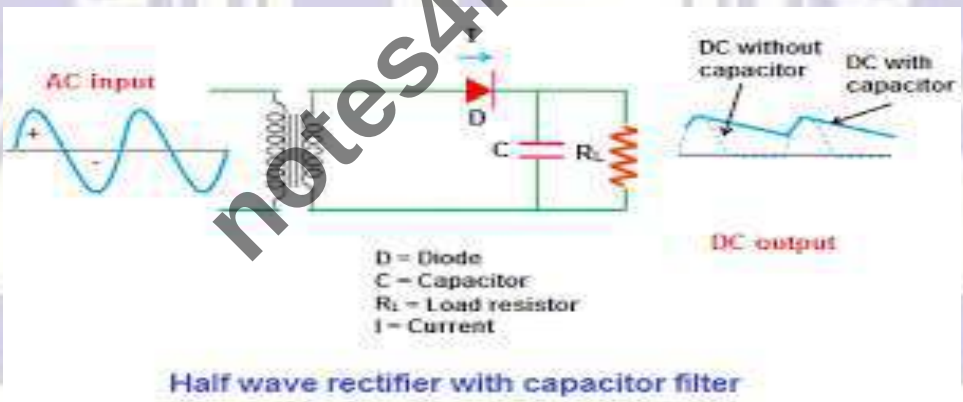
Types of Filters

1. Capacitor Filter (C-Filter)
2. Inductor Filter
3. Choke Input Filter (LC-filter)
4. Capacitor Input Filter (Π-filter)

Capacitor Filter(C-filter)

A capacitor-input filter is a filter circuit in which the first element is a capacitor connected in parallel with the output of the rectifier in a linear power supply. The capacitor increases the DC voltage and decreases the ripple voltage components of the output. The capacitor is often followed by other alternating series and parallel filter elements to further reduce ripple voltage, or adjust DC output voltage. It may also be followed by a voltage regulator which virtually eliminates any remaining ripple voltage, and adjusts the DC voltage output very precisely to match the DC voltage required by the circuit.

Circuit Diagram



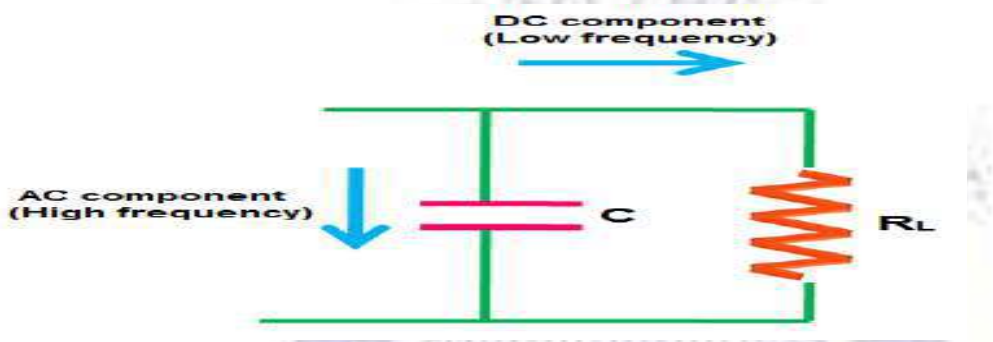
Half wave rectifier with capacitor filter

When AC voltage is applied, during the positive half cycle, the diode D is forward biased and allows electric current through it.

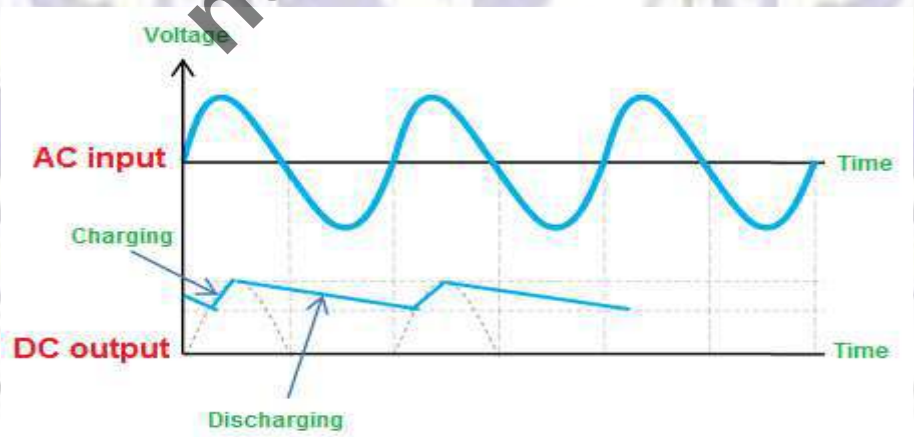
As we already know that, the capacitor provides high resistive path to dc components (low-frequency signal) and low resistive path to ac components (high-frequency signal).

Electric current always prefers to flow through a low resistance path. So when the electric current reaches the filter, the dc components experience a high resistance from the capacitor and ac components experience a low resistance from the capacitor.

The dc components does not like to flow through the capacitor (high resistance path). So they find an alternative path (low resistance path) and flows to the load resistor (RL) through that path.



On the other hand, the ac components experience a low resistance from the capacitor. So the ac components easily passes through the capacitor. Only a small part of the ac components passes through the load resistor (R_L) producing a small ripple voltage at the output. The passage of ac components through the capacitor is nothing but charging of the capacitor. In simple words, the ac components is nothing but an excess current that flows through the capacitor and charges it. This prevents any sudden change in the voltage at the output. During the conduction period, the capacitor charges to the maximum value of the supply voltage. When the voltage between the plates of the capacitor is equal to the supply voltage, the capacitor is said to be fully charged.



Half wave rectifier with filter o/p waveforms

When the capacitor is fully charged, it holds the charge until the input AC supply to the rectifier reaches the negative half cycle.

When the negative half cycle is reached, the diode D gets reverse biased and stops allowing electric current through it. During this non-conduction period, the input voltage is less than that of the capacitor voltage. So the capacitor discharges all the stored charges through the load resistor R_L. This prevents the output load voltage from falling to zero. The capacitor discharges until the input supply voltage is less than the capacitor voltage. When the input supply voltage is greater than the capacitor voltage, the capacitor again starts charging. When the positive half cycle is reached again, the diode D is forward biased and allows electric current. This makes capacitor to charge again. The capacitor filter with a large discharge time constant will produce a very smooth DC voltage.Thus, a smooth and steady DC voltage is obtained by using the filter.

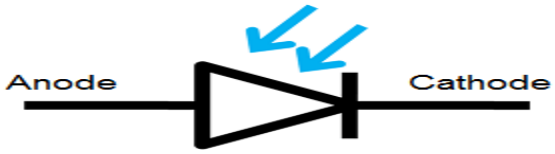
PHOTODIODE

A **photodiode** is a semiconductor device that converts light into an electrical current. The current is generated when photons are absorbed in the photodiode. Photodiodes may contain optical filters, built-in lenses, and may have large or small surface areas. Photodiodes usually have a slower response time as their surface area increases. The common, traditional solar cell used to generate electric solar power is a large area photodiode.

Photodiodes are similar to regular semiconductor diodes except that they may be either exposed (to detect vacuum UV or X-rays) or packaged with a window or optical fiber connection to allow light to reach the sensitive part of the device. Many diodes designed for use specifically as a photodiode use a PIN junction rather than a p–n junction, to increase the speed of response. A photodiode is designed to operate in reverse bias

Photodiode symbol

The symbol of photodiode is similar to the normal p-n junction diode except that it contains arrows striking the diode. The arrows striking the diode represent light or photons. A photodiode has two terminals: a cathode and an anode.



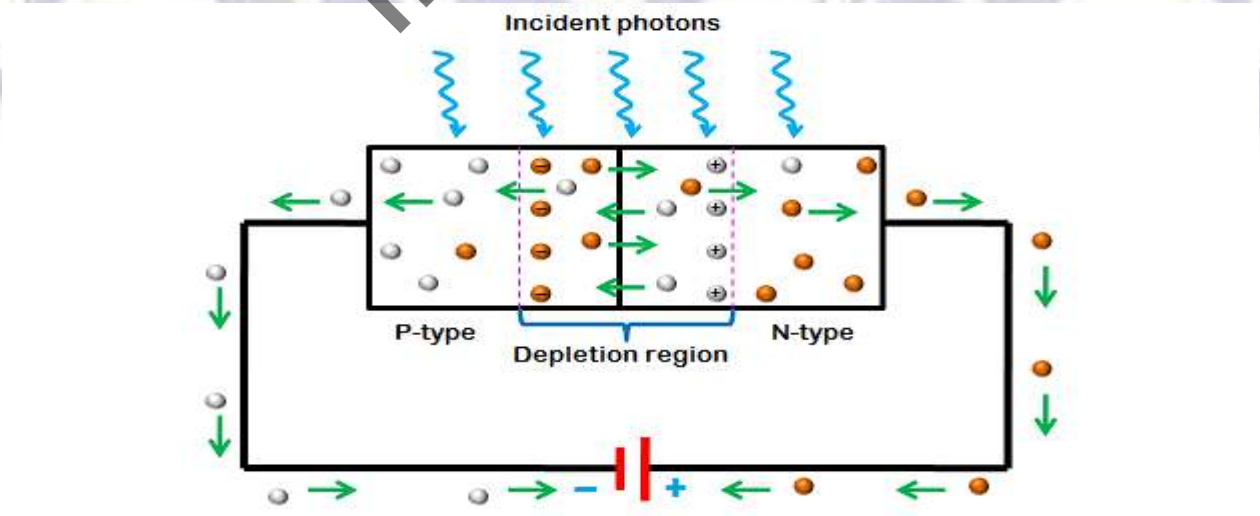
Photodiode symbol

How photodiode works

A normal p-n junction diode allows a small amount of electric current under reverse bias condition. To increase the electric current under reverse bias condition, we need to generate more minority carriers. The external reverse voltage applied to the p-n junction diode will supply energy to the minority carriers but not increase the population of minority carriers. However, a small number of minority carriers are generated due to external reverse bias voltage. The minority carriers generated at n-side or p-side will recombine in the same material before they cross the junction. As a result, no electric current flows due to these charge carriers. For example, the minority carriers generated in the p-type material experience a repulsive force from the external voltage and try to move towards n-side. However, before crossing the junction, the free electrons recombine with the holes within the same material. As a result, no electric current flows.

To overcome this problem, we need to apply external energy directly to the depletion region to generate more charge carriers.

A special type of diode called photodiode is designed to generate more number of charge carriers in depletion region. In photodiodes, we use light or photons as the external energy to generate charge carriers in depletion region.



PN Junction photodiode

Light Emitting Diode

In the simplest terms, a light-emitting diode (LED) is a semiconductor device that emits light when an electric current is passed through it. Light is produced when the particles that carry the current (known as electrons and holes) combine together within the semiconductor material.

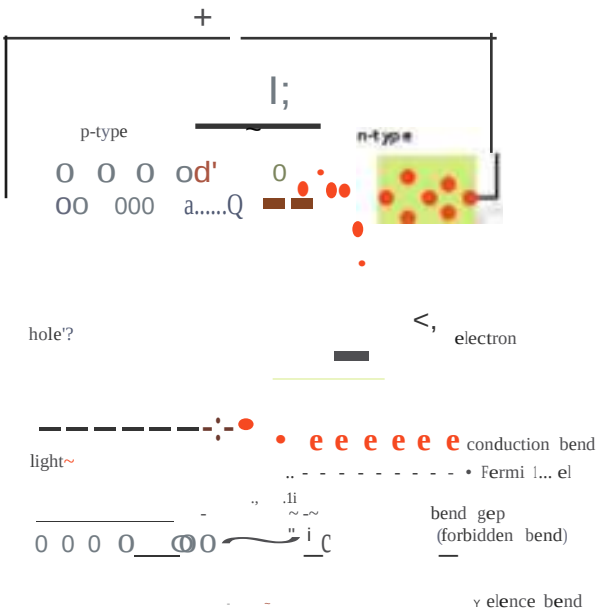
Since light is generated within the solid semiconductor material, LEDs are described as solid-state devices. The term solid-state lighting, which also encompasses organic LEDs (OLEDs), distinguishes this lighting technology from other sources that use heated filaments (incandescent and tungsten halogen lamps) or gas discharge (fluorescent lamps)

Working Principle of LED

The inner workings of an LED, showing circuit (top) and band diagram (bottom)

A P-N junction can convert absorbed light energy into a proportional electric current. The same process is reversed here (i.e. the P-N junction emits light when electrical energy is applied to it). This phenomenon is generally called electroluminescence, which can be defined as the emission of light from a semiconductor under the influence of an electric field. The charge carriers recombine in a forward-biased P-N junction as the electrons cross from the N-region and recombine with the holes existing in the P-region. Free electrons are in the conduction band of energy levels, while holes are in the valence energy band. Thus the energy level of the holes is less than the energy levels of the electrons. Some portion of the energy must be dissipated to recombine the electrons and the holes. This energy is emitted in the form of heat and light.

The electrons dissipate energy in the form of heat for silicon and germanium diodes but in gallium arsenide phosphide (GaAsP) and gallium phosphide (GaP) semiconductors, the electrons dissipate energy by emitting photons. If the semiconductor is translucent, the junction becomes the source of light as it is emitted, thus becoming a light-emitting diode. However, when the junction is reverse biased, the LED produces no light and—if the potential is great enough, the device is damaged.

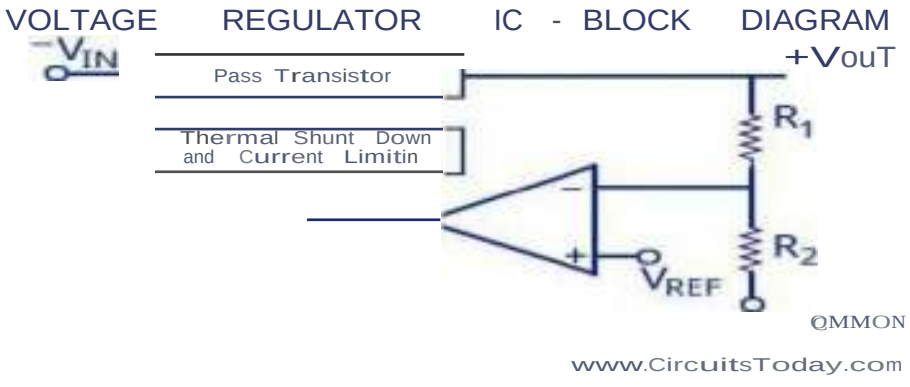


electronic c

VOLTAGE REGULATOR

A voltage regulator is one of the most w i ircuitry in any device. A regulated voltage (without fluctuations & noise levels) is very important for the smooth functioning of many digital electronic devices. A common case is with micro controllers, where a smooth regulated input voltage must be supplied for the micro controller to function smoothly.

78xx (sometimes L78xx, LM78xx, MC78xx...) is a family of self-contained fixed linear voltage regulator integrated circuits. The 78xx family is commonly used in electronic circuits requiring a regulated power supply due to their ease-of-use and low cost.



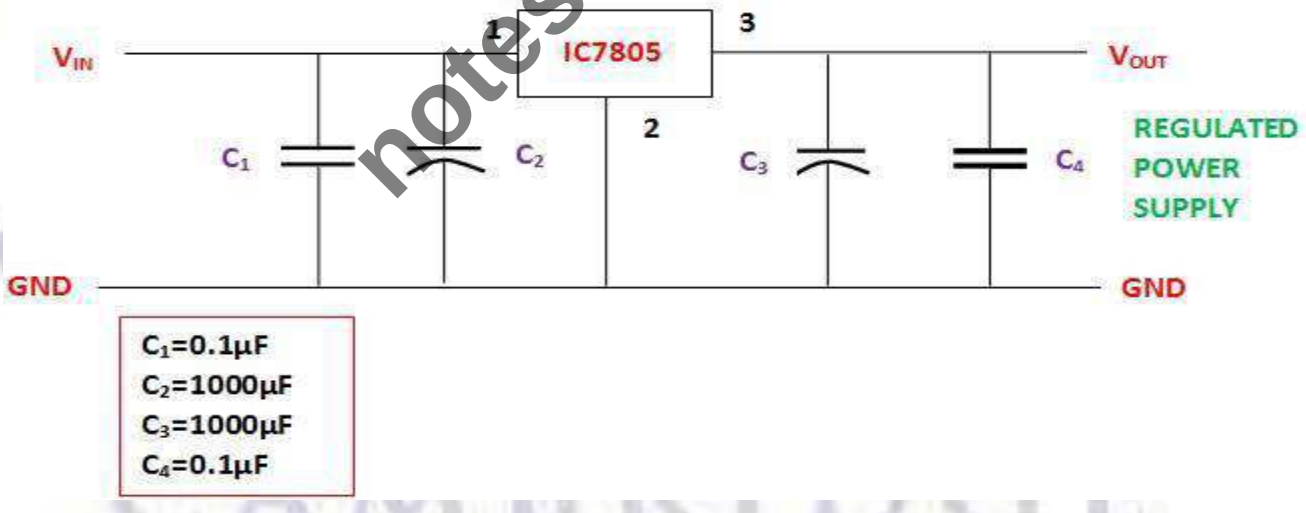
Fixed Voltage Regulators

These regulators provide a constant output voltage. A popular example is the 7805 IC which provides a constant 5 volts output. A fixed voltage regulator can be a positive voltage regulator or a negative voltage regulator. A positive voltage regulator provides with constant positive output voltage. All those IC's in the 78XX series are fixed positive voltage regulators. In the IC nomenclature – 78XX ; the part XX denotes the regulated output voltage the IC is designed for. Examples:- 7805, 7806, 7809 etc.

A negative fixed voltage regulator is same as the positive fixed voltage regulator in design, construction & operation. The only difference is in the polarity of output voltages. These IC's are designed to provide a negative output voltage. Example:- 7905, 7906 and all those IC's in the 79XX series.

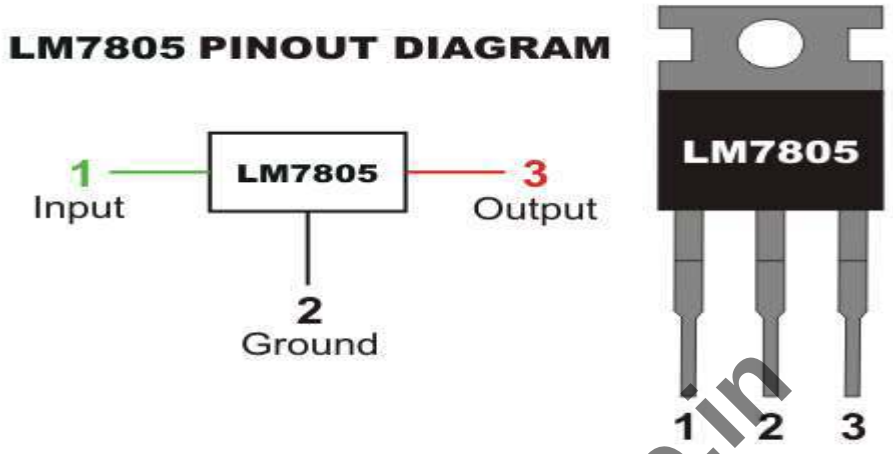
Regulated Power Supply Circuit

The **voltage regulator 7805** and the other components are arranged in the circuit as shown in figure.



The purposes of coupling the components to the IC7805 are explained below. C_1- It is the bypass capacitor, used to bypass very small extent spikes to the earth. C_2 and C_3- They are the filter capacitors. C_2 is used to make the slow changes in the input voltage given to the circuit to the steady form. C_3 is used to make the slow changes in the output voltage from the regulator in

the circuit to the steady form. When the value of these capacitors increases, stabilization is enlarged. But these capacitors single-handedly are unable to filter the very minute changes in the input and output voltages. C_4- like C_1, it is also a bypass capacitor, used to bypass very small extent spikes to the ground or earth. This is done without influencing other components.



Module 2 : FET and SCR.

Field Effect Transistor [FET]

- FET is a three terminal voltage controlled device. Three terminals of FET are Drain (D), Source (S) and Gate (G).
- Output Current I_D is a function of input voltage V_{GS}.
- FET is an unipolar device depending solely on either electrons (n-channel) or holes (p-channel).

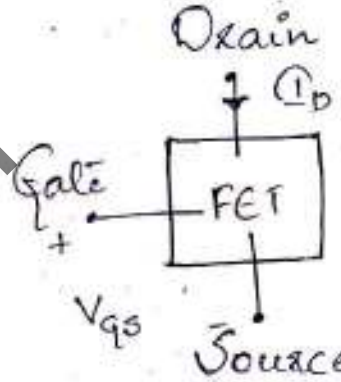


Fig:- FET Voltage Controlled Amplifier

- Electric field established by charges, controls the conduction path of output circuit without the need for direct contact between controlling and controlled quantities, hence the name FIELD EFFECT TRANSISTOR.
- FETs have high input impedance (range of 100MΩ)
- FETs are more temperature stable.
- Smaller in size, particularly useful in ICs.

Based on construction, types of FET:

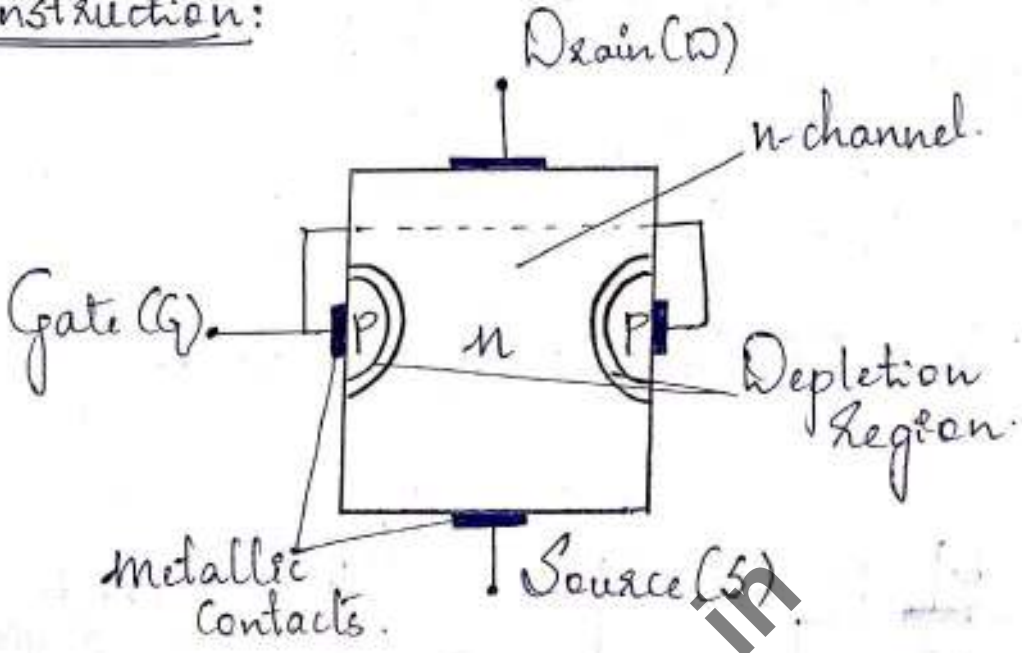
1. JFET → Junction Field Effect Transistor
2. MOSFET → Metal Oxide Semiconductor Field Effect Transistor.
   - ↳ Depletion-type MOSFET
   - ↳ Enhancement-type MOSFET

Differences between BJT and FET

BJT	FET
• Current Controlled device.	• Voltage Controlled device.
• Low input impedance.	• Very high input impedance.
• Bipolar device.	• Unipolar device.
• High Voltage Gain.	• Low voltage Gain.
• Low Current Gain.	• High Current Gain.
• Robust	• Easily damaged.
• less expensive.	• Expensive than BJT.
• Medium Noise Generation	• Low noise Generation.

JFET: Construction and Operation.

Construction:



Fig(a): n-channel JFET.

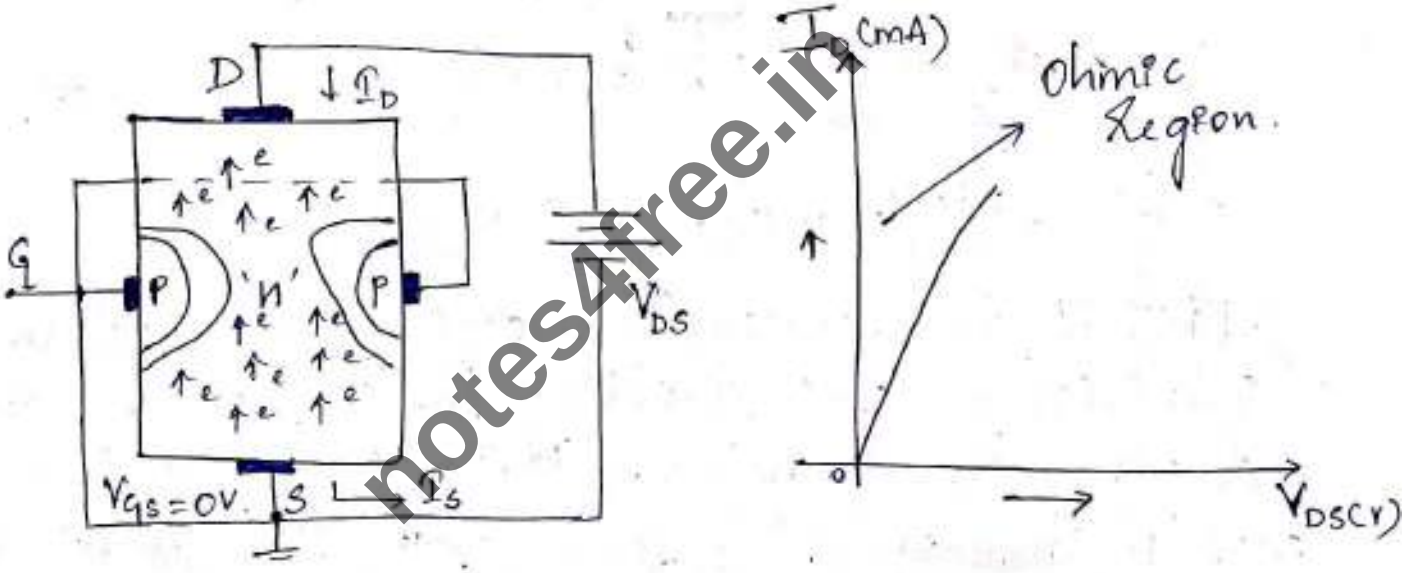
JFET is a three terminal device with one-terminal [gate] capable of controlling the current between the other two terminals. Majority of the structure has 'n' type material forming the channel between two embedded layers of p-material.

Top of the n-type channel is connected through metallic contact to a terminal called DRAIN(D). Lower end of n-channel is connected through the metallic contact to a terminal called SOURCE(S). Two p-type materials are connected together and to a terminal called Gate(G).

In the absence of applied potentials, JFET has two p-n junctions under no-bias conditions. Result is a depletion region at each junction just like in diodes which do not support conduction as they are void of free carriers.

Operation/Characteristics:-

Case i): $V_{GS} = 0V$; V_{DS} = Some positive value.



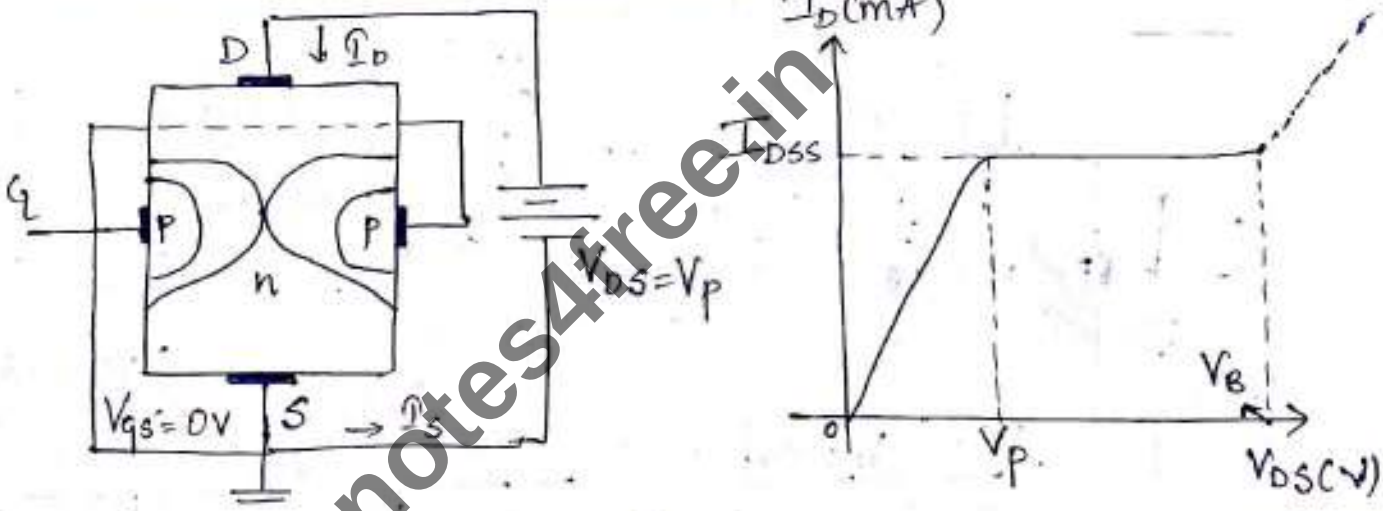
Fig(b): JFET Set-up for case (i) and its drain characteristics.

Gate is connected directly to source to establish $V_{GS}=0V$. A positive voltage V_{DS} is applied across channel. Since p-n junction is reverse biased, gate current $I_G = 0A$. When voltage V_{DS} is applied, electrons are drawn from channel to drain terminal, establishing current $I_D = I_S$.

Higher the positive voltage applied across drain and source, more will be the drain current I_D.

$\therefore I_D \propto V_{DS}$ which obeys law, hence when $V_{DS} > 0$ till certain voltage, JFET Resistance is said to be constant, and this region is called as ohmic region.

Case (ii): $V_{GS} = 0V$; $V_{DS} \geq V_p$

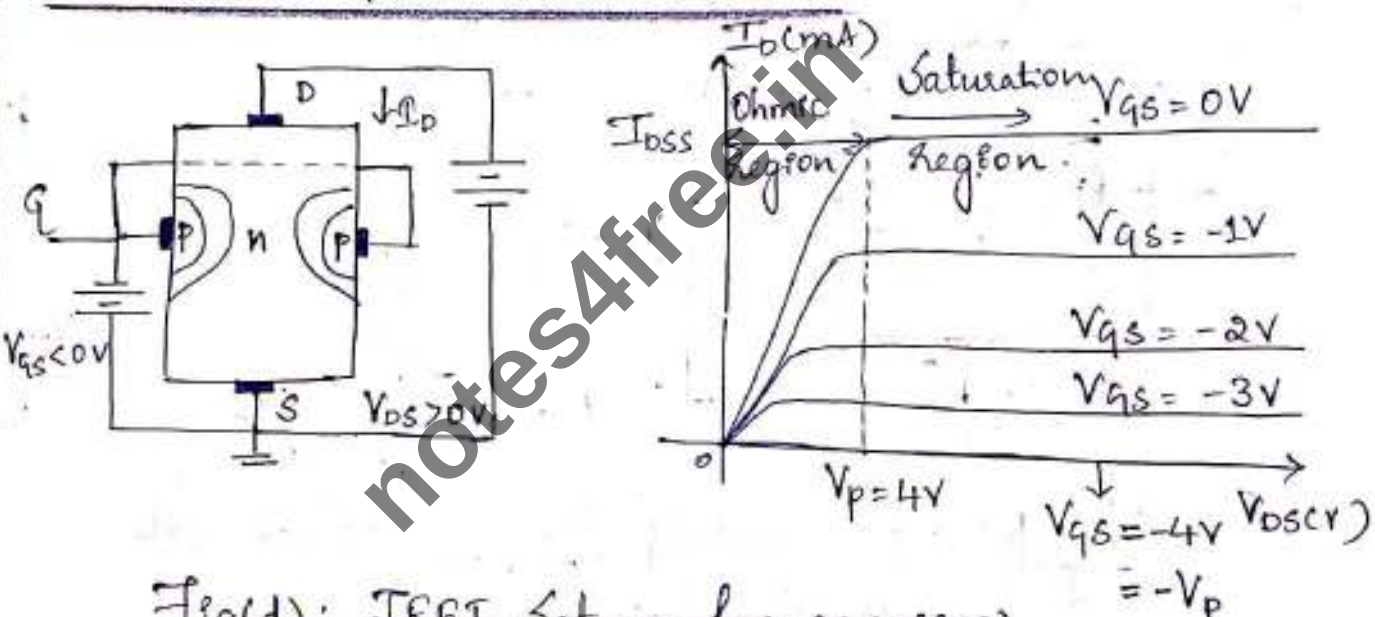


Fig(c): JFET set-up for case (ii) and its drain characteristics

'n' channel region towards the drain terminal is more reverse biased than the region near source terminal. Hence depletion region is wider near the top of n-channel, because more is the reverse biased voltage, wider is the width of depletion region.

When V_{DS} is equal to a voltage referred to as pinch-off voltage V_p, the two depletion regions meet and current I_D reaches its maximum value I_{DSS}. $\forall\ V_{DS} \geq V_p$ but $V_{DS} \leq V_B$, $I_D = I_{DSS}$, JFET behaves like a current source. When $V_{DS} \geq V_B$ where V_B = Breakdown Voltage, the JFET is damaged because current is abruptly increased.

Case (iii): $V_{GS} < 0V$; $V_{DS} > 0V$.



Fig(d): JFET Set-up for case(iii) and its drain characteristics

When negative voltage is applied to gate, holes in 'p' doped regions are drawn towards gate terminal which widens the width of depletion region. Hence as negative V_{GS} is increased, drain current is decreased. At $V_{GS} = -V_p$, I_D reduces to zero.

Pinch-off voltage V_p can be defined in terms of two voltages, V_{DS} and V_{GS}.

1) V_p is that value of V_{DS}, at which $I_D = I_{DSS}$
2) V_p is that value of V_{GS}, at which $I_D = 0$

Generally V_p is defined in terms of V_{GS}. Hence,
- V_p is negative for n-channel JFET.
- V_p is positive for p-channel JFET.

JFET Drain Characteristics

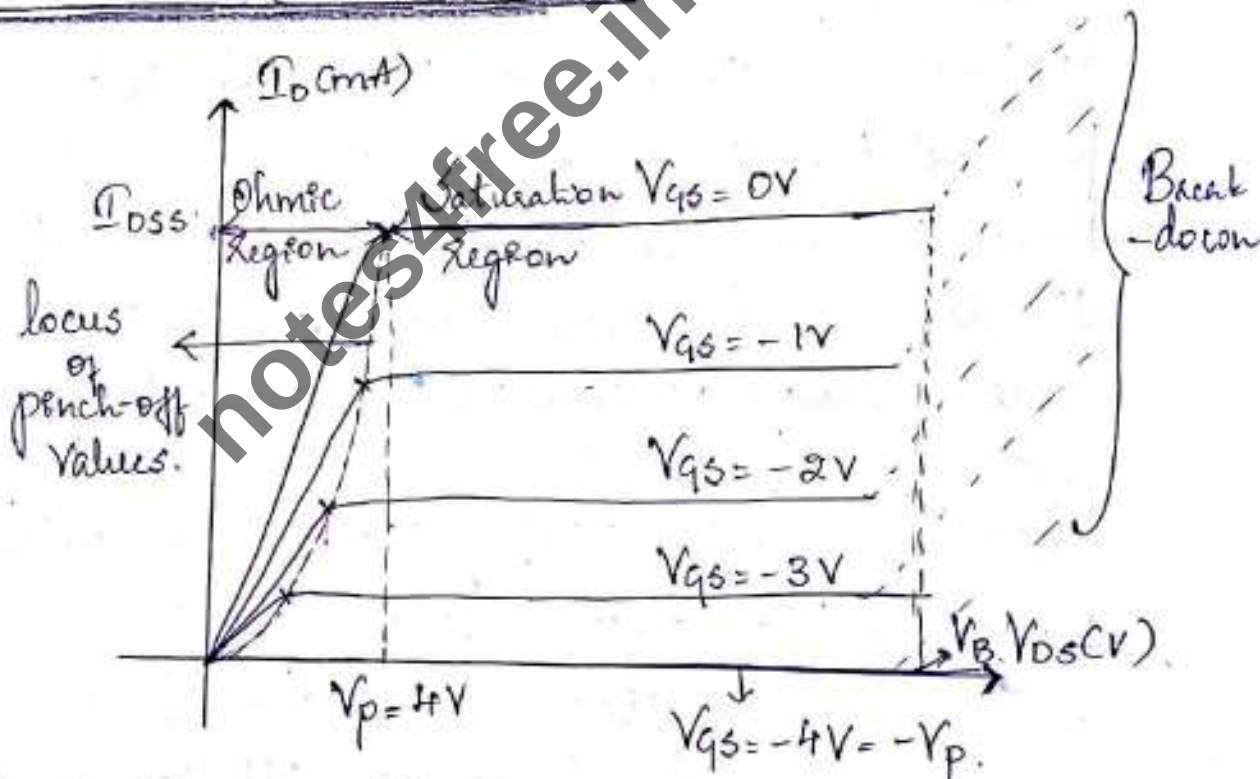


Fig:- Drain or Output Characteristics of JFET.

Drain/output characteristics is a graph of drain/output current I_D versus drain/output voltage V_{DS}.
I_D in terms of mA. V_{DS} in terms of Volts.

It explains the variation of output current I_D for increasing values of V_{DS}, output voltage. As seen in the graph, for increasing value of V_{DS}, I_D increases. This region is called ohmic region, since it obeys ohms law with evidently constant resistance. At $V_{DS} = V_p$, I_D reaches its maximum value I_{DSS} with $V_{GS} = 0V$. For $V_{DS} \geq V_p$, $V_{DS} \leq V_B$, $I_D = I_{DSS}$.

If V_{DS} is varied with negative values of V_{GS}, I_D is observed to be less than I_{DSS}. For increasing negative potential V_{GS}, I_D goes on decreasing. At $V_{GS} = -V_p$, I_D becomes zero. In the graph, for $V_{DS} = +1V$, I_D reaches its maximum value I_{DSS}. Hence pinch-off voltage $V_p = +1V$. Hence for $V_{GS} = -1V$, I_D reduces to zero. Region to the right of pinch-off locus is called as constant current / saturation region

Transfer Characteristics: Transfer curve is the graph plotted with Output current I_D in Y-axis versus Input voltage V_{GS} in X-axis. I_D in terms of mA, V_{GS} in terms of volts. It can be obtained by two ways,

1) By using square law expression of I_D.
2) From drain characteristics.

1) By using Square law expression of I_D:-

The Square law expression of I_D is given by,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2,$$

where I_D = Drain Current (mA)

I_{DSS} = Saturation Drain Current (mA)

V_{GS} = Input Voltage (V)

V_p = Pinch-off Voltage (V) { +ve → p channel JFET; -ve → n channel JFET }

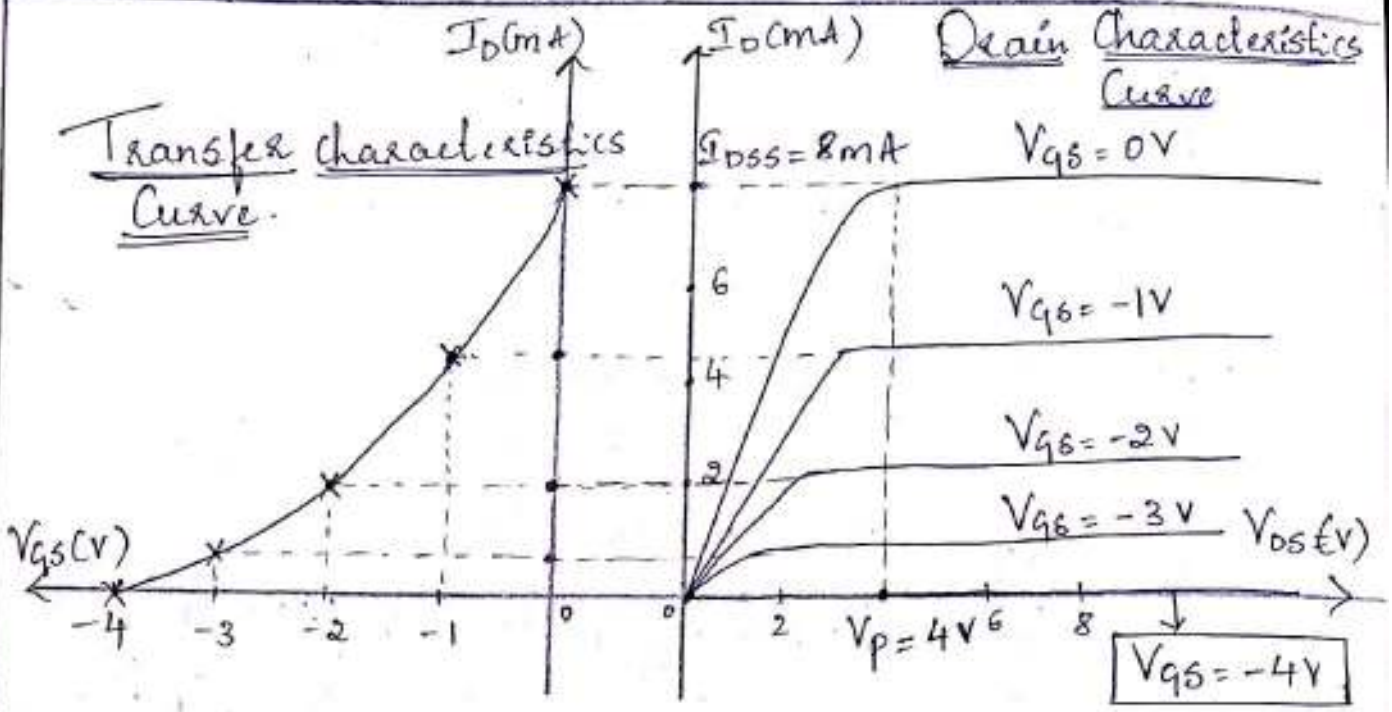
For a JFET, I_{DSS} and V_p are constant values. Hence I_D can be found for given values of V_{GS} to plot the transfer curve.

2) From the drain characteristics:-

In this method, to derive the transfer curve, drain/output characteristics curve should be obtained first. Drain Characteristics show the level of output current I_D for increasing values of V_{DS} for a constant value of V_{GS}. By extending the current I_D value from first quadrant to second quadrant, transfer curve can be obtained.

To draw the transfer curve, assumed values are: $I_{DSS} = 8mA$; When $V_{DS} = 4V$.

Hence $V_p = 4V$ of V_{DS} or $-4V$ of V_{GS}.



JFET Symbols

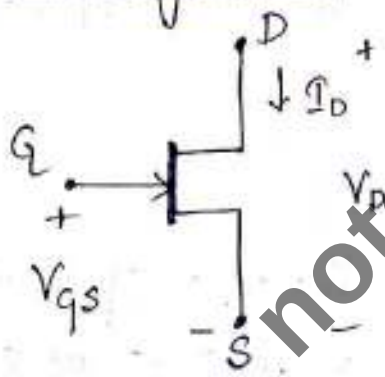


Fig:- n-channel JFET Symbol

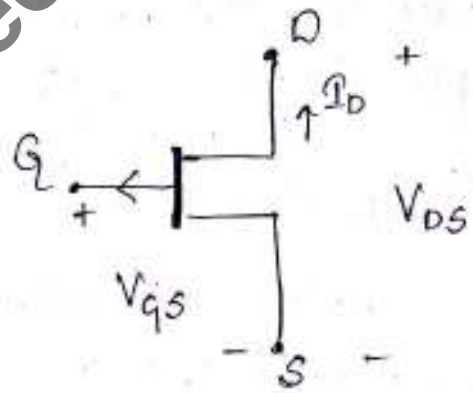


Fig:- p-channel JFET Symbol

Square Law Expression of I_D: It is given by,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$ where,

I_D = Drain Current (mA)

I_{DSS} = Saturation Drain Current (mA)

V_{GS} = Applied negative voltage to Gate of the n-channel JFET. (V) [If $V_{GS} < 0V$].

V_p = Value of V_{GS} for which $I_D = 0A$.

This expression is also called as 'SHOCKLEY'S EQUATION'. It relates output current and controlling parameter, which is Input Voltage. It can be seen that I_D is related to V_{GS} by a non-linear equation.

When $V_{GS} = 0V$,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = I_{DSS}(1-0)^2$$

$$\therefore \underline{I_D = I_{DSS}}$$

When $V_{GS} = V_p$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = I_{DSS}\left(1 - \frac{V_p}{V_p}\right)^2$$

$$\therefore \underline{I_D = 0A}$$

JFET Input Resistance: Input Resistance of JFET is expressed as, $R_{in} = \frac{|V_{GS}|}{|I_{GSS}|}$ ohms. R_{in} is usually very high (in range of MΩ), since $I_{GSS} \approx 0A$. I_{GSS} is of very negligible value because the channel is Reverse biased. I_{GSS} → Gate Reverse Current.

MOSFET : Stands for Metal Oxide Semiconductor Field Effect Transistor. There are two types:

1) Enhancement type MOSFET (EMOSFET)
2) Depletion type MOSFET (DMOSFET).

Enhancement - type MOSFET:-

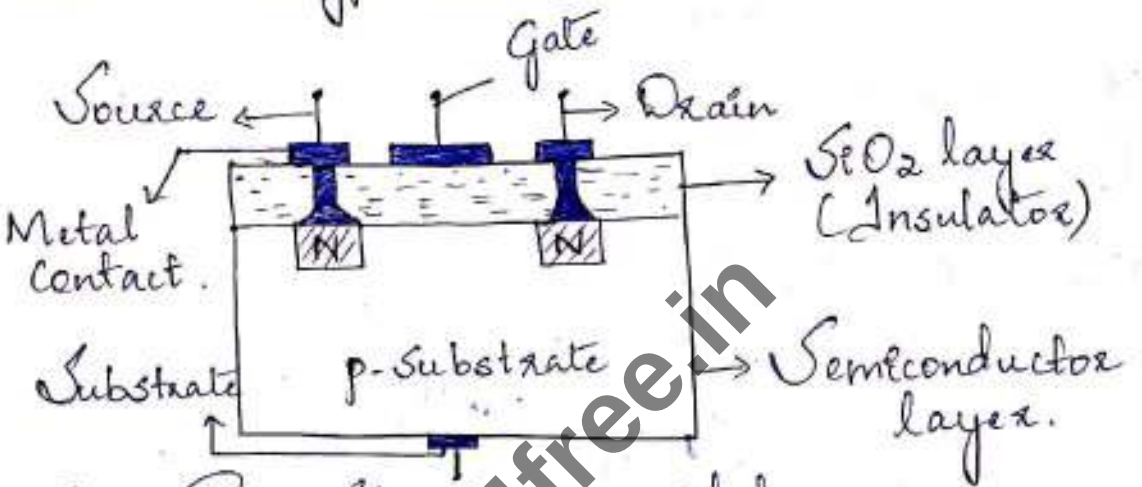


Fig:- Basic Structure of N channel EMOSFET

Construction: Basic structure of n-channel EMOSFET is shown in the above fig. A slab of p-type material is formed from a silicon base to form Substrate. Substrate is internally connected to Source. Drain and Source are connected through metallic contacts to n-doped regions. There is no channel present between the two n-doped regions.

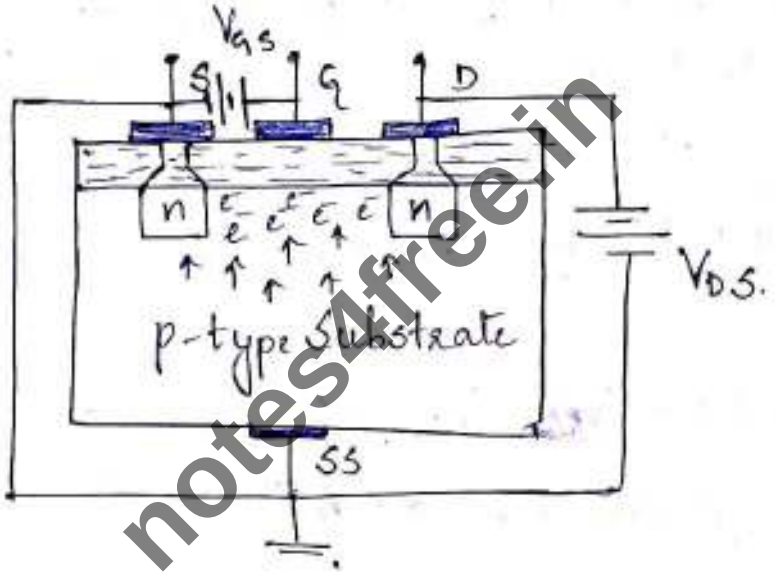
Gate is also connected to a metal surface, but it is isolated from p-type substrate by a thin layer of Silicon dioxide (SiO_2). Hence MOSFET is also called as Isolated Gate Field Effect Transistor (IGFET).

Characteristics or Operation:

Case (i): $V_{GS} = 0V$; V_{DS} = +ve Voltage.

Since there is no channel present between the n-doped regions, no output current I_D is present for any positive voltage V_{DS} as long as V_{GS} remains at zero volts.

Case (ii): V_{GS} = +ve voltage ; V_{DS} = +ve voltage.



When positive voltage V_{GS} is applied, the electrons present in p-type material (as minority charge carriers) are drawn towards the insulating SiO_2 layer, which doesn't absorb electrons. As applied V_{GS} is increased, the density of electrons present in between the two n-regions increases. At some point, the density of electrons is enough to act as a channel. The maximum value of V_{GS} for which $I_D = 0$ is learned as Threshold Voltage, denoted by '$V_{GS(Th)}$' or 'V_T'.

$\forall V_{GS} > V_{GS(Th)}$; $I_D \neq 0$. Since there is no channel present but it is enhanced because of the applied voltage V_{GS}. Hence the name, Enhancement MOSFET.

Case (iii): V_{GS} = Constant at a voltage > V_T.

V_{DS} = +ve Voltage.

As V_{GS} is increased, I_D also increases. But, when V_{GS} is held constant at a value greater than V_T, I_D tends to decrease with increasing level of V_{DS}. It can be demonstrated with below assumptions. Assume V_{GS} to be constant at 8V.

WKT $V_{DG} = V_{DS} - V_{GS}$.

Vary V_{DS} from 2V to 5V,

when $V_{DS} = 2V$; $V_{DG} = 2 - 8 = -6V$

$V_{DS} = 3V$; $V_{DG} = 3 - 8 = -5V$

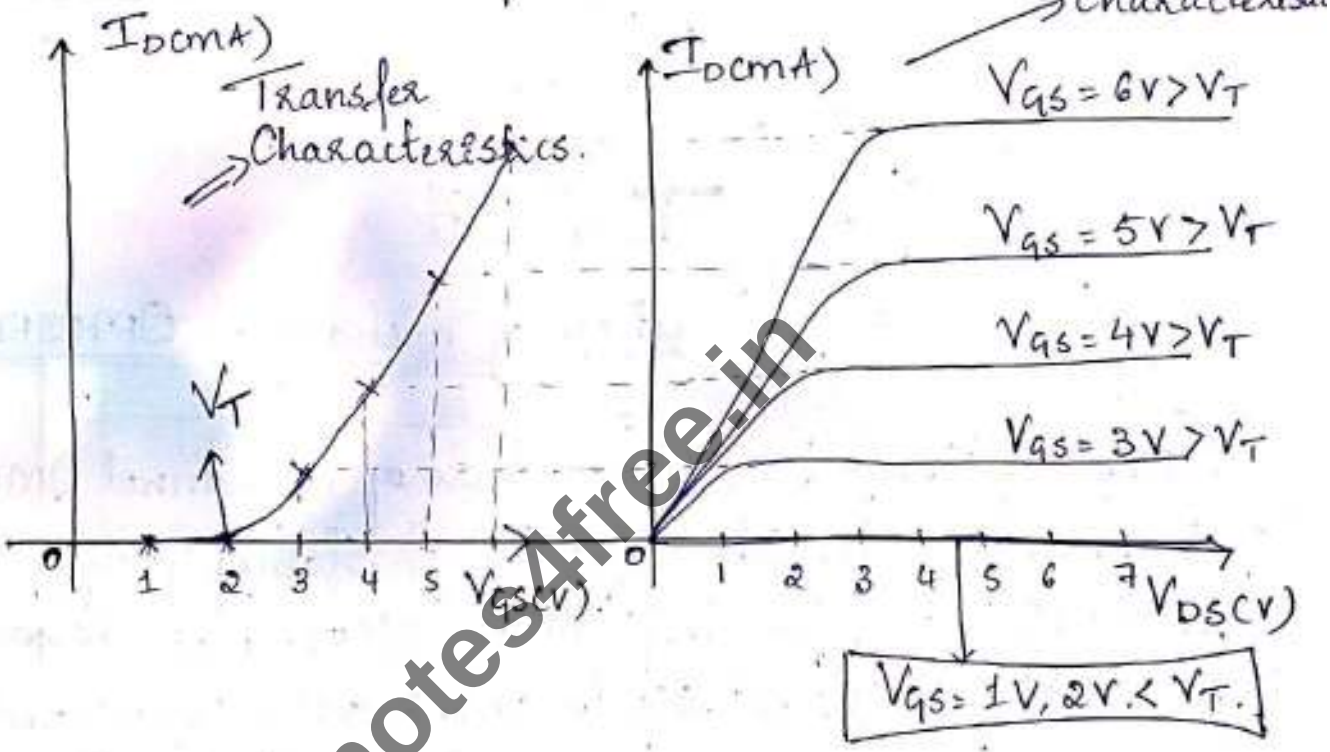
$V_{DS} = 4V$; $V_{DG} = 4 - 8 = -4V$

$V_{DS} = 5V$; $V_{DG} = 5 - 8 = -3V$.

It is observed that with constant V_{GS} and increasing V_{DS}, gate tends to become less positive with respect to drain. Lesser the positive voltage applied to gate, lesser will be the density of e^-s resulting in the formation of channel.

Hence, the output Current I_D, Stops increasing at a level of V_{DS}, called as $V_{DS(sat)}$, It is given by $V_{DS(sat)} = V_{GS} - V_T$.

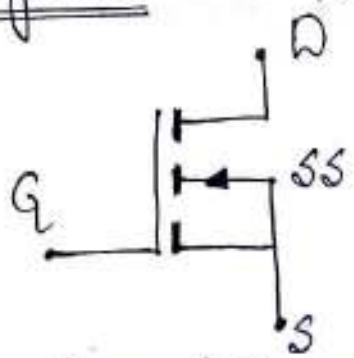
Drain and Transfer Characteristics.



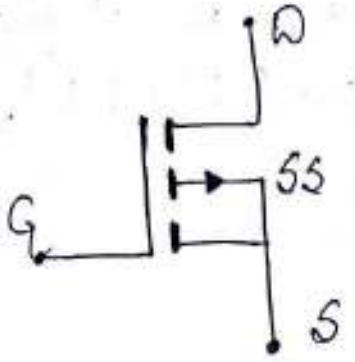
EMOSFET does not agree with Shockley's Equation. Instead, their characteristics are defined by,

$$I_D = k(V_{GS} - V_T)^2$$

Symbol:-



n-channel EMOSFET



p-channel EMOSPET.

Depletion-type MOSFET

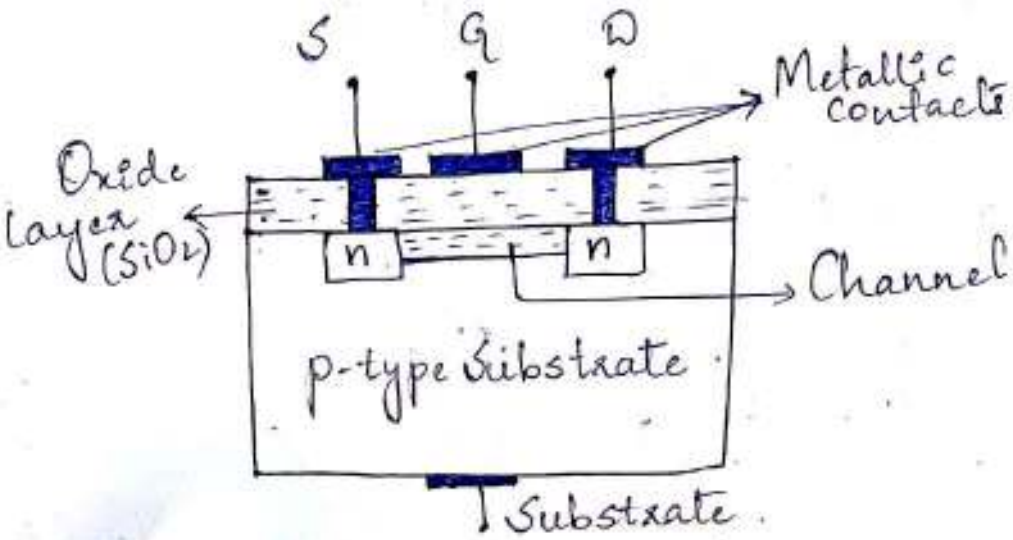


Fig:- Basic Structure of n-channel DMOSFET

Construction:- Basic structure of n-channel DMOSFET is shown in the above figure. A slab of p-type material is formed from a Silicon base to form a substrate. Substrate is internally connected to Source. Drain and Source are connected through the n-channel. Gate is also connected to a metal surface, but it is isolated from p-type substrate, by a thin layer of SiO_2. Hence MOSFET is also called as Isolated Gate Metal Oxide Semiconductor (IGFET).

Characteristics or Operation:

Case (i): $V_{GS} = 0V$; V_{DS} = +ve Voltage.

When positive voltage is applied to drain, due to presence of n-channel, electrons flow. Hence with increasing voltage V_{DS}, drain current I_D increases. In this region of drain characteristics, resistance remains effectively constant.

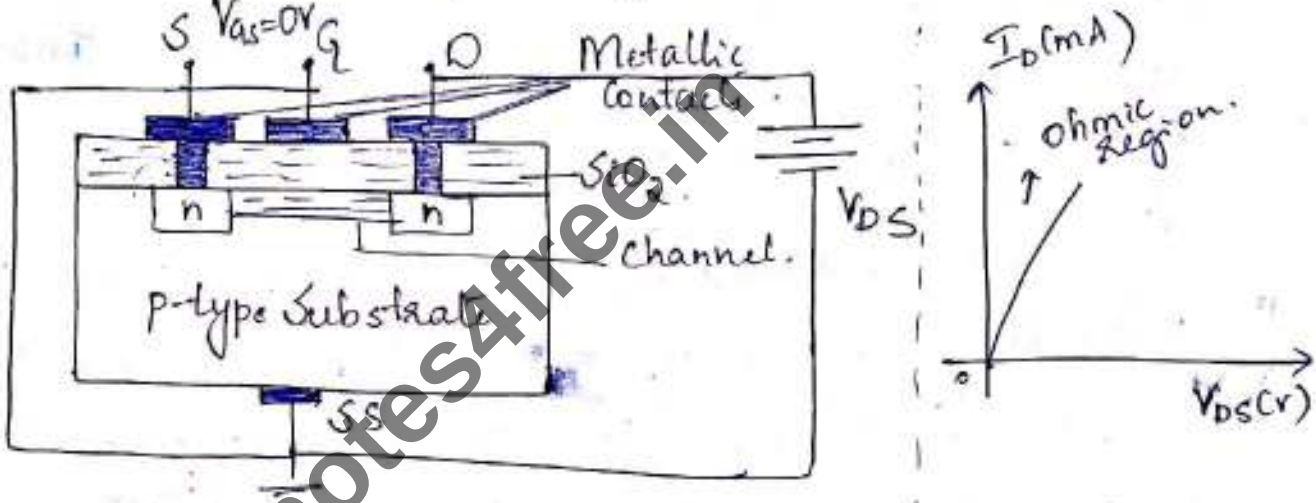


Fig:- Case (i) Set-up and its drain characteristics.

Case (ii) $V_{GS} = 0V$; V_{DS} = +ve Voltage $\geq V_p$.

. When $V_{DS} = V_p$, I_D reaches its maximum, value I_{DSS}. $\forall V_{DS} > V_p$, I_D remains constant at I_{DSS}. At $V_{DS} \geq V_B$, V_B - Breakdown Voltage, I_D increases suddenly, device breaks down. V_p is called as Pinch-off Voltage.

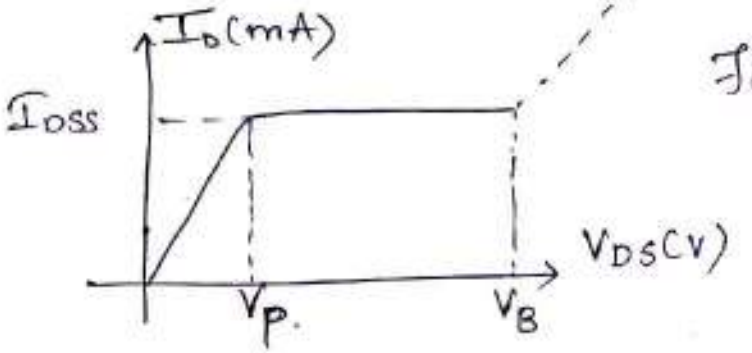


Fig:- Drain Characteristics for case (ii)

Case (iii) :- V_{GS} = -ve voltage ; V_{DS} = +ve voltage.

When negative voltage is applied to gate, electrons present in the 'n'-channel, are drawn towards the SiO_2 layer. The layer being insulator, does not absorb any charges. Hence the electrons of the channel are repelled towards the p-substrate. In the substrate, free electrons of channel combine with holes of p-substrate. This process is called Recombination. Hence greater the negative voltage applied to the gate, lesser will be the amount of drain current.

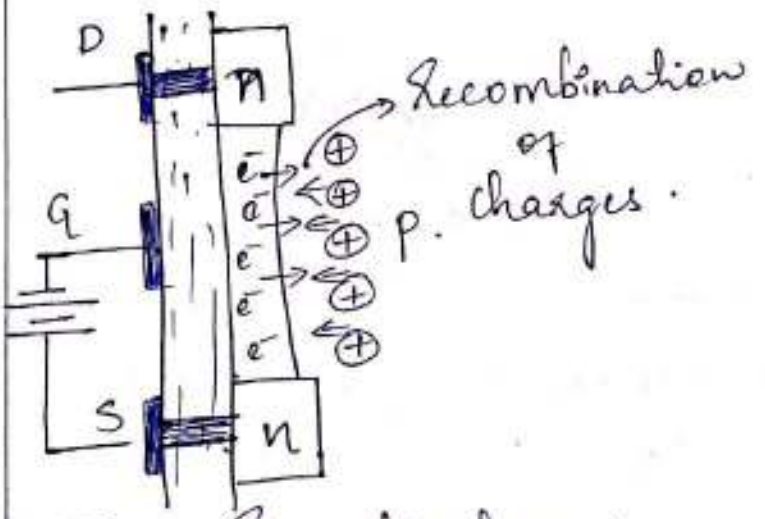
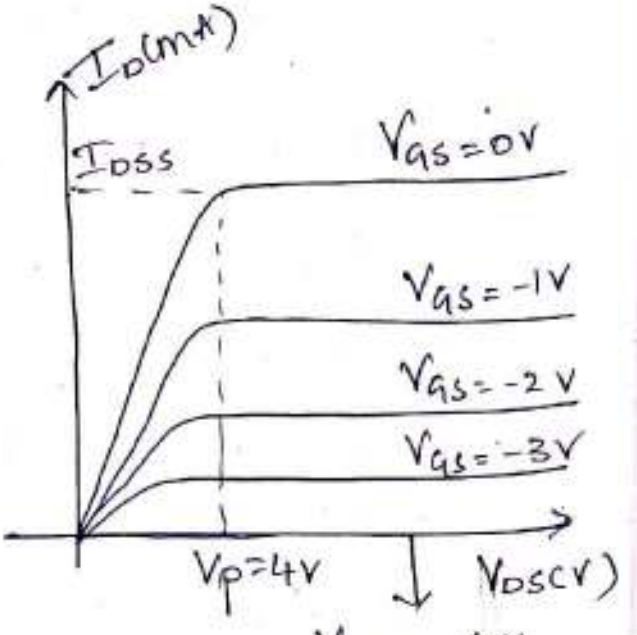


Fig:- Recombination of free charges.



Case (iv): V_{GS} = +ve Voltage; V_{DS} = +ve Voltage.

When positive voltage is applied to gate, electrons from p-substrate are drawn to the channel, increasing the number of free electrons in the channel. Hence drain current I_D increases above I_{DSS} for all positive voltages applied to gate.

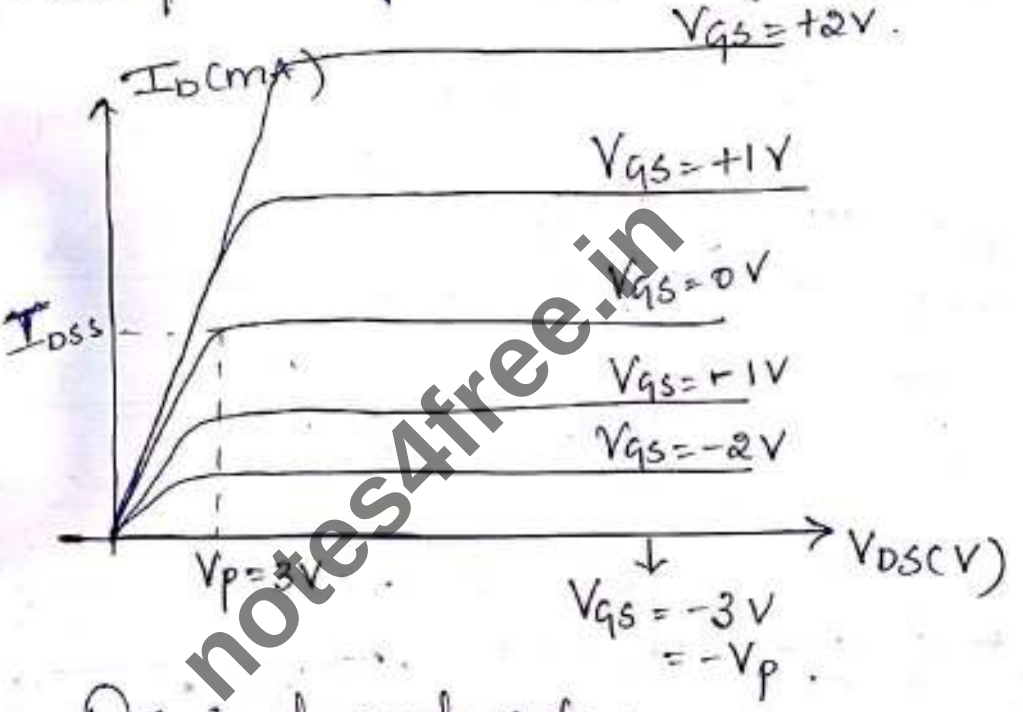


Fig:- Drain characteristics of n-channel DMOSFET

Transfer Characteristics:-

DMOSFETs obey Shockley's equation.

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$. Transfer curve can be obtained by 2 methods.

1) By Shockley's Equation
2) By drain characteristics.

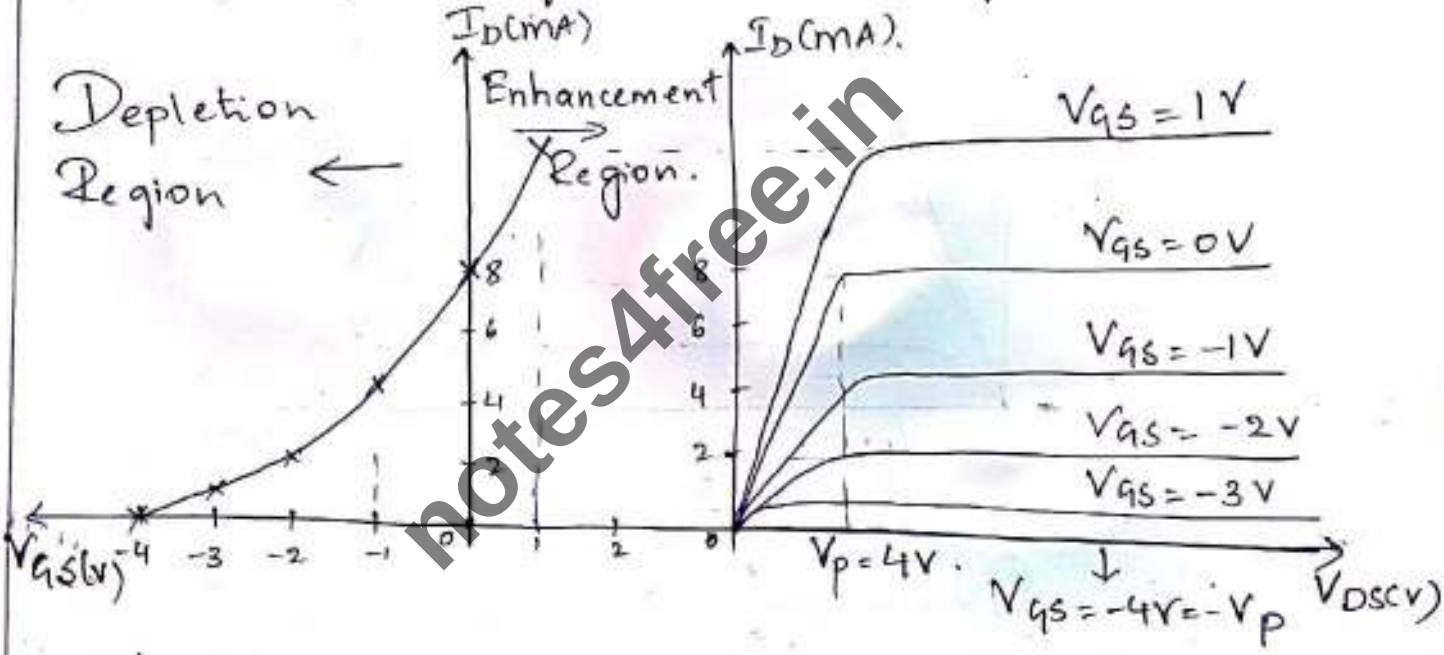
1) By using Shockley's Equation:-

For a DMOSFET, I_D values can be found for given values of V_{GS} to plot the transfer curve.

2) From the drain characteristics:-

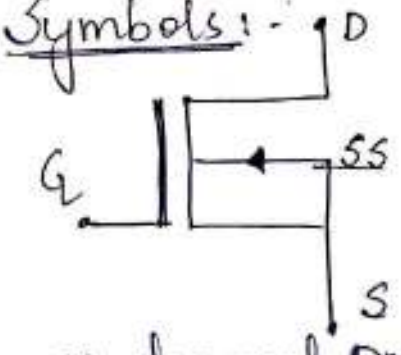
Assume, $I_{DSS} = 8mA$, when $V_{DS} = 4V$

$\therefore V_p = 4V$ of V_{DS} or $-4V$ of V_{GS}.

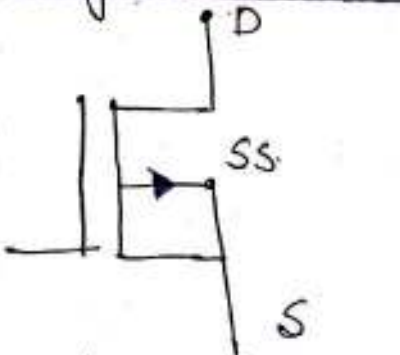


In transfer curve, the left portion is called as depletion region, the right portion is called as enhancement region.

Symbols:-



n-channel DMOSFET



p-channel DMOSFET

Complementary Metal Oxide Semiconductor (CMOS)

CMOS is a logic circuit which is a combination of P-channel MOSFET (PMOS) and N-channel MOSFET (NMOS). PMOS and NMOS are constructed on the same substrate.

One simple application of CMOS is an Inverter.

CMOS Inverter

CMOS Inverter is a logic circuit which inverts (or) complements the input. If the input is 0V (Logic 0), the output is +5V (Logic 1) and if the input is +5V (Logic 1), the output is 0V (Logic 0).

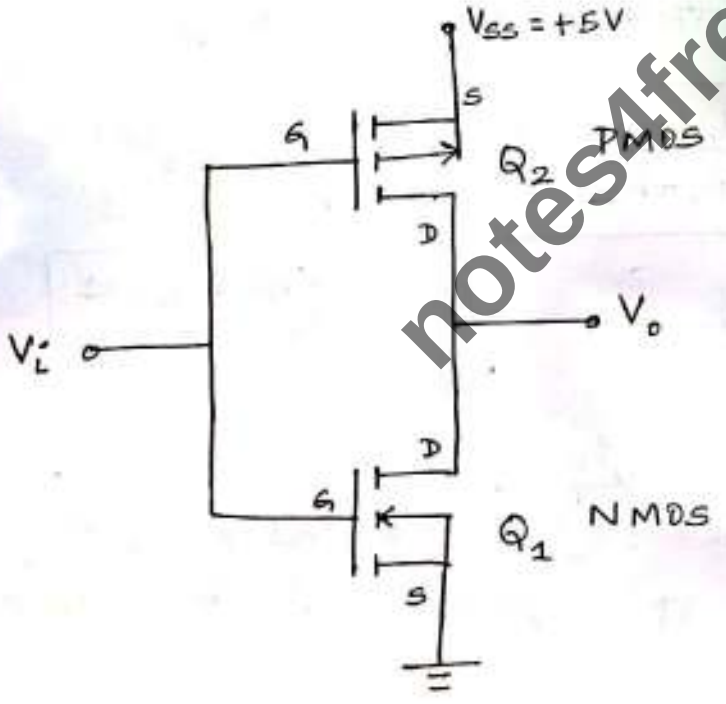


Fig: CMOS Inverter

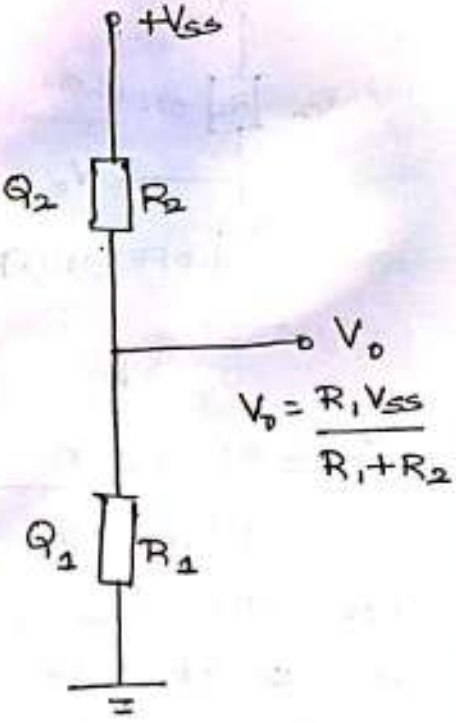


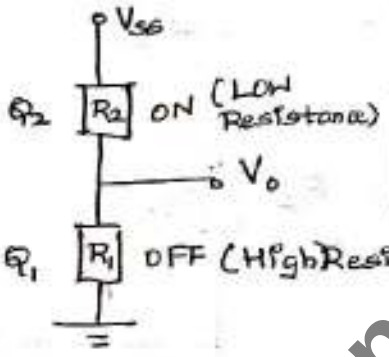
Fig: Equivalent circuit of CMOS

The source terminal of PMOS is connected to supply V_{SS} while the source terminal of NMOS is connected to ground. The gate terminals of PMOS & NMOS are shorted and it acts as input terminal. The drain terminals of PMOS & NMOS are shorted and it acts as output terminal.

NMOS operates with positive gate voltage and PMOS operates with 0V (or) negative gate voltage.

Case 1: When $V_i = 0V$ (Logic 0)

When $V_i = 0V$, PMOS (Q_2) is ON and NMOS (Q_1) is OFF. PMOS forms a short circuit and NMOS forms a open circuit.



The output voltage is voltage across R_1,

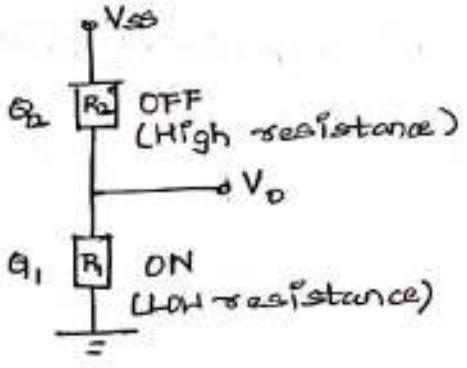
$$V_o = \frac{R_1 V_{SS}}{R_1 + R_2}$$

(or) $V_o = 5V$

V_o = Logic 1

Case 2: When $V_i = +5V$ (Logic 1)

When $V_i = +5V$, PMOS (Q_2) is OFF and NMOS (Q_1) is ON. PMOS (Q_2) forms a open circuits and NMOS forms a short circuit.



V_o is connected to ground directly.

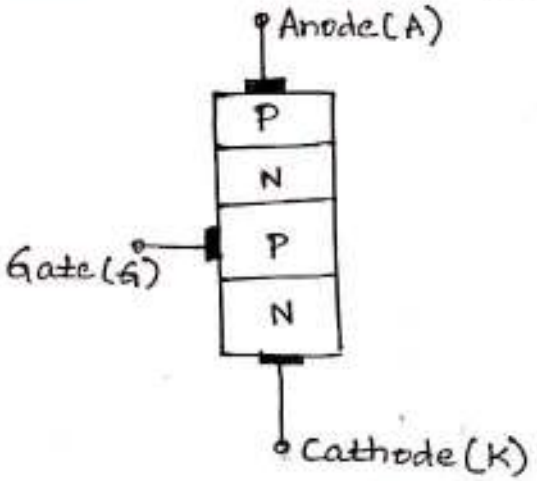
$\therefore V_o = 0V$ (or)

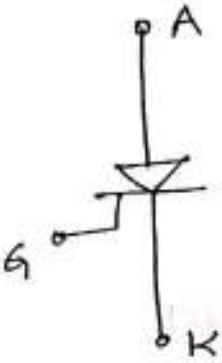
V_o = Logic 0

Silicon Controlled Rectifier (SCR)

Silicon Controlled Rectifier (SCR) is a switching device used in power control applications.

It is a four layered PNPN device with three terminals : Anode (A), Cathode (K) and Gate (G).





In OFF state, SCR acts as an open circuit between the anode and cathode. In the ON state, SCR ideally acts as a short circuit between the anode and the cathode.

The outer P and N layers are connected to terminals to form anode (A) and cathode (K), and the P-layer closer to cathode forms the terminal Gate (G).

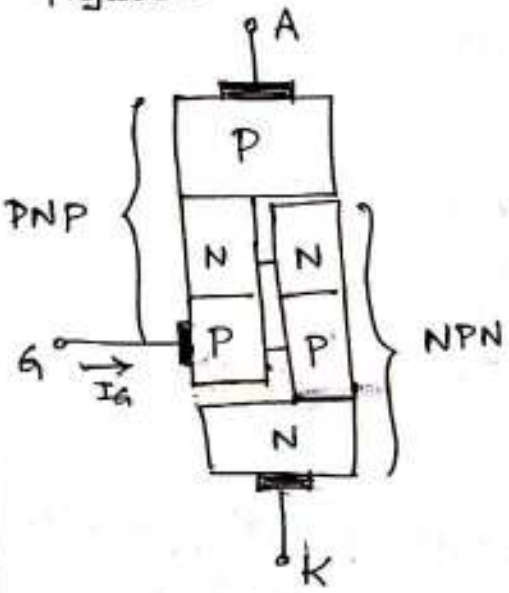
To turn ON the SCR, two conditions must be satisfied :

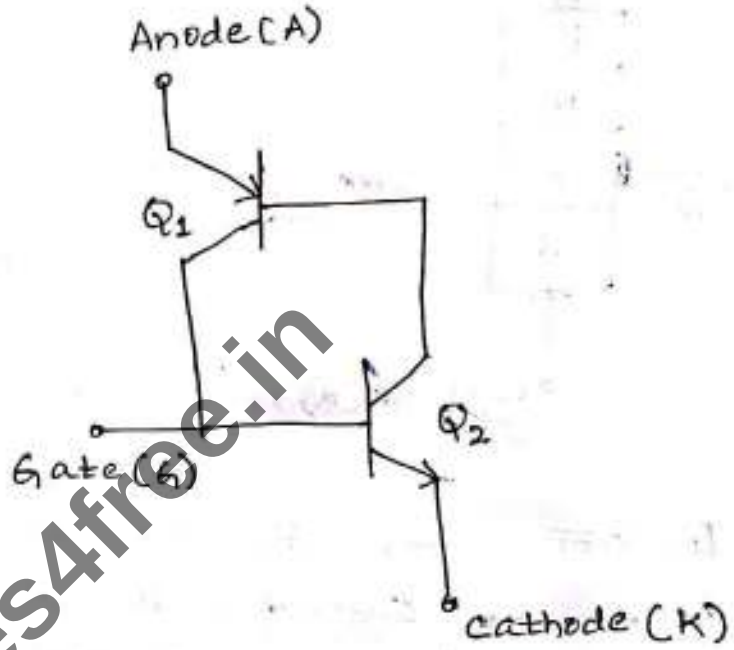
* Anode must be positive with respect to cathode.
* Gate pulse must be applied between gate and cathode.

Two transistor Model of SCR

The basic operation of the SCR can be explained by using two transistor model.

The four layered PNPN structure can be split into two three layered transistor structures as shown in the figure.





SCR comprises of two transistors:

→ PNP transistor (Q_1)

→ NPN transistor (Q_2)

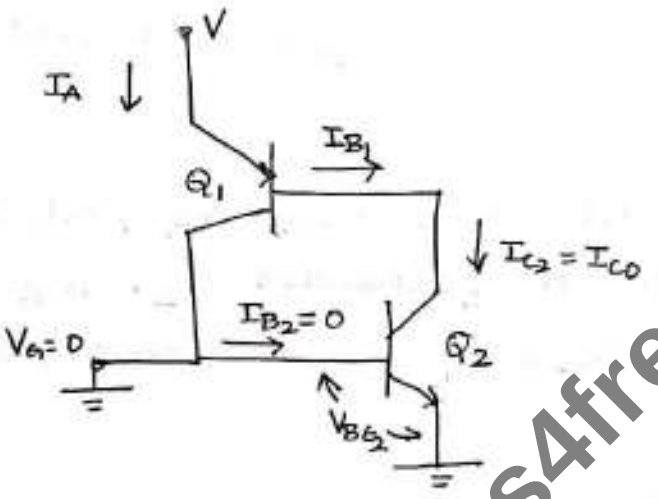
The base of PNP transistor is connected to collector of NPN transistor. The collector of PNP transistor is connected to the base of NPN transistor and the gate is connected to the base of NPN transistor.

Switching Action of SCR

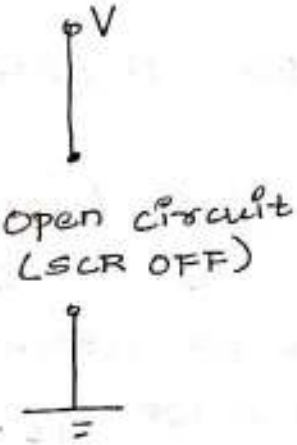
Let a positive voltage 'V' be applied to the anode(A) and the cathode (K) be grounded. Now, anode(A) is more positive with respect to cathode (K)

Turning ON and OFF of SCR depends on the application of gate pulse.

* OFF operation



(a) OFF state of SCR



(b) Switch OFF.

When V_G is grounded, $V_G = 0$.

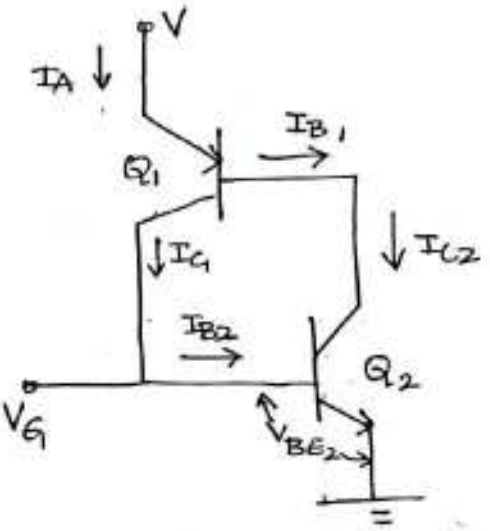
The current flowing into the base of Q_2, $I_{B_2} = 0$.

∴ The collector current, $I_{C_2} = I_{CO}$ (Leakage current)

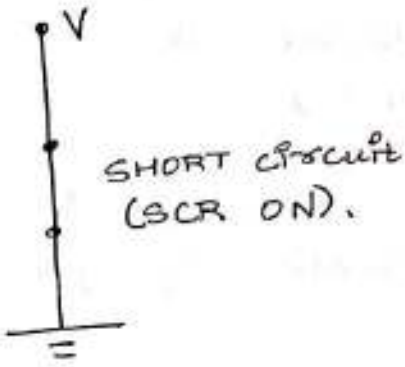
Since, $I_{B_1} = I_{C_2} = I_{CO}$, it is very small to turn ON Q_1.

i.e., When $V_G = 0$, both the transistors Q_1 and Q_2 are OFF. ∴ SCR acts as a OPEN circuit.

ON operation



(a) 'ON' State of SCR



(b) short circuit.

When V_G is sufficiently large, $V_{BE_2} = V_G$ and I_{B2} is large enough to turn ON transistor Q_2. The collector current of Q_2, $I_{C_2} = I_{B_1}$ which turns ON transistor Q_1.

Both the transistors Q_1 and Q_2 turns ON and the SCR acts as a short circuit.

Turn-OFF of SCR

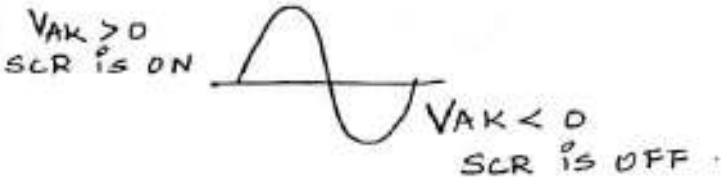
Once the SCR is turned ON, it remains in ON state even if gate signal is removed.

The mechanism of turning OFF of SCR is called Commutation.

Types: i) Natural Commutation / Line Commutation
ii) Forced commutation.

Natural / Line commutation

* In natural commutation, the SCR turns OFF when negative voltage appears across the SCR.
* The applied V_{AK} voltage is AC.
* No external circuits are required to turn off SCR.

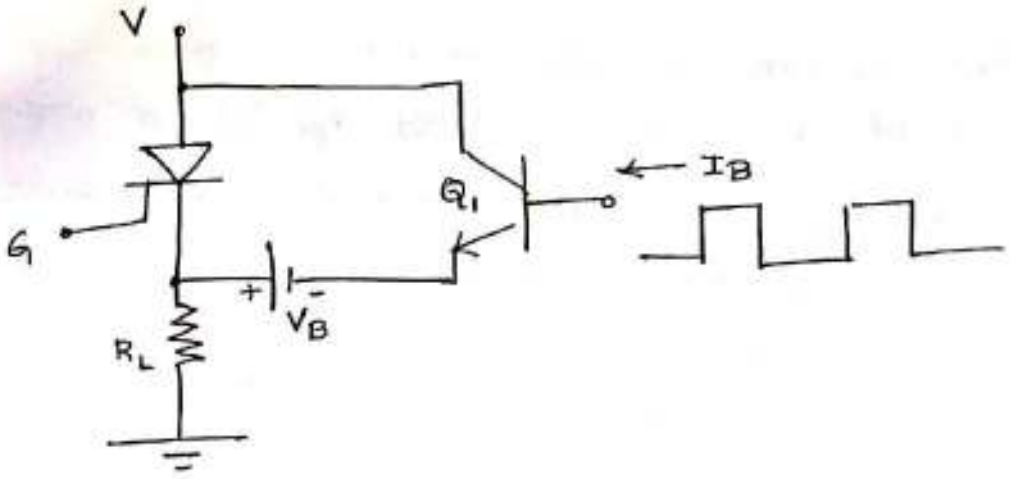


Forced commutation

* The applied V_{AK} voltage is DC & always $V_{AK} > 0$.
* External circuits are used to turn off SCR. These circuits are called commutation circuits.

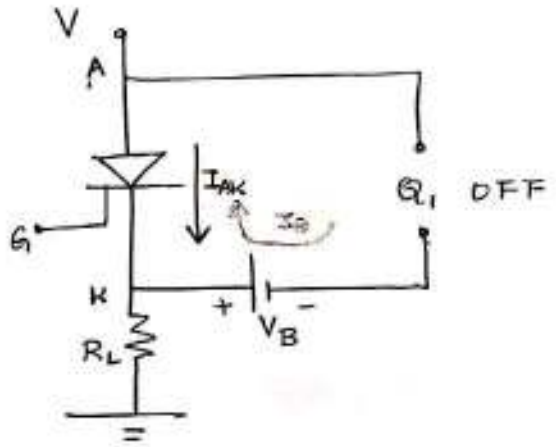
In forced commutation, the current through the SCR is forced to become zero by passing a current through it in the direction opposite to forward current.

A simple forced commutation circuit is as shown in fig.



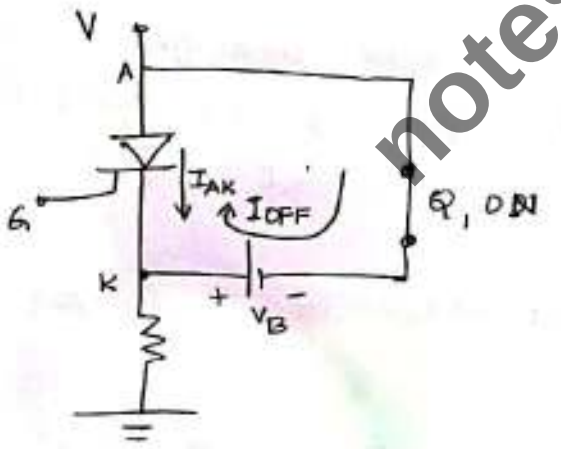
The turn-off circuit consists of NPN transistor Q_1, a dc battery V_B and a pulse generator.

When the SCR is ON, base drive is not applied. Transistor Q_1 is OFF & it acts as a open circuit.



Q_1 is OFF

To turn off the SCR, a positive pulse is applied to the base of the transistor Q_1. The transistor Q_1 turns ON and acts as a short circuit.

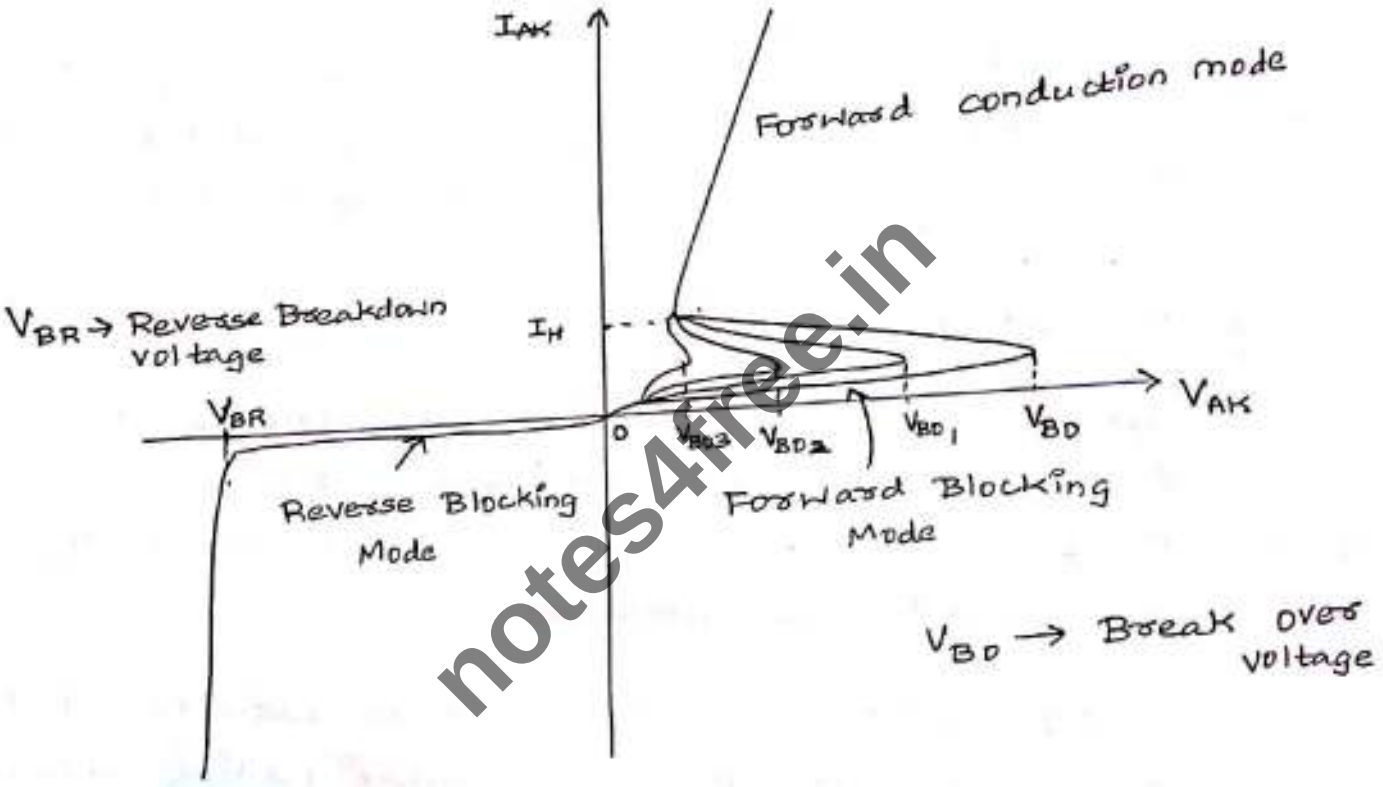


This short circuit provides a path for the flow of current from the battery V_B in reverse direction. This action forces the current to become zero & SCR is said to be OFF.

Characteristics of SCR

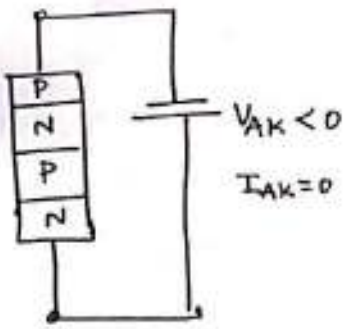
The VI characteristics of SCR can be explained in three regions of operation.

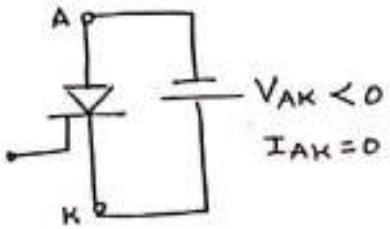
(i) Reverse Blocking region
(ii) Forward Blocking region.
(iii) Forward Conducting region.



Reverse Blocking Region / Reverse Blocking Mode

In this region, SCR is reverse biased and the SCR is said to be OFF.

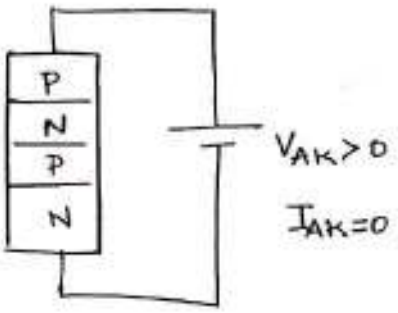


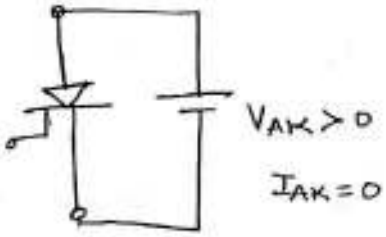


If the reverse bias voltage is increased above reverse breakdown voltage V_{BR}, high current flows through SCR & it gets damaged.

Forward Blocking Mode

In forward Blocking mode, the SCR is forward biased (i.e., $V_{AK} > 0$). But the SCR is in OFF state.





Reverse blocking mode and forward blocking mode corresponds to open circuit conditions (OFF state) which blocks the flow of current from anode to cathode.

Forward conduction Mode

Forward Breakover voltage is the voltage above which SCR enters the conduction region with the application of gate voltage. Once the SCR turns ON, V_{AK} decreases and I_{AK} increases.

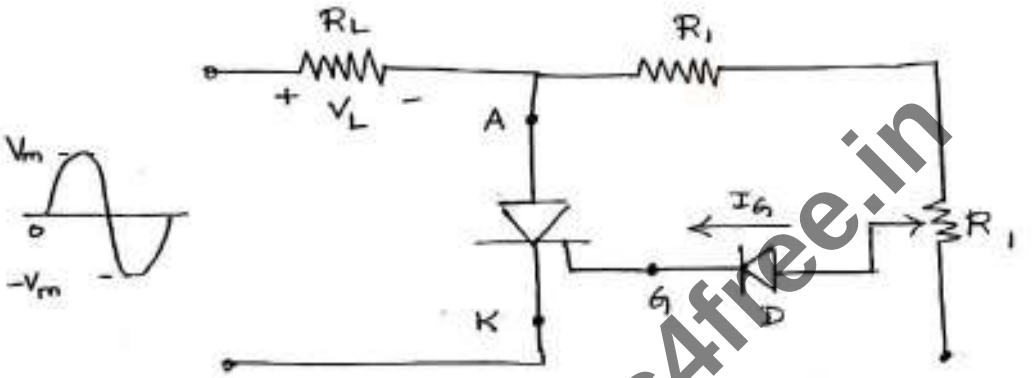
I_H - Holding current is the minimum current which keeps the SCR in ON state. and below holding current the SCR turns OFF. If the current is below holding current, the SCR switches from conduction state to forward blocking region. ($\because V_{AK} > 0$)

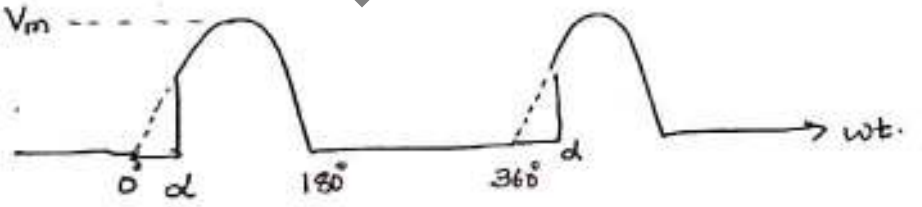
Applications of SCR

The applications of SCR includes power control, relay control, regulated power supplies, static switches, motor controls, choppers, inverters, heater controls etc.

→ Variable Resistance Phase Control

It is an application of SCR in which the power delivered to the load is controlled by controlling the rms value of the current.





The triggering circuit / firing circuit consists of a diode D, a fixed resistor R and variable resistor R_1. The combination of the resistors R and R_1 limits the gate current during positive cycle of the input voltage. The diode D blocks the voltage on gate during negative cycle of the input voltage.

The value of gate current can be varied by varying R_1. If R_1 is maximum, the gate current may not be sufficient to make SCR ON. The required gate current to turn ON SCR is obtained by varying R_1. Thus the conduction angle (α) of SCR can be varied from 0° to 90°. This operation is called 'half wave variable resistance phase control'.

Module-3

Operational Amplifier

The Operational Amplifier is a direct-coupled , high gain , negative feedback amplifier. It is nothing more than a differential amplifier which amplifies the difference between two inputs.

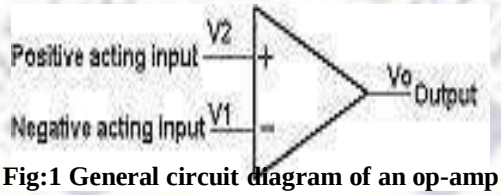


Fig:1 General circuit diagram of an op-amp

The terminal marked - is called the inverting terminal which means signal applied there will appear phase inverted at the output while the terminal marked + is called the non inverting terminal means that the signal applied here will appear in phase and applied at the output . Please understand that the - and + do not denote any type of voltage it means that output voltage is proportional to the difference of Non Inverting and inverting voltages which is Vo = V2 - V1 . When there is no feedback , no voltage or capacitor between output and input the op-amp is said to be in open loop condition .

Characteristics of an ideal op-amp

An Ideal Op-Amp has the following characteristics.

* An infinite voltage gain
* An infinite bandwidth
* An infinite input resistance: The resistance b/w V1 and V2 terminals is infinite .
* Zero output resistance: Vo remains constant no matter what resistance is applied across output .
* Perfect balance: When V1 is equal to V2 the Vo is 0 .

Single-Ended Input

Single-ended input operation results when the input signal is connected to one inputwith the other input connected to ground.

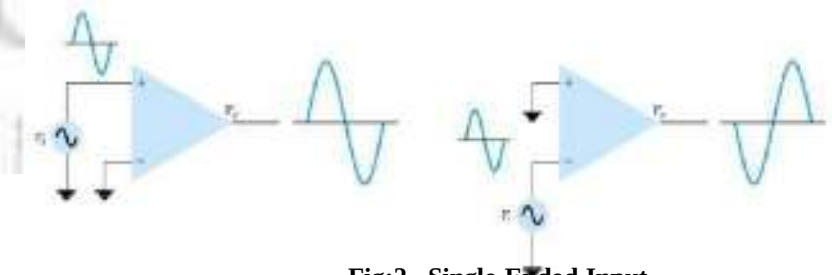


Fig:2 Single-Ended Input

Double-Ended Output

While the operation discussed so far had a single output, the op-amp can also be operated with opposite outputs, as shown in Fig2 . An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity. Figure 3 shows a single- ended input with a double-ended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. Figure 4 shows the same operation with a single output measured.

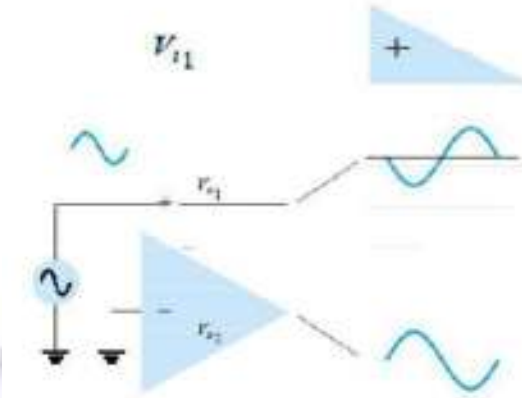


FIG.3 Double-ended output

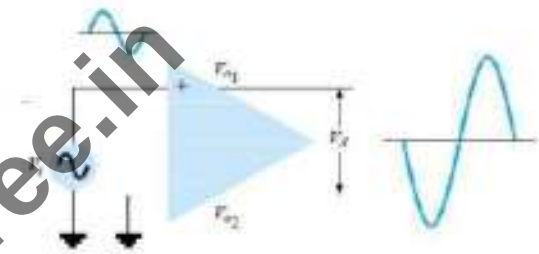


FIG.4 Double-ended output with single-ended input

Common-Mode Operation

When the same input signals are applied to both inputs, common-mode operation results, the two inputs are equally amplified, and since they result in opposite polarity signals at the output, these signals cancel, resulting in0-V output. Practically, a small output signal will result

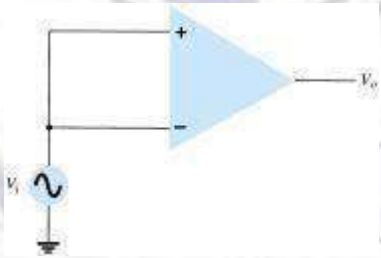


FIG.5 Common-mode operation

Common-Mode Rejection

A significant feature of a differential connection is that the signals which are opposite at the inputs are highly amplified, while those which are common to the two inputs are only slightly amplified—the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs.

DIFFERENTIAL AND COMMON MODE OPERATION

One of the more important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs, while only slightly amplifying signals that are common to both inputs. An op-amp provides an output component that is due to the amplification of the difference of the signals applied to the plus and minus inputs and a component due to the signals common to both inputs. Since amplification of the opposite input signals is much greater than that of the common input signals, the circuit provides a common mode rejection as described by a numerical value called the common-mode rejection ratio (CMRR).

Differential Inputs

When separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs.

$$V_d = V_{i_1} - V_{i_2}$$

Common Inputs

When both input signals are the same, a common signal element due to the two inputs can be defined as the average of the sum of the two signals.

$$V_c = \frac{1}{2}(V_{i_1} + V_{i_2})$$

Output Voltage

Since any signals applied to an op-amp in general have both in-phase and out-of phase components, the resulting output can be expressed as

$$V_0 = A_d V_d + A_c V_c$$

Where Vd = difference voltage given by Eq.
Vc = common voltage given by Eq.
Ad =differential gain of the amplifier
Ac = common-mode gain of the amplifier

Common-Mode Rejection Ratio

Having obtained Ad and Ac (as in the measurement procedure discussed above), we can now calculate a value for the common-mode rejection ratio (CMRR), which is defined by the following equation:

$$\text{CMRR} = \frac{A_d}{A_c}$$

The value of CMRR can also be expressed in logarithmic terms as

$$\text{CMRR (log)} = 20 \log_{10} \frac{A_d}{A_c} \quad \text{(dB)}$$

We can express the output voltage in terms of the value of CMRR as follows:

$$V_o = A_d V_d + A_c V_c = A_d V_d \left(1 + \frac{A_c V_c}{A_d V_d}\right)$$

$$V_o = A_d V_d \left(1 + \frac{1}{\text{CMRR}} \frac{V_c}{V_d}\right)$$

Basic of Op-Amp

The circuit shown provides operation as a constant-gain multiplier. An input signal, V1, is applied through resistor R1 to the minus input. The output is then connected back to the same minus input through resistor Rf. The plus input is connected to ground. Since the signal V1 is essentially applied to the minus input, the resulting output is opposite in phase to the input signal. Figure 6a shows the op-amp replaced by its ac equivalent

circuit. If we use the ideal op- amp equivalent circuit, replacing Ri by an infinite resistance and Ro by zero resistance, the ac equivalent circuit is that shown in Fig.6b. The circuit is then redrawn, as shown in Fig. 6c, from which circuit analysis is carried out.

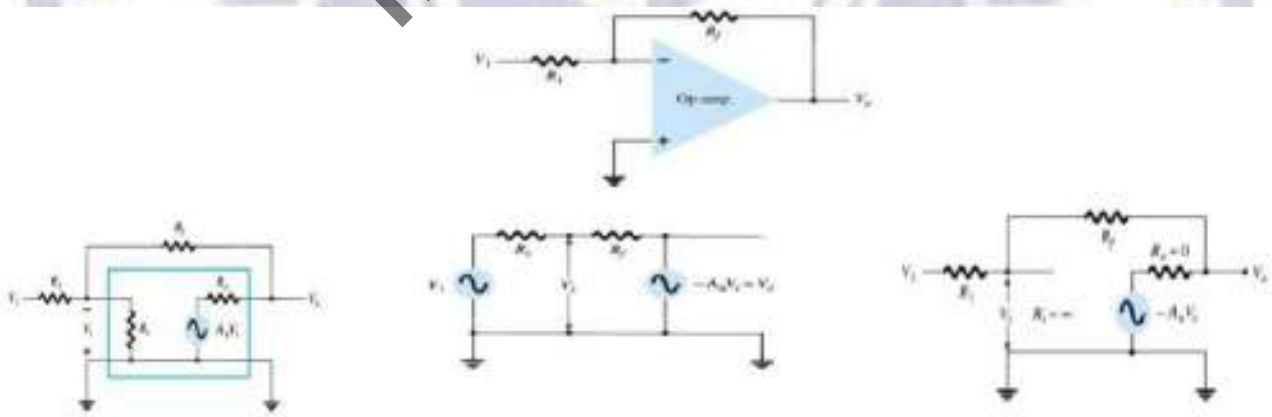


FIG.6.Operation of op-amp as constant-gain multiplier: (a) op-amp ac equivalent circuit; (b) ideal op-amp equivalent circuit; (c) redrawn equivalent circuit.

Using superposition, we can solve for the voltage V_i in terms of the components due to each of the sources. For source V_1 only (-A"V, set to zero).

$$V_{i1} = \frac{R_f}{R_1 + R_f} V_1$$

For ource $-A_v V_i$ only (V_i set to zero).

$$V_{i2} = \frac{R_1}{R_1 + R_f}(-A_v V_i)$$

The total voltage V_i is then

$$V_i = V_{i1} + V_{i2} = \frac{R_f}{R_1 + R_f} V_1 + \frac{R_1}{R_1 + R_f}(-A_v V_i)$$

which can be solved for V, as

$$V_i = \frac{R_f}{R_f + (1 + A_v)R_1} V_1$$

If $A_v \gg 1$ and $A_v R_1 \gg R_f$- a is usually true. then

$$V_i = -\frac{R_f}{A_v R_1} V_1$$

Solving for V_o/V_1. we get

$$\frac{V_o}{V_i} = \frac{-A_v V_i}{V_i} \qquad \frac{-A_v R_1 V_i}{V_i A_v R_1} \qquad \frac{R_f}{R_1} \frac{V_1}{V_i}$$

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

Unity Gain

If $R_f = R_1$. the

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

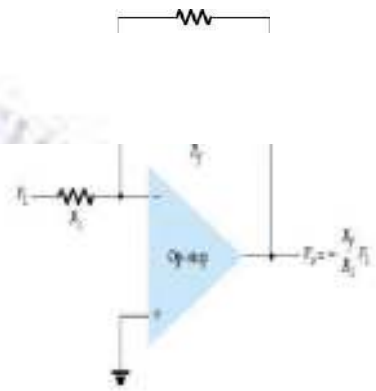
$$\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}$$

so that the circr
actly R_1. the vo

PRACTICAL OP-AMP CIRCUITS

Inverting Amplifier

The most widely used constant -gain amplifier circuit is the inverting amplifier, as shown. The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor (R1) and feedback resistor (Rf)—this output also being inverted from the input. Using Eq. (14.8) we can write



$$V_o = -\frac{R_f}{R_1} V_1$$

Noninverting Amplifier

The connection of Fig. 8shows an op-amp circuit that works as a noninverting amplifier or constant-gain multiplier. It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability (discussed later) . To determine the voltage gain of the circuit, we can use the equivalent representation shown in Fig. Note that the voltage across R_1 is V_1 since Vi =0 V. This must be equal to the output voltage, through a voltage divider of R1 and Rf, so that

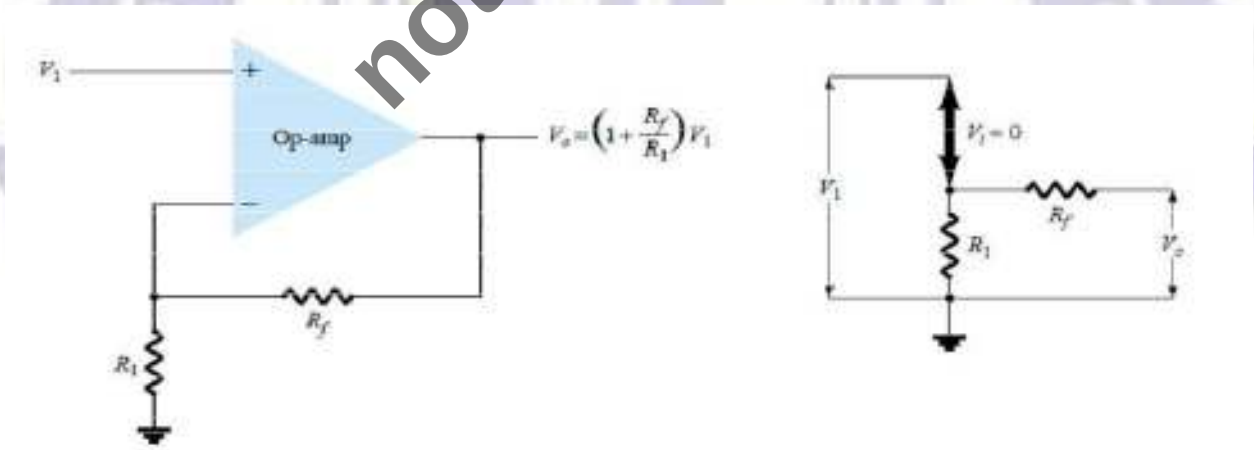


FIG.8.Noninverting constant-gain multiplier

Summing amplifier

The circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain factor. Using the equivalent representation shown in Fig. 9, the output voltage can be expressed in terms of the inputs as

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$$

In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier. If more inputs are used, they each add an additional component to the output.

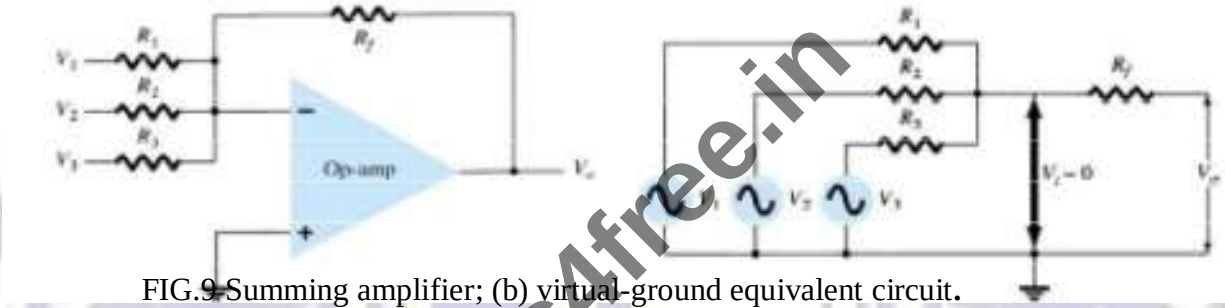


FIG.9 Summing amplifier; (b) virtual-ground equivalent circuit.

Subtractor:

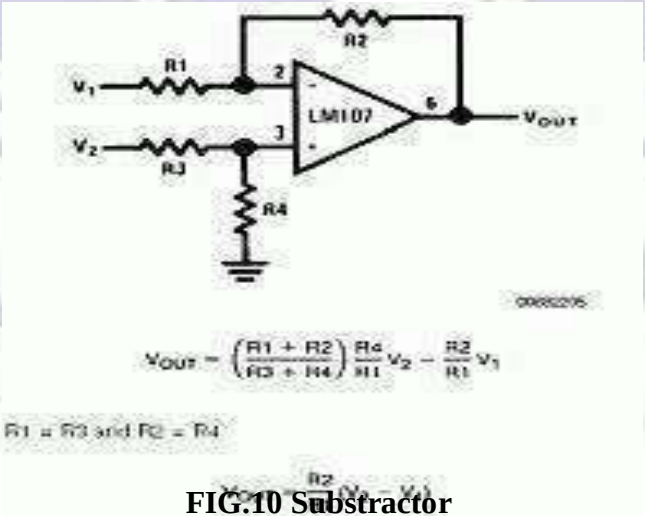


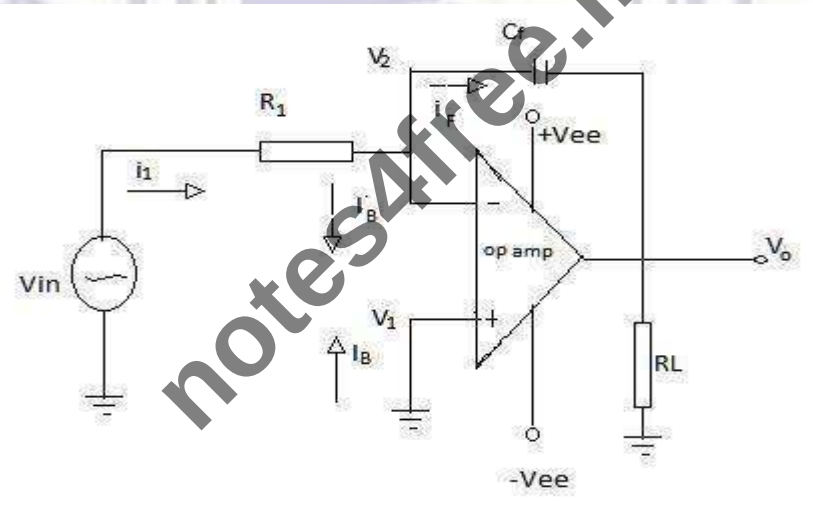
FIG.10 Substractor

The aim of the subtractor is to provide an output which is equal to the difference of the two input signals or proportional to their difference. For minimum offset error R1 || R2 = R3 || R4 .

Op-Amp as Integrator

The operational amplifier integrator is an electronic integration circuit. Based around the operational amplifier (op- amp), it performs the mathematical operation of integration with respect to time; that is, its output voltage is proportional to the input voltage integrated over time. The input current is offset by a negative feedback current flowing in the capacitor, which is generated by an increase in output voltage of the amplifier. The output voltage is therefore dependent on the value of input current it has to offset and the inverse of the value of the feedback capacitor. The greater the capacitor value, the less output voltage has to be generated to produce a particular feedback current flow.

Ideal circuit



The circuit operates by passing a current that charges or discharges the capacitor C_f during the time under consideration, which strives to retain the virtual ground condition at the input by off-setting the effect of the input current. Referring to the above diagram, if the op-amp is assumed to be ideal, nodes v_1 and v_2 are held equal, and so v_2 is a virtual ground. The input voltage passes a current v_{in}/R_1 .through the resistor producing a compensating current flow through the series capacitor to maintain the virtual ground. This charges or discharges the capacitor over time. Because the resistor and capacitor are connected to a virtual ground, the input current does not vary with capacitor charge and a linear integration of output is achieved**.**

The circuit can be analyzed by applying Kirchhoff's current law at the node v_2, keeping ideal op-amp behavior in mind

$$i1 = IB + iF$$

IB=U in an ideal op-amp, so:

$$i_1 = i_F$$

Furthermore, the capacitor has a current relationship governed by the equation:

$$Ic=C\bullet \frac{dVc}{dt}$$

Substituting the appropriate variables:

$$\frac{v_{in} - v_2}{R_1} = C_F \frac{d(v_2 - v_o)}{dt}$$

v2=v1=0 in an ideal op-amp, resulting in:

$$\frac{Vin}{R1} = -CF \frac{dv_0}{dt}$$

Integrating both sides with respect to time:

$$\int_0^t \frac{Vin}{R1}\, dt = -\int_0^t CF \frac{dv_0}{dt}\, dt$$

If the initial value of v_o is assumed to be 0 V, then integrating gives us:

$$Vo = -\frac{1}{R_1 C_F} \int_0^t Vin\, dt$$

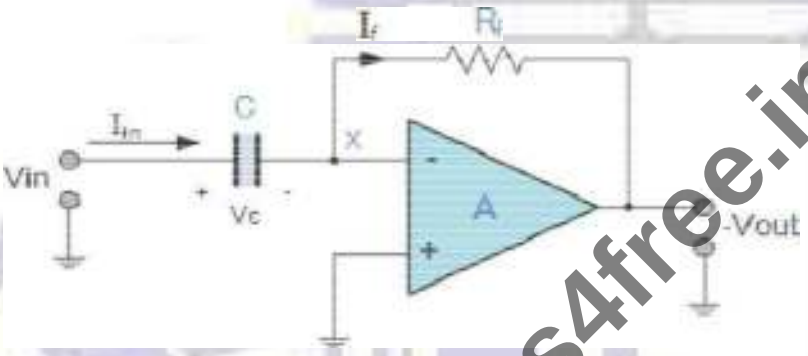
The Op-amp Differentiator Amplifier

The basic op-amp differentiator circuit is the opposite to that of the integrator amplifier circuit that we looked at in the previous tutorial. Here, the position of the capacitor and resistor have been reversed and now the reactance, Xc is connected to the input terminal of the inverting amplifier while the resistor, R*f* forms the negative feedback element across the operational amplifier as normal.

This Operational Amplifier circuit performs the mathematical operation of Differentiation that is it "produces a voltage output which is directly proportional to the input voltage's rate-of-change with respect to time ". In other words the faster or larger the change to the input voltage signal, the greater the input current, the greater will be the output voltage change in response, becoming more of a "spike" in shape.

As with the integrator circuit, we have a resistor and capacitor forming an RC Network across the operational amplifier and the reactance (Xc) of the capacitor plays a major role in the performance of a Op-amp Differentiator.

Op-amp Differentiator Circuit



The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependent on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is "High" resulting in a low gain (R*f*/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor R*f*.

$$I_{IN} = I_F \quad \textbf{and} \quad I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance x Voltage across the capacitor

$$Q = C \times V_{IN}$$

The rate of change of this charge is

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current i

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore \quad -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

from which we have an ideal voltage output for the op-amp differentiator is given as:

$$V_{OUT} = -R_F C\frac{dV_{IN}}{dt}$$

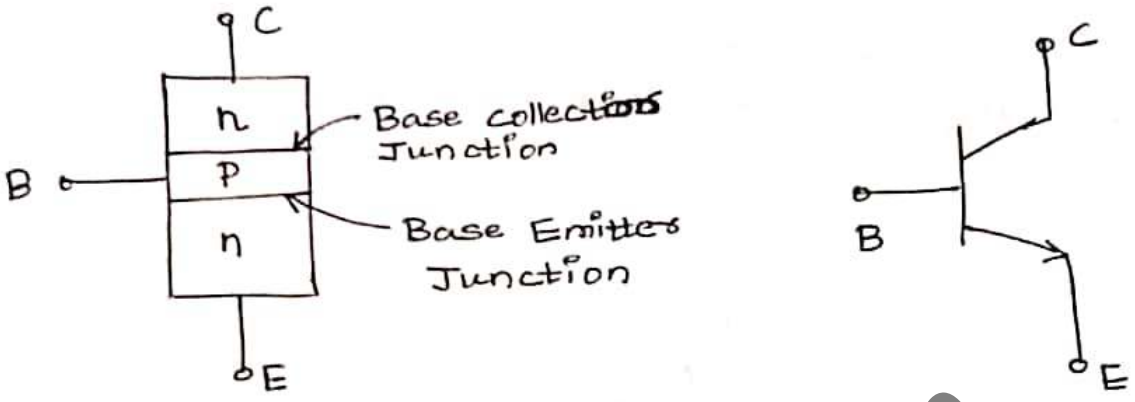
Therefore, the output voltage Vout is a constant -Rf .C times the derivative of the input voltage Vin with respect to time. The minus sign indicates a 180^o phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

MODULE - 4

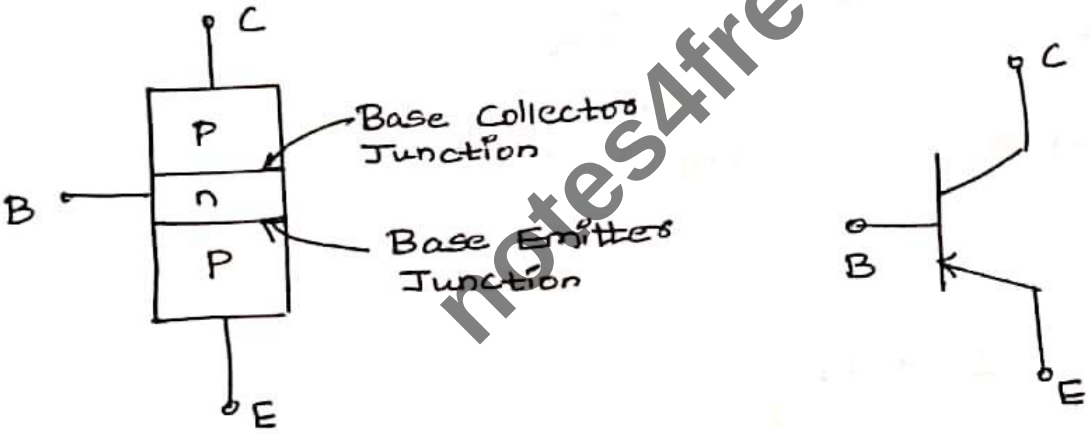
BJT Applications, Feedback amplifiers & Oscillators

Basic of Transistor

The BJT is constructed with three doped semiconductor regions separated by two pn junctions.



(a) npn transistor



(b) pnp transistor

The three terminals of BJT are : Base, Collector & Emitter.

Emitter is heavily doped
Collector is moderately doped
Base is lightly doped.

Biasing

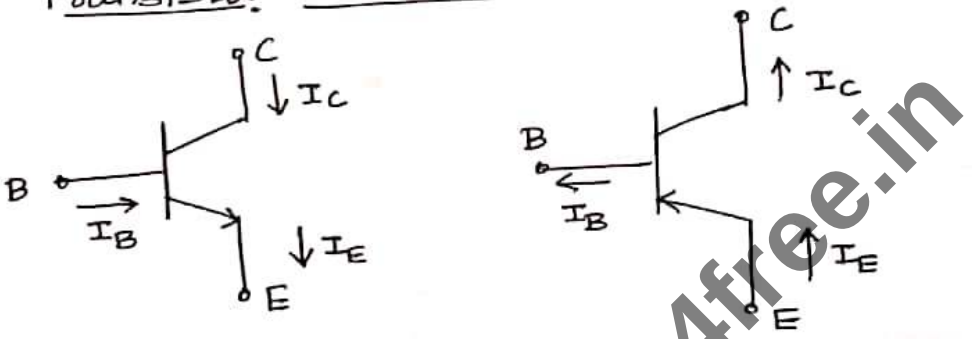
For transistor operation,

* Base - Emitter junction is forward biased.
* Base - Collector junction is reverse biased.

The transistor is operated in three regions:

- Cut-off region
- Saturation region } Transistor is used as switch
- Active region → Transistor is used as amplifier

Transistor Currents



npn transistor pnp transistor.

For transistor,

$$I_E = I_C + I_B$$

Transistor current gains:

→ common Emitter current gain (β_{dc})

→ common Base current gain (α_{dc})

The DC current gain β_{dc} is given by,

$$\beta_{dc} = \frac{I_C}{I_B}$$

β_{dc} range from 20 to 200 or more

The DC current gain α_{dc} is given by,

$$\alpha_{dc} = \frac{I_C}{I_E}$$

Always $\alpha_{dc} < 1$

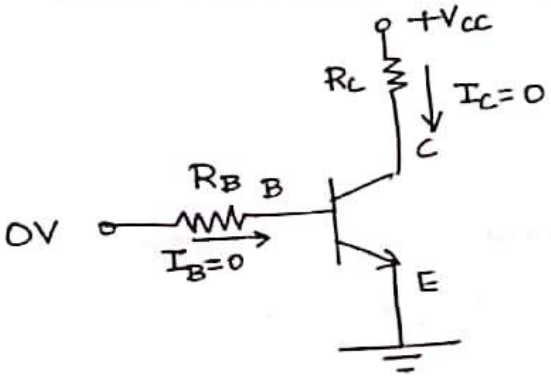
BJT as a Switch

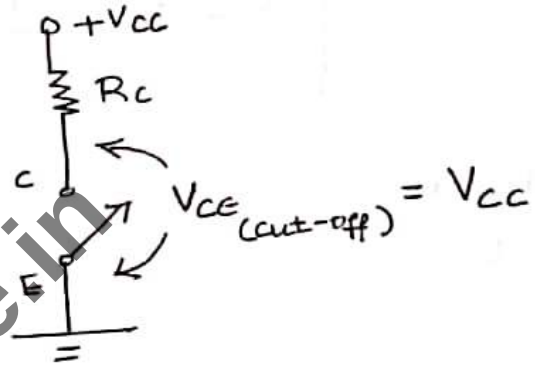
The major application of BJT is SWITCH. When BJT is used as a switch, it is operated alternately in cut-off and saturation regions.

In cut-off region, the transistor is OFF

In saturation region, the transistor is ON.

* Cut-off region : Switch Open (or) transistor OFF



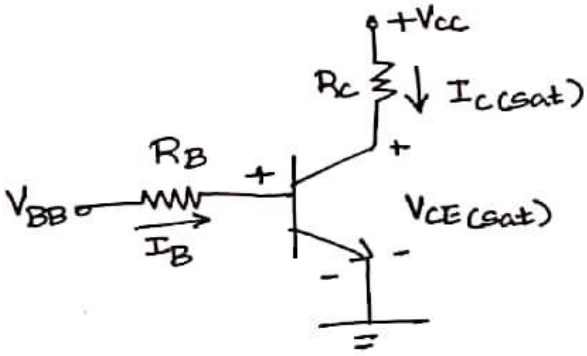


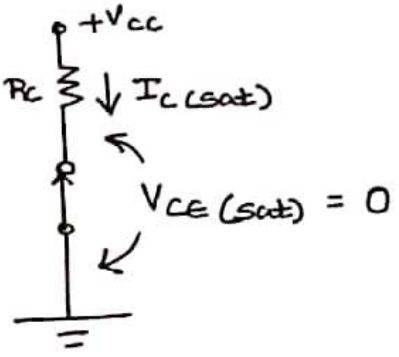
The base-emitter junction is not forward biased. Neglecting leakage current, all currents are zero.

i.e., $I_B = 0$, $I_C = 0$

$$V_{CE\,(cut-off)} = V_{cc}$$

* Saturation region : Switch close (or) transistor ON





The base-emitter junction is forward biased. Sufficient base current is applied to produce maximum collector current ($I_{C(sat)}$).

Applying KVL to the loop consisting of V_{cc}, V_{CE} & R_c,

$$V_{cc} = I_{C(sat)} R_c + V_{CE(sat)}$$

$$\boxed{I_{C(sat)} = \frac{V_{cc} - V_{CE(sat)}}{R_c}}$$

$V_{CE(sat)}$ is very small compared to V_{cc} & it can be neglected.

$$\therefore \boxed{I_{C(sat)} = \frac{V_{cc}}{R_c}}$$

The minimum value of base current I_B required to keep the transistor in saturation region is,

$$\boxed{I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}}}$$

Normally, I_B should be significantly greater than $I_{B(min)}$ to ensure that the transistor is in saturation.

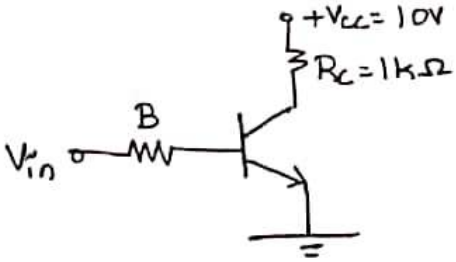
Problems

1) In the circuit shown below,

(a) What is V_{CE} when $V_{in}=0V$?

(b) What minimum value of I_B is required to keep the BJT in saturation ? Given $\beta_{dc}=200$

(c) Calculate the maximum value of R_B when $V_{in}=5V$.



a) When $V_{in}=0$, the transistor is in cut-off region.

$$\therefore \boxed{V_{CE} = V_{CE(cut-off)} = V_{CC} = 10V}$$

b) Neglecting $V_{CE(sat)}$,

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10}{1\times10^3}$$

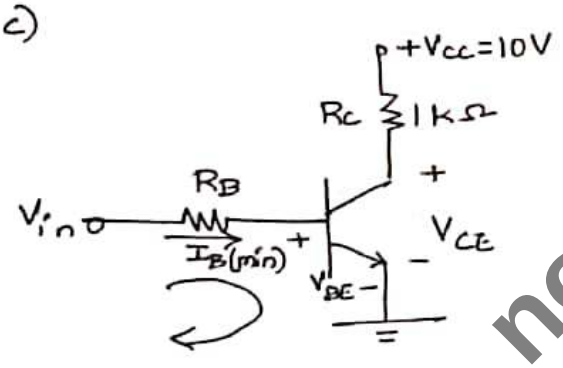
$$\boxed{I_{C(sat)} = 10mA}$$

c)

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{10\times10^{-3}}{200}$$

$$\boxed{I_{B(min)} = 50\mu A}$$

c)



Applying KVL,

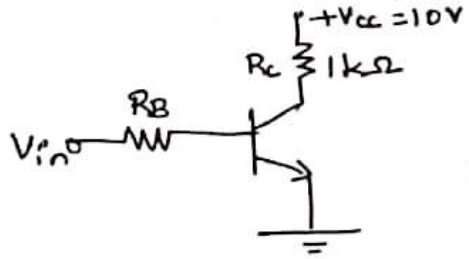
$$V_{in} = I_{B(min)} R_B + V_{BE}$$

$$R_{B(max)} = \frac{V_{in} - V_{BE}}{I_{B(min)}}$$

$$R_{B(max)} = \frac{5 - 0.7}{50\mu A} = \frac{4.3}{50\mu A}$$

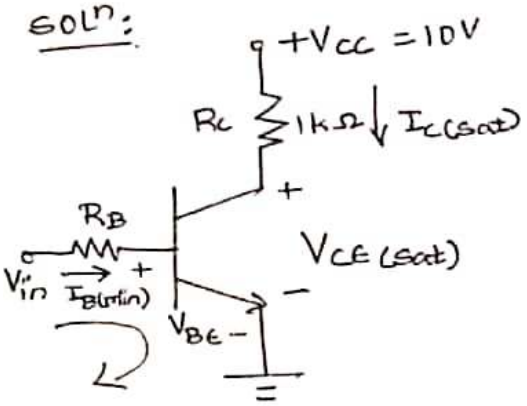
$$\boxed{R_{B(max)} = 86k\Omega}$$

2) What is the minimum value of I_B required to saturate the transistor shown in fig. if $\beta_{dc}=125$ & $V_{CE(sat)}=0.2V$



Also find the maximum value of R_B required when $V_{in} = 8V$.

Soln:



Applying KVL to the loop consisting of V_{CC}, R_C & V_{CE},

$$V_{CC} = I_{C(sat)} R_C + V_{CE(sat)}$$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

$$= \frac{10 - 0.2}{1k\Omega}$$

$$\boxed{I_{C(sat)} = 9.8\,mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{9.8 \times 10^{-3}}{125}$$

$$\boxed{I_{B(min)} = 78.4\,\mu A}$$

Applying KVL to the loop consisting of V_{in}, R_B, V_{BE}

$$V_{in} = I_{B(min)} R_B + V_{BE}$$

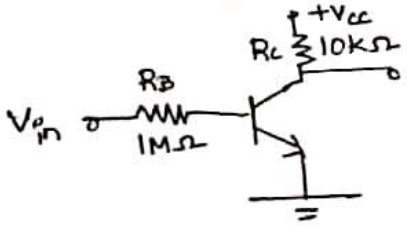
$$R_B = \frac{V_{in} - V_{BE}}{I_{B(min)}} = \frac{8 - 0.7}{78.4\mu A}$$

$$\boxed{R_B = 93.11k\Omega}$$

3) In the circuit shown,

(a) What is the value of I_B necessary to produce saturation?

(b) What is the minimum value of V_{in} necessary for saturation? Assume $V_{CE(sat)} = 0V$



$\beta_{dc} = 150$

Sol":

(i) Assuming $V_{CE(sat)} = 0V$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{V_{CC}}{R_C}$$

$$I_{C(sat)} = \frac{5}{10K}$$

$$\boxed{I_{C(sat)} = 500\mu A}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}}$$

$$= \frac{500\mu A}{150}$$

$$\boxed{I_{B(min)} = 3.33\mu A}$$

(ii) $V_{in} = I_B R_B + V_{BE}$

We get $I_{B(min)}$ when V_{in} is minimum

$$V_{in(min)} = I_{B(min)} R_B + V_{BE}$$

$$V_{in(min)} = (3.33\mu A) \times 1M\Omega + 0.7$$

$$\boxed{V_{in(min)} = 4.03V}$$

Transistor switch circuit to switch ON/OFF an LED/Lamp

A simple application of transistor switch circuit is to switch ON/OFF an LED.

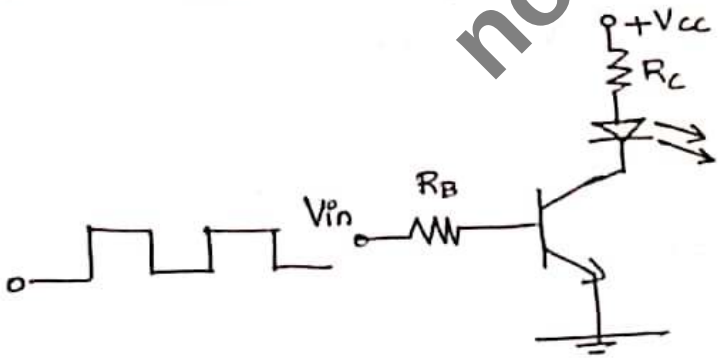


Fig: Transistor circuit to switch ON/OFF LED

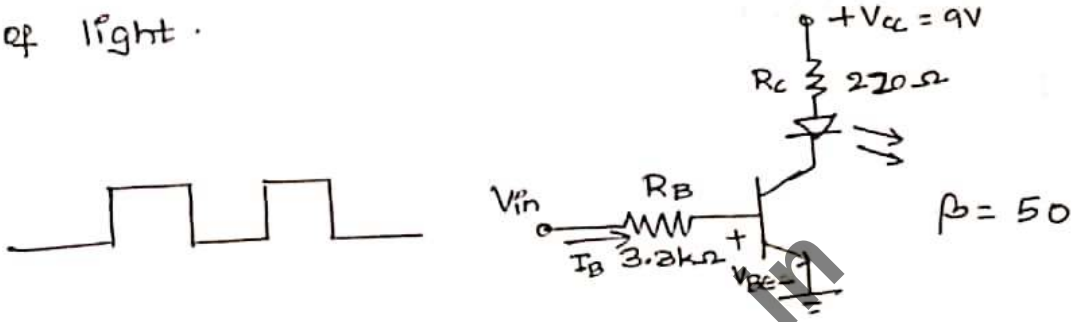
The input to the circuit is a square wave. When the square wave is at 0V, the transistor is in cut-off & $I_B = 0$ and $I_C = 0$, therefore LED is OFF and does not emit light.

When the square wave goes to its high level, the transistor saturates and this forward biases the LED. The resulting collector current through the LED causes it to emit light.

Thus the LED turns ON when V_{in} is high and OFF when $V_{in}=0$, resulting in blinking of LED.

Problem

1) The LED shown in fig requires 30mA to emit a sufficient level of light.



Determine the amplitude of the square wave input voltage necessary to make sure that the transistor saturates. Use double the minimum value of I_B to ensure saturation. Assume $V_{CE(sat)} = 0.3V$ & $V_{LED} = 1.6V$.

soln:

Applying KVL to the loop consisting of V_{CC}, R_C, LED, V_{CE},

$$V_{CC} = I_{C(sat)} \cdot R_C + V_{LED} + V_{CE(sat)}$$

$$I_{C(sat)} = \frac{V_{CC} - V_{LED} - V_{CE(sat)}}{R_C} = \frac{9 - 1.6 - 0.3V}{220\Omega}$$

$$\boxed{I_{C(sat)} = 32.3mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{(min)}} = \frac{32.3mA}{50} \Rightarrow \boxed{I_{B(min)} = 646\mu A}$$

To ensure saturation, double $I_{B(min)}$ $\longrightarrow$ $\boxed{2I_{B(min)} = 1.29mA}$

Applying KVL to loop consisting of V_{in}, R_B, V_{BE}

$$V_{in} = 2I_{B(min)} R_B + V_{BE} = (1.29mA \times 3.3k\Omega) + 0.7$$

$$\boxed{V_{in} = 4.96\,V}$$

BJT as amplifier

* Current amplification

A transistor amplifies current and the collector current is given by,

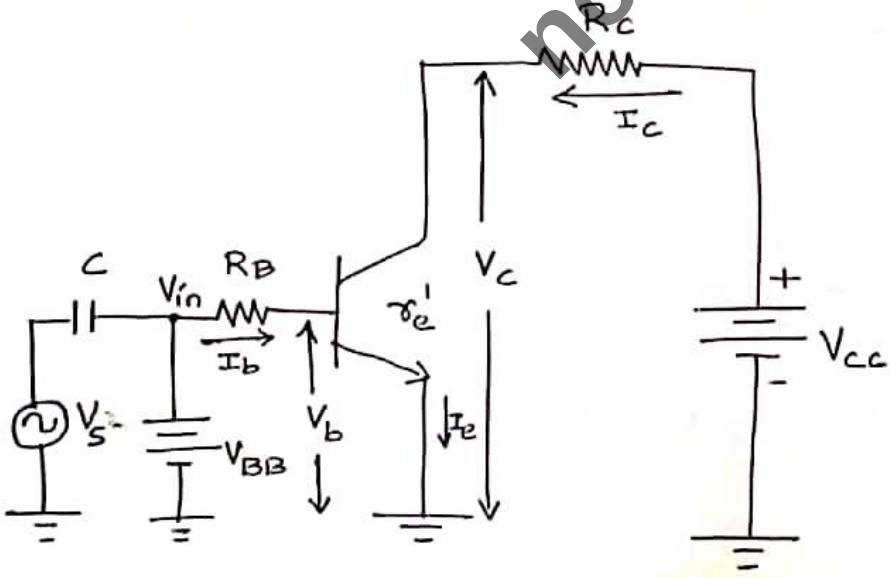
$$I_C = \beta I_B$$

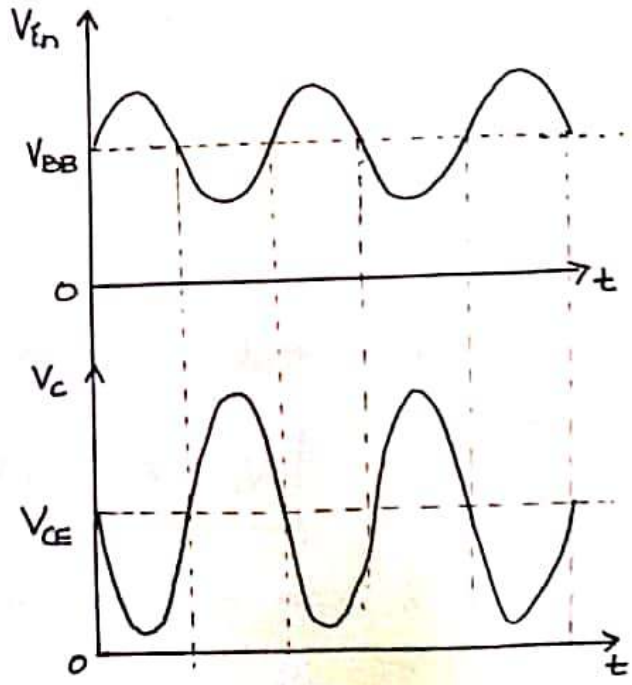
i.e., base current I_B is amplified by a factor called current gain 'β'.

* Voltage amplification

The transistor amplifier circuit is as shown in the figure.

An ac voltage V_s is superimposed on the dc bias voltage V_{BB} by capacitive coupling. The dc bias voltage V_{cc} is connected to the collector through the collector resistance R_C.





The ac input voltage produces an ac base current which results in a much larger ac collector current. The ac collector current produces an ac voltage across R_C which is amplified and inverted version of ac input voltage.

The forward biased base-emitter junction offers a low resistance to the ac signal. This internal resistance is ac emitter resistance 'r_e'' and it appears in series with R_B.

The ac base voltage is,

$$V_b = I_e r_e'$$

The ac collector voltage V_c is the ac voltage drop across R_C,

$$V_C = I_c R_C$$

WKT, $I_E = I_c + I_b$

$\because I_c >> I_b$

$I_e \simeq I_c$

$\therefore$ $$V_C \simeq I_e R_C$$

V_b can be considered as the transistor ac input voltage,

$$V_b = V_s - I_b R_B$$

V_c can be considered as the transistor ac output voltage.

Voltage gain is defined as the ratio of the output voltage to the input voltage.

$\therefore$ $$A_V = \frac{V_c}{V_b}$$

Substituting the values for V_c & V_b,

$$A_V = \frac{V_c}{V_b} = \frac{I_e R_c}{I_e r_e'}$$

$$A_V = \frac{V_c}{V_b} = \frac{R_c}{r_e'}$$

This equation shows that the transistor provides amplification in the form of voltage gain, which is dependent on the values of R_c and r_e'.

Since R_c is looger than r_e', the output voltage is greater than the input voltage.

$$V_c = A_V V_b$$

$$V_c = \frac{R_c}{r_e'} V_b$$

Problems

▷ A transistor amplifier has a voltage gain is 50. What is the output voltage when the input voltage is 100mV?

Soln:

Given,

$A_V = 50$

$V_b = 100mV$

Voltage gain, $A_V = \frac{V_c}{V_b}$

$V_c = A_V V_b$

$= 50 \times 100mV$

$V_c = 5V$

2) To achieve an output of 10V with an input of 300mV, what is the required voltage gain?

Soln:

$V_{out} = V_c = 10V$

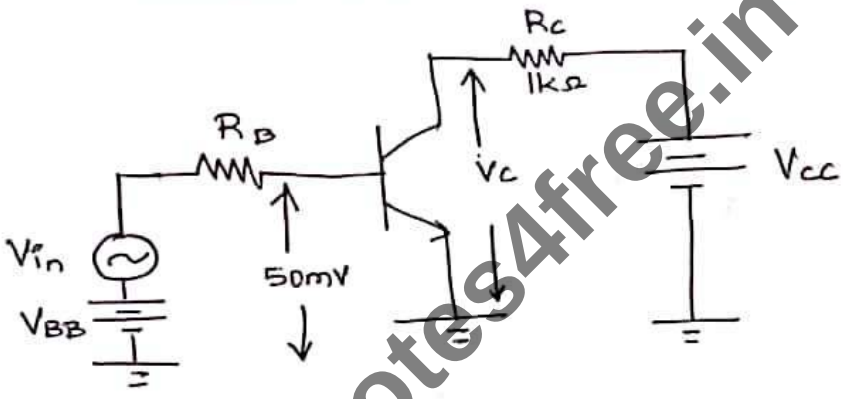
$V_{in} = V_b = 300mV$

Voltage Gain,

$$A_V = \frac{V_c}{V_b} = \frac{10}{300mV}$$

$$\boxed{A_V = 33.33}$$

3) Determine the voltage gain and the ac output voltage for the circuit shown. Assume $r_e' = 50\Omega$



Soln: Given,

$V_b = 50mV$

$r_e' = 50\Omega$

Voltage gain, $A_V = \frac{R_c}{r_e'} = \frac{1 \times 10^3}{50}$

$$\boxed{A_V = 20}$$

$$A_V = \frac{V_c}{V_b}$$

$V_c = A_V V_b = 20 \times 50mV$

$$\boxed{V_c = 1V}$$

4) A 50mV signal is applied to the base of a transistor with $r_e' = 20\Omega$ and $R_c = 620\Omega$. Determine the output voltage.

Soln:

Given,

$V_b = 50mV$

$r_e' = 20\Omega$

$R_c = 620\Omega$

Voltage gain,

$$A_V = \frac{R_c}{r_e'} = \frac{620}{20}$$

$$\boxed{A_V = 31}$$

Output voltage,

$$V_c = A_V V_b$$

$$= 31 \times 50mV$$

$$\boxed{V_c = 1.55V}$$

5) A change of 20μA in base current results in a change of 2.5mA in collector current. Calculate the current gain.

Soln:

Given,

$I_b = 20\mu A$

$I_c = 2.5mA$

Current gain, $A_i = \frac{I_c}{I_b} = \frac{2.5 \times 10^{-3}}{20 \times 10^{-6}}$

$$\boxed{A_i = 125}$$

6) If the voltage gain of a amplifier is 110 and the current gain is 12.5 . Calculate the power gain.

Soln:

$A_V = 110$

$A_i = 12.5$

Power gain,

$A_p = A_V A_i$

$= 110 \times 12.5$

$\boxed{A_p = 1375}$

7) An amplifier has an input signal of 0.25V and draws 1mA from the source. It delivers 8V to a load at 10mA. Determine the voltage, current and power gains.

Soln:

Given,

$V_b = 0.25V$ $\quad I_b = 1mA$

$V_c = 8V$ $\quad I_c = 10mA$

Voltage gain, $A_V = \frac{V_c}{V_b} = \frac{8}{0.25}$ $\quad \boxed{A_V = 32}$

Current gain, $A_i = \frac{I_c}{I_b} = \frac{10 \times 10^{-3}}{1 \times 10^{-3}}$ $\quad \boxed{A_i = 10}$

Power gain, $A_p = A_V A_i$

$= 32 \times 10$

$\boxed{A_p = 320}$

MODULE-5

Digital Electronics Fundamentals:

Number System

The decimal number system (Base 10) is a familiar number system. Some other number systems that are having equal importance are: Binary (Base 2),octal(Base 8), Hexadecimal(Base 16)

All number systems have some common characteristics:

- The digits are consecutive.
- The number of digits is equal to the size of the base.
- Zero is always the first digit.
- The base number is never a digit.
- When 1 is added to the largest digit, a sum of zero and a carry of one results.
- Numeric values determined by the have implicit positional values of the digits.

Binary Numbers

The binary number system is used to model the series of electrical signals computers use to represent information. It is also called the **"**Base 2 system**"**.

Each digit in binary is a 0 or a 1 and is called a **bit**, which is an abbreviation of **binary digit**. 0 represents the no voltage or an off state and 1 represents the presence of voltage or an on state

There are several common conventions for representation of numbers in binary. The most familiar is **unsigned binary**. An example of a 8-bit number in this case

is $010011112 = 0*2^7 + 1*2^6 + \_\ \_\ \_ + 1*2^0 = 64 + 8 + 4 + 2 + 1 = 7910$

The largest number which can be represented by **n** bits is $2^n - 1$. For example, with 4 bits the largest number is $1111_2 = 15$.

The most significant bit (MSB) is the bit representing the highest power of 2, and the Least significant bit (LSB) represents the lowest power of 2.

Example : Binary: 1110110111

MSB **LSB**

Deciml	Binary No
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Decimal to Binary Conversion

The easiest way to convert a decimal number to its binary equivalent is to use the repeated division of a decimal number by 2 and records the quotient and remainder.

The remainder digits (a sequence of zeros and ones) form the binary equivalent in least significant to most significant digit sequence

Example: Convert 67 to its binary equivalent:

$67_{10} = x_2$

Step 1: 67 / 2 = 33 R 1 **Divide 67 by 2. Record quotient in next row**

Step 2: 33 / 2 = 16 R 1 **Again divide by 2; record quotient in next row**

Step 3: 16 / 2 = 8 R 0 **Repeat again**

Step 4: 8 / 2 = 4 R 0 **Repeat again**

Step 5: 4 / 2 = 2 R 0 **Repeat again**

Step 6: 2 / 2 = 1 R 0 **Repeat again**

Step 7: 1 / 2 = 0 R 1 STOP **when quotient equals 0**

Thus $(67)_{10}= (1\ 0\ 0\ 0\ 0\ 1\ 1)_2$

Similarly we can convert 57 and 211 as given below

- 53 = 32 + 16 + 4 + 1
  = 25 + 24 + 22 + 20
  = 1*25 + 1*24 + 0*23 + 1*22 + 0*21 + 1*20
  = 110101 in binary
  = 00110101 as a full byte in binary

- 211= 128 + 64 + 16 + 2 + 1
  = 27 + 26 + 24 + 21 + 20
  = 1*27 + 1*26 + 0*25 + 1*24 + 0*23 + 0*22
  + 1*21 + 1*20
  = 11010011 in binary

Binary to Decimal Conversion

Multiply the binary digits by increasing powers of two, starting from the right and then find the decimal number equivalent by summing those products.

Example:

- What is 10011010 in decimal?

$10011010 = 1*2^7 + 0*2^6 + 0*2^5 + 1*2^4 + 1*2^3 + 0*2^2 + 1*2^1 + 0*2^0$
$= 2^7 + 2^4 + 2^3 + 2^1$
$= 128 + 16 + 8 + 2$
$= 154$

- What is 00101001 in decimal?

$00101001 = 0*2^7 + 0*2^6 + 1*2^5 + 0*2^4 + 1*2^3 + 0*2^2 + 0*2^1 + 1*2^0$
$= 2^5 + 2^3 + 2^0$
$= 32 + 8 + 1$
$= 41$

Representation of Negative Numbers

There are two commonly used conventions for representing negative numbers. With **sign magnitude**, the MSB is used to flag a negative number. So for example with 4-bit numbers we would have 0011 = 3 and 1011 = −3. This is simple to see, but is not good for doing arithmetic.

With **2's complement**, negative numbers are designed so that the sum of a number and its 2's complement is zero.

Using the 4-bit example , we have 0101 = 5 and its 2's complement −5 = 1011. Adding (remember to carry) gives 10000 = 0. (The 5th bit doesn't count!)

Both addition and multiplication work as you would expect using 2's complement.

There are two methods for forming the 2's complement:

1. Make the transformation 0 ! 1 and 1!0, then add 1.

2. Add some number to −2MSB to get the number you want. For 4-bit numbers an example of finding the 2's complement of 5 is −5 = −8 + 3 = 1000 + 0011 = 1011.

- 2's complement
  - Step 1: Find 1's complement of the number

    Binary # 11000110

    1's complement 00111001
  - Step 2: Add 1 to the 1's complement

```
  00111001
+ 00000001
----------
  00111010
```

Octal Number System

Also known as the Base 8 System. Uses digits 0 – 7.It can be readily converts to binary by grouping three (binary) digits starting from the radix point. Each octal number converts to 3 binary digits

Example:

1) Convert 427_{10} to its octal equivalent:

427 / 8 = 53 R3 — Divide by 8; R is LSD

53 / 8 = 6 R5 — Divide Q by 8; R is next digit

6 / 8 = 0 R6 — Repeat until Q = 0

Thus $427_{10} = 653_8$

2) Convert 653_8 to binary

```
6   5   3
↓   ↓   ↓
110 101 011
```

Thus $653_8 = 110101011_2$

Hexadecimal Representation

It is very often quite useful to represent blocks of 4 bits by a single digit. Thus in base 16 there is a convention for using one digit for the numbers 0,1,2,**: : :**,15 which is called **hexadecimal**. It follows decimal for 0 to 9, then uses letters A to F for representing 10 to 15 respectively.

Decimal	Hexadecimal
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	A
11	B
12	C
13	D
14	E
15	F

CONVERSIONS

- Convert 830_{10} to its hexadecimal equivalent:

  830 / 16 = 51 R14

  51 / 16 = 3 R3

  3 / 16 = 0 R3

  Thus 830_{10} = 33E(As 14 is represented as E)

Binary to Hexadecimal Conversion

The easiest method for converting binary to hexadecimal is to use a substitution code.Each hex number converts to 4 binary digits as shown in the table.

Substitution Code

0000 = 0	0100 = 4	1000 = 8	1100 = C
0001 = 1	0101 = 5	1001 = 9	1101 = D
0010 = 2	0110 = 6	1010 = A	1110 = E
0011 = 3	0111 = 7	1011 = B	1111 = F

Floating Point Numbers

Real numbers must be normalized using scientific notation:

$0.1\ldots \times 2^{\mathbf{n}}$ where **n** is an integer

Note that the whole number part is always 0 and the most significant digit of the fraction is a 1 – ALWAYS!

Standard Format single precision representation uses 32-bit word
The exponent field (8 bits) can be used to represent integers from 0-255
Because of the need for negative exponents to be represented as well, the range is offset or biased from – 128 to + 127
In this way, both very large and very small numbers can be represented

Logic Gate

A logic gate is a hardware implementing a Boolean function; that is, it performs a logical operation on one or more logical inputs, and produces a single logical output. Depending on the context, the term may refer to an ideal logic gate, one that has for instance zero rise time and unlimited fan-out(the number of gate inputs it can feed or connect to), or it may refer to a non-ideal physical device

Logic gates are primarily implemented using diodes or transistors acting as electronic witches, but can also be constructed using vacuum tubes, electromagnetic relays , fluidic ogic, pneumatic logic, optics, molecules, or even mechanical elements. With amplification, logic gates can be cascaded in the same way that Boolean functions can be composed, allowing the construction of a physical model of all of Boolean logic, and therefore, all of the algorithms and mathematics that can be described with Boolean logic.

The three basic logical operations are:

- AND
- OR
- NOT

AND gate

The AND gate is an electronic circuit that gives true output i.e output (1) only if all its inputs are true. A dot (·) is used to show the AND operation i.e. A·B.

OR gate

The OR gate is an electronic circuit that gives a gives a true output true output (1) if one or more one or more of its inputs are true. A plus (+) is used to show the OR operation.

NOT gate

The NOT gate is an electronic circuit that produces an inverted version of the input at its output.

- It is also known as an inverter.
- If the input variable is A, the inverted output is known as NOT A

This is also shown as A', or Ā with a bar over the top.

NAND gate

- This is a NOT-AND gate which is equal to an AND followed by a NOT gate.
- The outputs of all NAND gates are true if any of the inputs are false.
- The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

NOR gate

- This is a NOT-OR gate which is equal to an OR gate followed by a gate followed by a NOT gate .
- The outputs of all NOR gates are false if any of the inputs are true.
- The symbol is an OR gate with a small circle on the output. The small circle represents inversion represents inversion.

EXOR gate

- The 'Exclusive-OR' gate is a circuit which will give a true output if either, but not both, of its two inputs are true.
- An encircled plus sign (⊕) is used to show the EXOR operation.

EXNOR gate

- The 'Exclusive-NOR' gate circuit does the opposite to the EXNOR gate.
- It will give a false output if either, but not both, of its two inputs are true.
- The symbol is an EXOR gate with a small circle on the output small circle on the output .
- The small circle represents inversion.

T)p▷	Oi.lfnClht vhupe	Rt!climAular ,11upc	Oook..1ll UIJ.!,tl,ra between &. U	Trulli U.tble
\ 11)	=D-	~	A:.B	I 'PLT OuTPL"T A B AANDB 0 0 0 0 I 0 I 0 0 I I I
OR	~	~	A+ B	A B AORB 0 0 0 0 I I I 0 I I I I
-OT 'I \1'D	~	-{2)-	A	11'P I OIJTPTT 0 I I 0
	~	—	A·B	I 'PI-I' OI"TI'I'T A B A ANDB 0 0 I 0 I I I 0 I I I 0
'OI<	=D-	~	A+ B	11'PLT OuTPL'T A B ANORB 0 0 I 0 I 0 I 0 0 I I 0
XOM.	~	~	,1 'O LJ	L..P.rr O<rn>U ' A B A..XOR B 0 0 0 0 I I I 0 I I I 0
x.NO.R.	~	~	Acrf"'ZJ-.10 /3	L A a A XNORO 0 I I 0 0 0 I I

Boolean Algebra

Invented by George Boole in 1854. It's a convenient way and systematic way of expressing and analyzing the operation of logic circuits.

An algebraic structure defined by a set **B** = {0, 1}, together with two binary operators (+ and ·) and a unary operator.

Terms going to be used-

- **Variable** – a symbol used to represent a logical quantity.
- **Complement** – the inverse of a variable and is indicated by a bar over the variable.
- **Literal** – a variable or the complement of a variable.

Boolean Addition

- Boolean addition is equivalent to the OR operation
- A **sum term** is produced by an OR operation with no AND ops involved.
  - i.e. **A + B, A + B, A + B + C , A + B + C + D**
  - A **sum term** is equal to 1 when one or more of the literals in the term are 1.
  - A **sum term** is equal to 0 only if each of the literals is 0.

Boolean Multiplication

- Boolean multiplication is equivalent to the AND operation
- A **product term** is produced by an AND operation with no OR ops involved. i.e. **AB, AB, ABC , ABCD**

A **product term** is equal to 1 only if each of the literals in the term is 1.

A **product term** is equal to 0 when one or more of the literals are 0.

Laws of Boolean Algebra

The basic laws of Boolean algebra:
The **commutative** laws
The **commutative law of addition** for two variables is written as: **A+B = B+A**
The **commutative law of multiplication** for two variables is written as: **AB = BA**

The **associative** laws
The **associative law of addition** for 3 variables is written as:**A+(B+C) = (A+B)+C**
The **associative law of multiplication** for 3 variables is written as: **A(BC) = (AB)C**
The **distributive** laws
The **distributive law** is written for 3 variables as follows: **A(B+C) = AB**

DeMorgan's Theorems

The complement of two or more ANDed variables is equivalent to the OR of the complements of the individual variables.

$$\overline{X \cdot Y} = \overline{X} + \overline{Y}$$

The complement of two or more ORed variables is equivalent to the AND of the complements of the individual variables.

$$\overline{X + Y} = \overline{X} \cdot \overline{Y}$$

Latches & Flip-flops

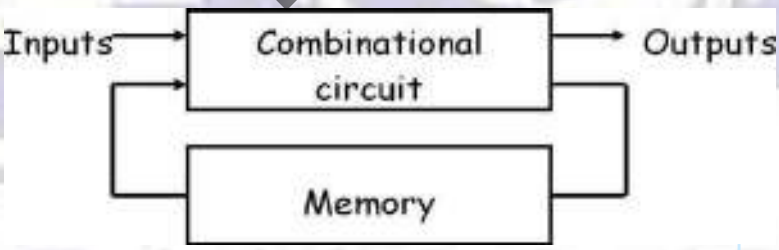
Digital circuits can be classified as

1. **Combinational circuits:**

In this case present output of the circuit depends on present inputs only.

2.. **Sequential circuits:**

- Present output not only depends on present inputs but also on the previous state of output.
- It can be realized as combinational circuit with a feedback path along with a memory element.



The most basic memory element can be realized by two inverters forming a static memory cell. Assume A=0 and B=1, then the below circuit will maintain these values indefinitely (as long as it has power applied) . The state is defined by the value of the memory cell

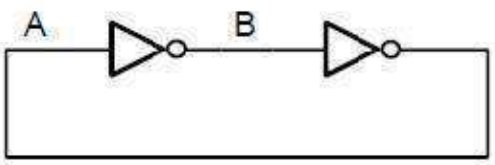


Fig: Static memory cell

S-R Latches :

Most basic type of latch.

It is known as set-reset latch as it has two stable output state.

- NOR gates can be used instead of inverters. The SR latch below has two inputs S and R, which will control the outputs Q and Q'.
- Here Q and Q' feed back into the circuit. They're not only outputs, they're also inputs!
- To figure out how Q and Q' change, we have to look at not only the inputs S and R, but also the **current** values of Q and Q':

Qnext = (R + Q'current)'

Q'next = (S + urrent)'

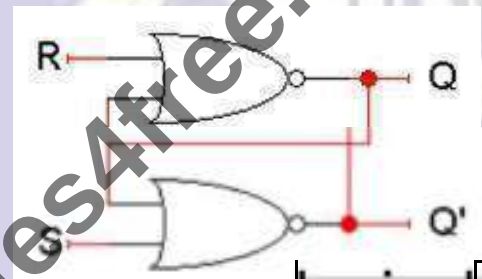
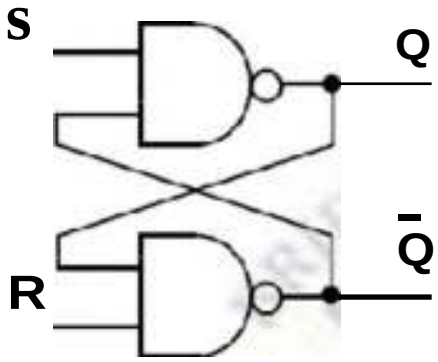


Fig : S-R latch using NOR gate

The state S=R=1 is invalid and not allowed

Fig : Truth table S-R latch using NOR gate

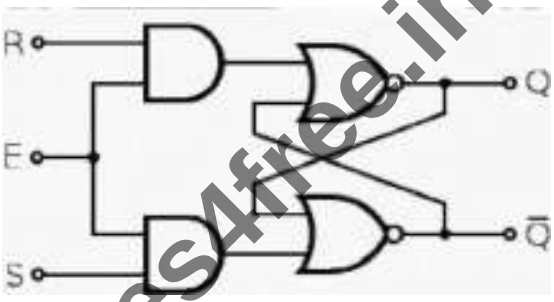
S	R	Q
0	0	No change
0	1	0 (reset)
1	0	1 (set)



S	R	a+	ā+	Function
0	0	1-?	1-?	Indeterminate State
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	Q	Storage State

Fig: S'-R' Latch using cross coupled NAND gate

Gated SR latch



A gated SR latch circuit diagram constructed from NOR gates.

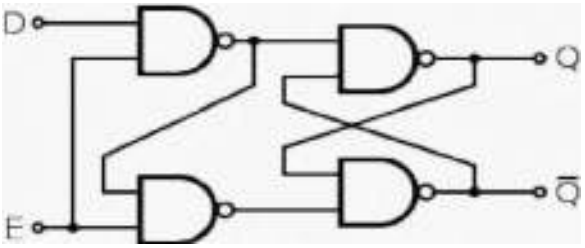
A **synchronous SR latch** (sometimes **clocked SR flip-flop**) can be made by adding a second level of NAND gates to the inverted SR latch (or a second level of AND gates to the direct SR latch). The extra NAND gates further invert the inputs so the simple SR latch becomes a gated SR latch (and a simple SR latch would transform into a gated SR latch with inverted enable).

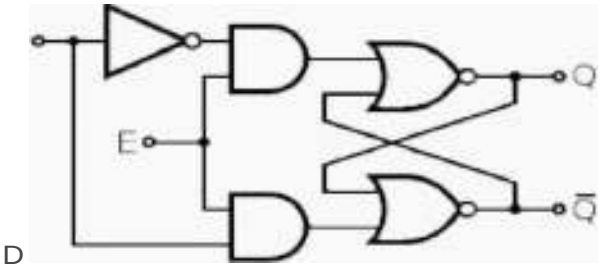
With E high (**enable** true), the signals can pass through the input gates to the encapsulated latch; all signal combinations except for (0,0) = **hold** then immediately reproduce on the (Q,Q) output, i.e. the latch is**transparent**.

With E low (**enable** false) the latch is **closed (opaque)** and remains in the state it was left the last time E was high.

The **enable** input is sometimes a clock signal, but more often a read or write strobe.

Gated D latch





A D-type transparent latch based on an SR NAND latch

A gated D latch based on an SR NOR latch

This latch exploits the fact that, in the two active input combinations (01 and 10) of a gated SR latch, R is the complement of S. The input NAND stage converts the two D input states (0 and 1) to these two input combinations for the next SR latch by inverting the data input signal. The low state of the **enable** signal produces the inactive "11" combination. Thus a gated D-latch may be considered as a **one-input synchronous SR latch**. This configuration prevents application of the restricted input combination. It is also known as **transparent latch**,**data latch**, or simply **gated latch**. It has a **data** input and an **enable** signal (sometimes named **clock**, or **control**). The word ~~**transparent** comes from the fact~~ that~~, when the~~ enable input ~~is on, the signal propagates directly~~ through the circuit, from the input D to the output Q.

Transparent latches are typically used as I/O ports or in asynchronous systems, or in synchronous two-phase systems (synchronous systems that use a two-phase clock), where two latches operating on different clock phases prevent data transparency as in a master–slave flip-flop.

Latches are available as integrated circuits, usually with multiple latches per chip. For example, 74HC75 is a quadruple transparent latch in the 7400 series.

Gated D latch truth table

E/C	D	Q	Q	Comment
0	X	Qprev	pre v	No change
1	0	0	1	Reset latch
1	1	1	0	Set

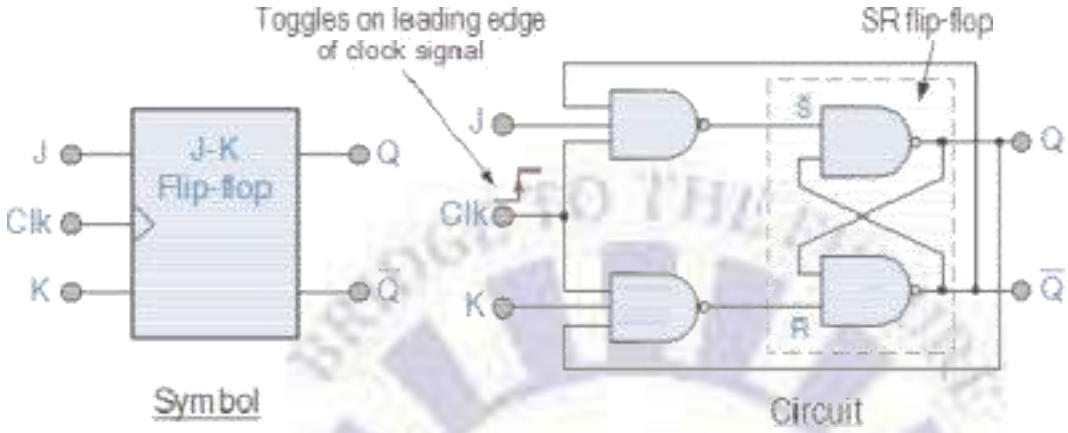
Symbol for a gated D

The truth table shows that when the **e**nable/**c**lock input is 0, the D input has no effect on the output. When E/C is high, the output equals D.

J-K Flip-flop

This simple **JK flip Flop** is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit. The sequential operation of the JK flip flop is exactly the same as for the previous SR flip-flop with the same "Set" and "Reset" inputs. The difference this time is that the "JK flip flop" has no invalid or forbidden input states of the SR Latch even when S and R are both at logic "1".

The **JK flip flop** is basically a gated SR Flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations, "logic 1", "logic 0", "no change" and "toggle". The symbol for a JK flip flop is similar to that of an SR Bistable Latch as seen in the previous tutorial except for the addition of a clockinput



Both the S and the R inputs of the previous SR bistable have now been replaced by two inputs called the J and K inputs, respectively after its inventor Jack Kilby. Then this equates to: J = S and K = R.

The two 2-input AND gates of the gated SR bistable have now been replaced by two 3-input NANDgates with the third input of each gate connected to the outputs at Q and Q. This cross coupling of the SR flip-flop allows the previously invalid condition of S = "1" and R = "1" state to be used to produce a "toggle action" as the two inputs are now interlocked.

If the circuit is now "SET" the J input is inhibited by the "0" status of Q through the lower NAND gate. If the circuit is "RESET" the K input is inhibited by the "0" status of Q through the upper NAND gate. As Qand Q are always different we can use them to control the input. When both inputs J and K are equal to logic "1", the JK flip flop toggles as shown in the following truth table.

Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
⊠	x	x	-		-		Latched
⊓	0	0	0	1	0	1	No Change
⊓			1	0	1	0	
⊓	0	1	0	1	0	1	Reset
⊓			1	0	0	1	
⊓	1	0	0	1	1	0	Set
⊓			1	0	1	0	
⊓	1	1	0	1	1	0	Toggles
⊓			1	0	0	1	

shift registers

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flop is driven by a common clock, and all are set or reset simultaneously.

Register:

- n A set of n flip-flops
- n Each flip-flop stores one bit
- n Two basic functions: data storage (Fig 1.2) and data movement (Fig 1.1).

Shift Register:

A register that allows each of the flip-flops to pass the stored information to its adjacent neighbour. Fig 1.1 shows the basic data movement in shift registers.

Counter:

A register that goes through a predetermined sequence of states

Figure 1.1: Basic data movement in shift registers

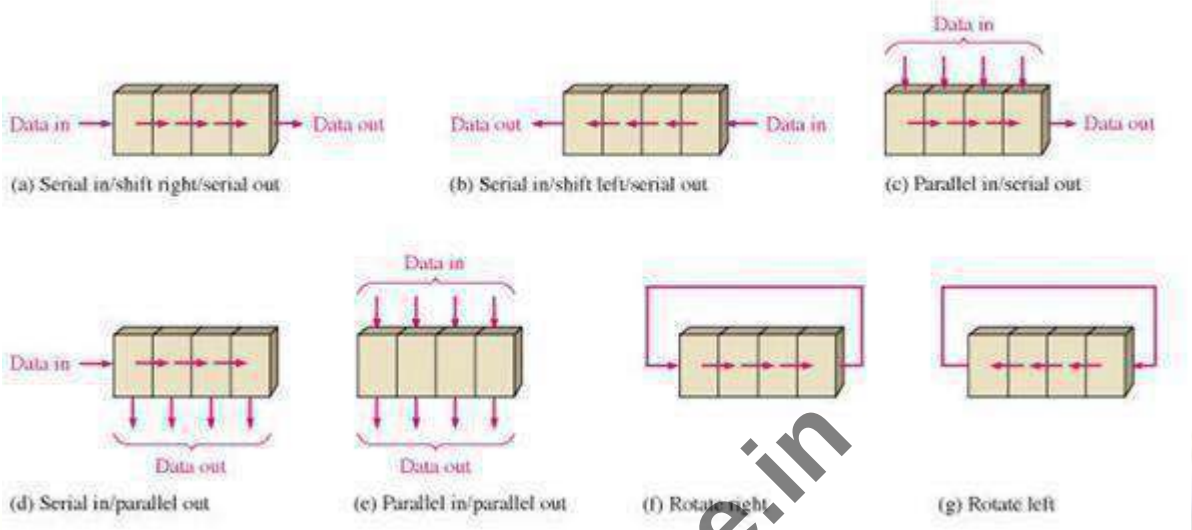


Fig 1.2: The flip-flop as a storage element

Storage Capacity:

The storage capacity of a register is the total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity.

Classification

The shift registers can be classified as

- Serial In - Serial Out(SISO) Shift Registers
- Serial In - Parallel Out (SIPO)Shift Registers
- Parallel In - Serial Out (PISO)Shift Registers
- Parallel In - Parallel Out (PIPO)Shift Registers

Serial In - Serial Out Shift Registers

The serial in/serial out shift register accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.

Basic four-bit shift register

A basic four-bit shift register can be constructed using four D flip-flops, as shown in Fig 2.1. The operation of the circuit is as follows.

- The register is first cleared, forcing all four outputs to zero.
- The input data is then applied sequentially to the D input of the first flip-flop on the left (FF0).
- During each clock pulse, one bit is transmitted from left to right.
- Assume a data word to be 1001.
- The least significant bit of the data has to be shifted through the register from FF0 to FF3.

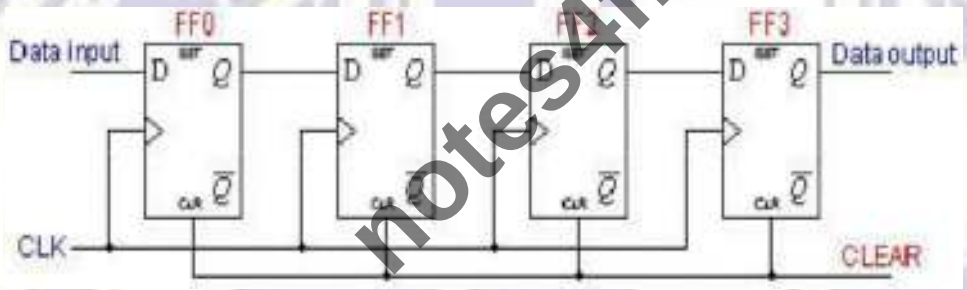


Fig 2.1: Basic four-bit shift register

In order to get the data out of the register, they must be shifted out serially. The data is loaded to the register when the control line is HIGH (ie WRITE). The data can be shifted out of the register when the control line is LOW (ie READ).

Fig. 2.2 illustrates entry of the four bits 1010 into the register. Fig.2.3 shows the four bits (1010) being serially shifted out of the register and replaced by all zeros.

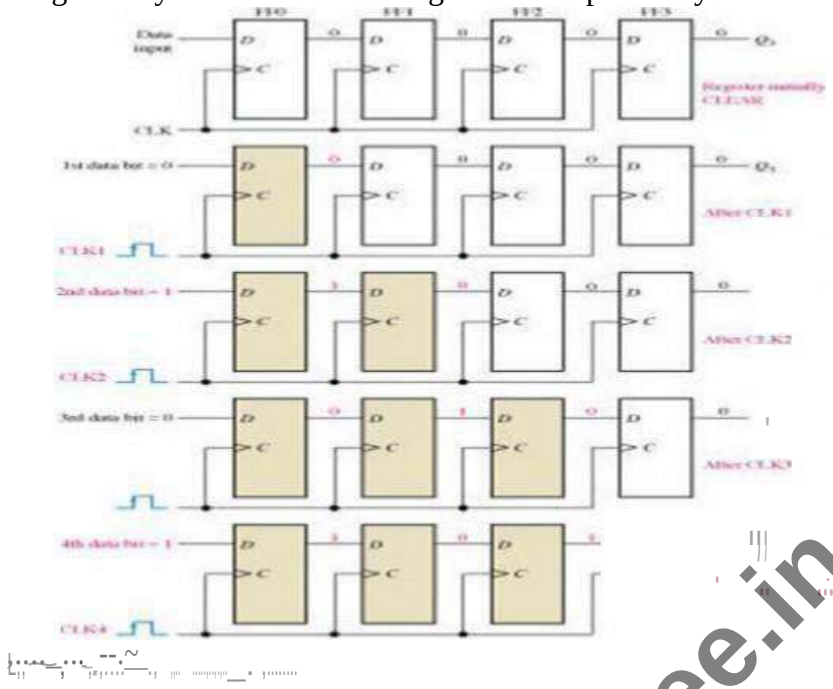


Figure 2.2: Four bi) being entered serially into the register.

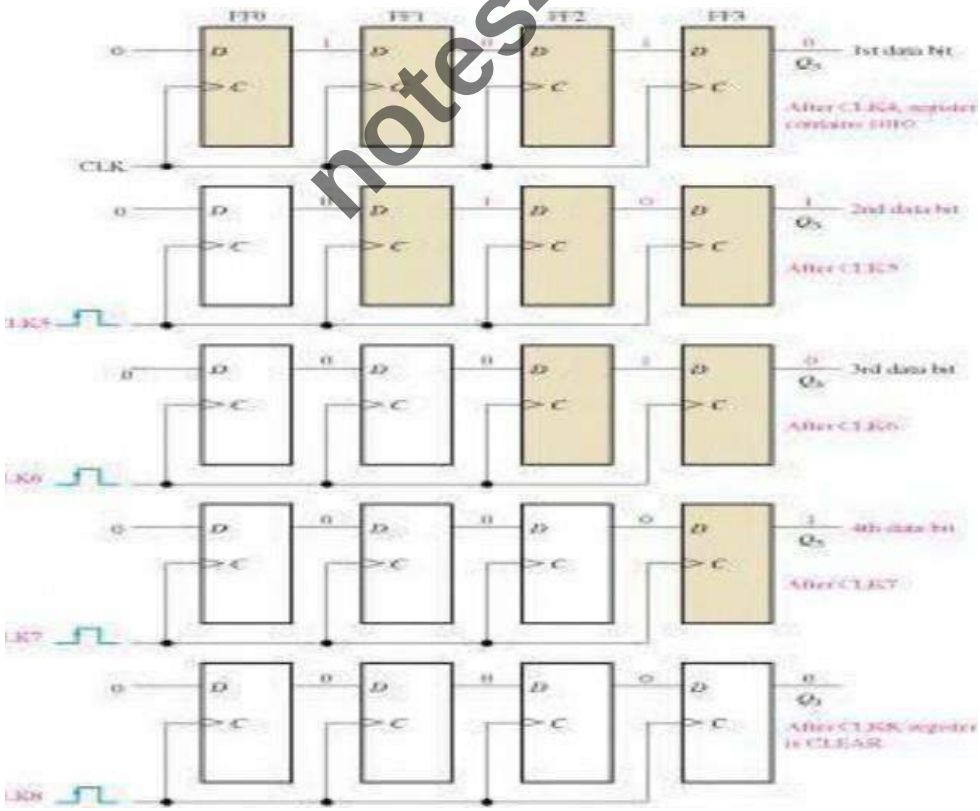


Figure 2.3: Four bits (1010) being serially shifted out of the register and replaced by all zeros

Serial In - Parallel Out Shift Registers

For this kind of register, data bits are entered serially in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. A construction of a four-bit serial in - parallel out register is shown below(Fig.2.4).

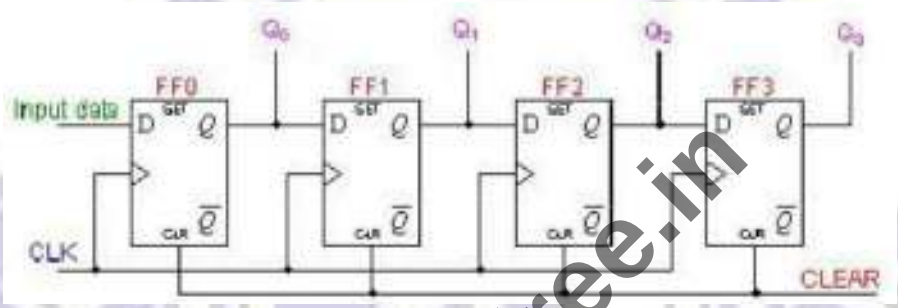


Fig.2.4: A four-bit serial in - parallel out register

Parallel In - Serial Out Shift Registers

A four-bit parallel in - serial out shift register is shown below. The circuit uses D flip-flops and NAND gates for entering data (ie writing) to the register.

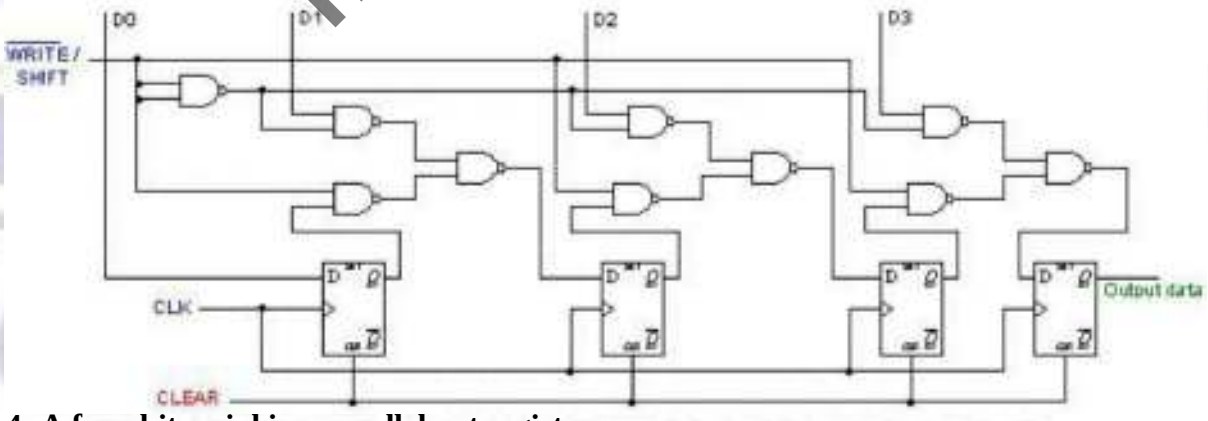


Fig.2.4: A four-bit serial in - parallel out register

D0, D1, D2 and D3 are the parallel inputs, where D0 is the most significant bit and D3 is the least significant bit. To write data in, the mode control line is taken to LOW and the data is clocked in. The data can be shifted when the mode control line is HIGH as SHIFT is active high.

Parallel In - Parallel Out Shift Registers

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by D flip-flops.

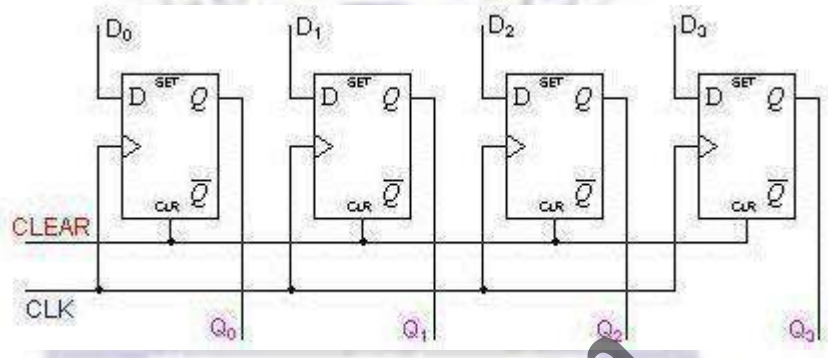


Fig.2. 5: parallel in - parallel out shift registers

The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously.

Bidirectional Shift Registers

The registers discussed so far involved only right shift operations. Each right shift operation has the effect of successively dividing the binary number by two. If the operation is reversed (left shift), this has the effect of multiplying the number by two. With suitable gating arrangement a serial shift register can perform both operations.

A bidirectional, or reversible, shift register is one in which the data can be shift either left or right. A four-bit bidirectional shift register using D flip-flops is shown below.

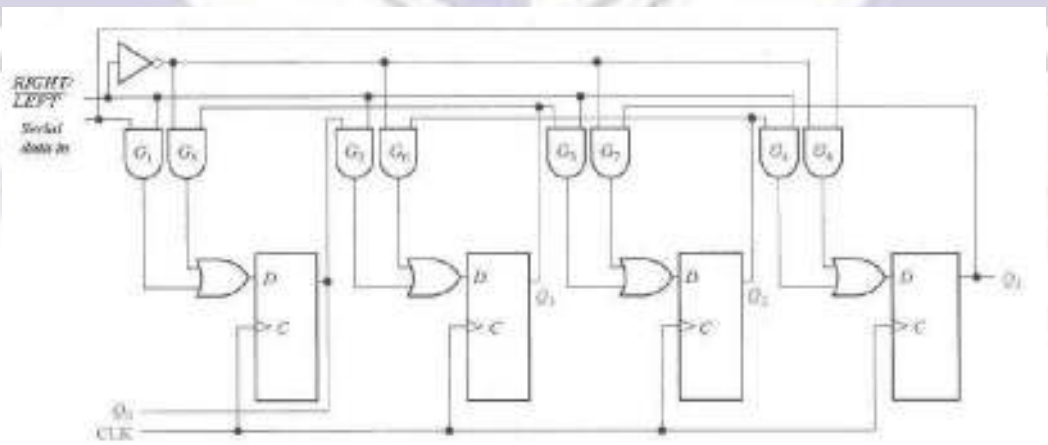
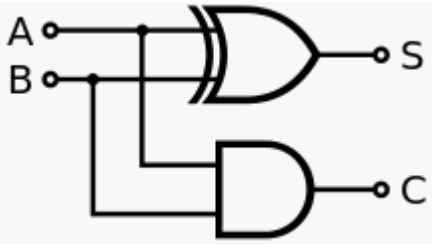


Fig.2.6: Bidirectional shift registers

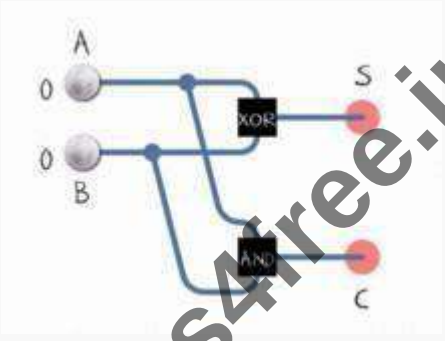
ADDER is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units or ALU.

Binary adders

Half adder



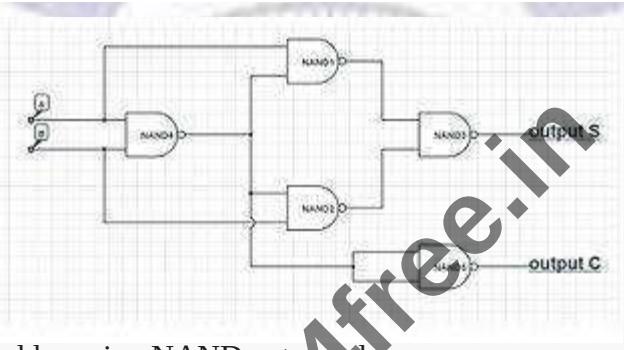
Half adder logic diagram



Inputs		Outputs	
A	**B**	**C**	**S**
0	0	0	0
1	0	0	1
0	1	0	1
1	1	1	0

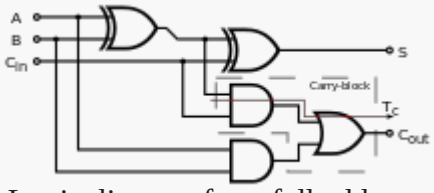
.

The **half adder** adds two single binary digits A and B. It has two outputs, sum (S) and carry (C). The carry signal represents an overflowinto the next digit of a multi-digit addition. The value of the sum in decimal system is 2C + S. The simplest half-adder design, pictured on the right, incorporates an XOR gate for S and an AND gate for C. The Boolean logic for the sum (in this case **S**) will be **A'B+AB'** whereas for carry (**C**) will be **AB**. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder.[1] The half adder adds two input bits and generates a carry and sum, which are the two outputs of a half adder. The input variablesof a half adder are called the augend and addend bits. The output variables are the sum and carry. The truth table for the half adder is:

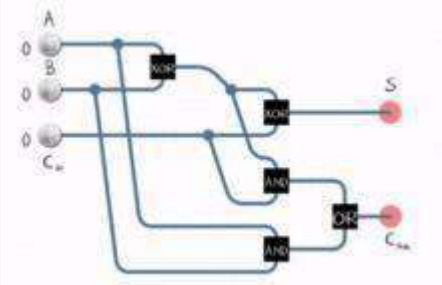


Half adder using NAND gates only.

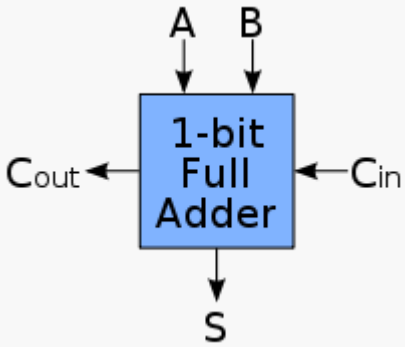
Full adder



Logic diagram for a full adder.



A full adder gives the number of 1s in the input in binary representation.



Schematic symbol for a 1-bit full adder with C_{in} and C_{out} drawn on sides of block to emphasize their use in a multi-bit adder

A **full adder** adds binary numbers and accounts for values carried in as well as out. A one-bit full-adder adds three one-bit numbers, often written as A, B, and C_{in}; A and B are the operands, and C_{in} is a bit carried in from the previous less-significant stage.[2] The full adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. bit binary numbers. The circuit produces a two-bit output. Output carry and sum typically represented by the signals C_{out} and S, where in decimal system.

A full adder can be implemented in many different ways such as with a custom transistor-level circuit or composed of other gates.

One example implementation is with and gate

In this implementation, the final OR gate before the carry-out output may be replaced by an XOR gate without altering the resulting logic. Using only two types of gates is convenient if the circuit is being implemented using simple IC chips which contain only one gate type per chip.

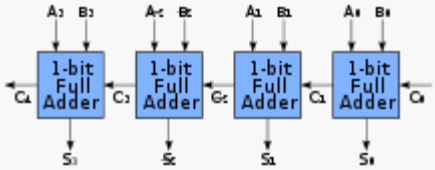
A full adder can also be constructed from two half adders by connecting and to the input of one half adder, then taking its sum-output(S) as one of the inputs to the second half-adder and as its other input, and finally the carry-outputs from the two half-adders are connected to an OR gate. The sum-output from the second half-adder is the final sum-output () of the full-adder and the output from the OR gate is the final carry-output (). The criticalath of a full adder runs through both XOR-gates and ends at the sum bit . Assumed that an XOR-gate takes 1 delays to complete, the delay imposed by the critical path of a full adder is equal to the critical path of a carry runs through 1 XOR-gate in adder and through 2 gates (AND and OR) in carry-block .

The truth table for the full adder is:

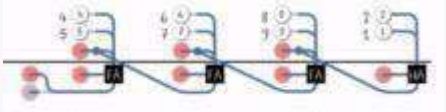
Inputs			Outputs	
A	**B**	**C_{in}**	**C_{out}**	**S**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Adders supporting multiple bits

Ripple-carry adder



4-bit adder with logical block diagram shown



Decimal 4-digit ripple carry adder. FA = full adder, HA = half adder.

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. This kind of adder is called a **ripple-carry adder** (RCA), since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder (under the assumption that $C_{in} = 0$).

The layout of a ripple-carry adder is simple, which allows fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic.

Multiplexer

Multiplexer, we can simply say that a circuit which can deliver single output from multiple inputs. It can often refer as **data selector or mux**. The inputs to this circuit may be Analog or Digital. It is very useful in sending large amount of data over a network with decrease in bandwidth and time. A single pole multi-positioned switch is a plain example of a multiplexer which is not having an electronic circuit or components. But for high speed switching, automatically selecting electronic multiplexers are implemented. Multiplexers that are built from transistors and relays are employed for analog applications. In digital applications, standard logic gates are used to build it. They are also termed as digital multiplexer.

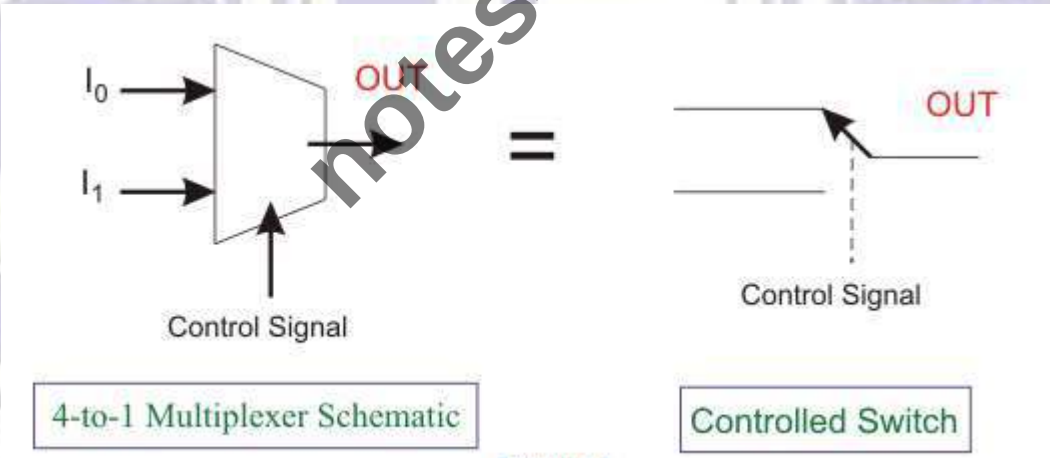
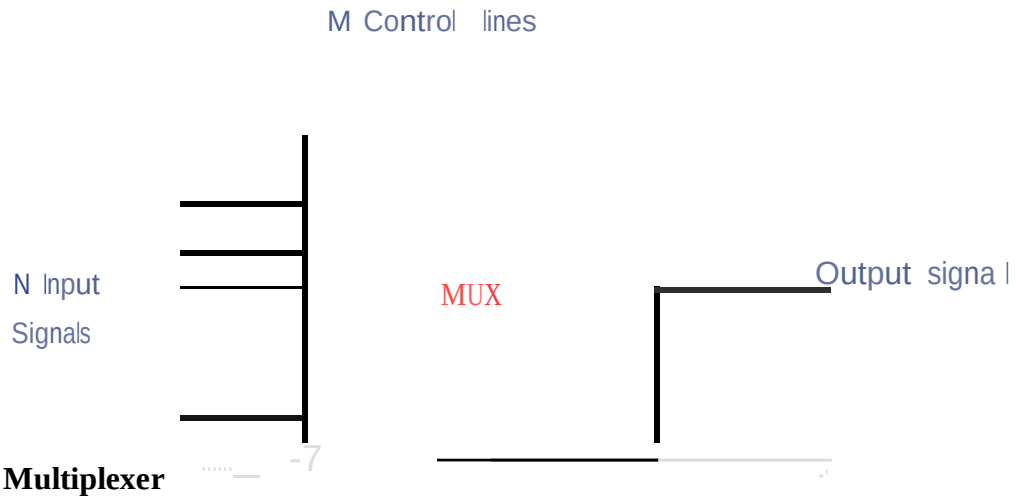


Figure 1

This circuit selects one of the inputs with the help of control signals and delivers that particular input into a single line as output. Therefore, it is also termed as data selector. The figure below shows the pin diagram of **multiplexer**



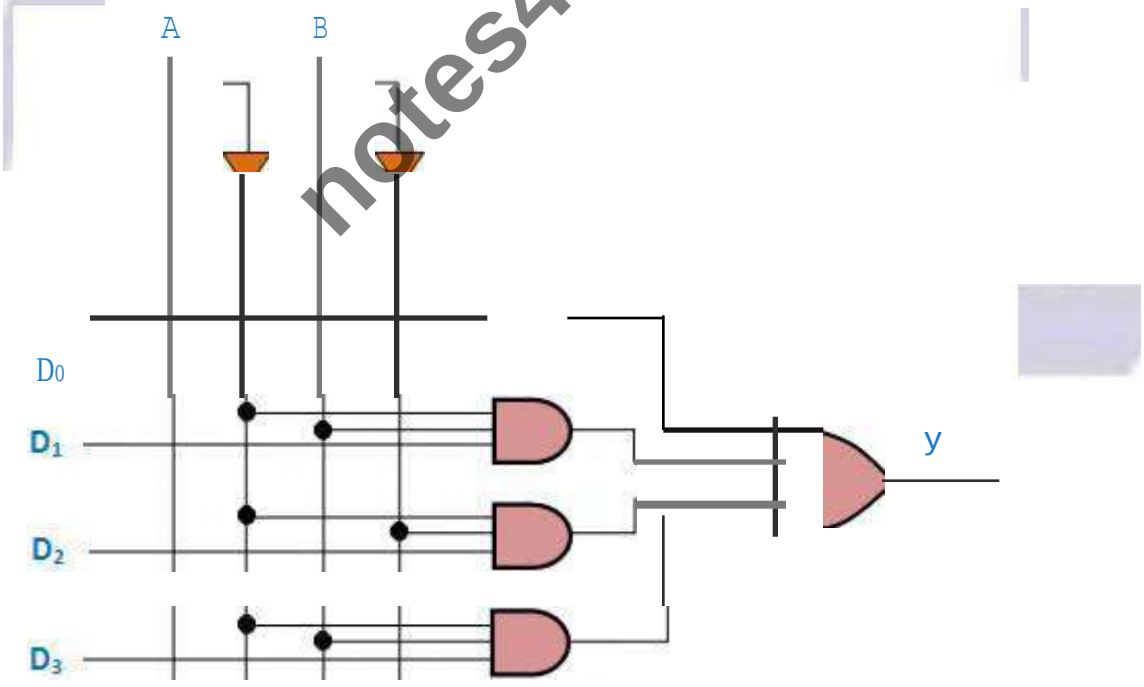
4 to 1 Multiplexer

For understanding the multiplexer, the details are the following: 4-to-1 Multiplexer. There are many others like 2-to-1, 8-to-1,

Inputs As the name indicates, D_0, D_1, D_2 and D_3.

Output The number of output

Control Bits Two control bits will decide which input bit should have been selected. The output clearly depends on this control bits.



If the condition AB = 00, the top most AND gate is enabled (shown in figure above). At this time, all the other three AND gates are in disabled condition. So, input bit D_0 is selected and transmitted as output. Thus, $Y = D_0$. If the condition AB = 11, every other AND gates are

disabled excluding the bottom most AND gate. So, input bit D_3 is selected and transmitted as output. Thus, $Y = D_3$. The examples of multiplexers are IC 74153, IC 45352 (4-to-1 multiplexers), IC 74150 (16-to-1 multiplexer)

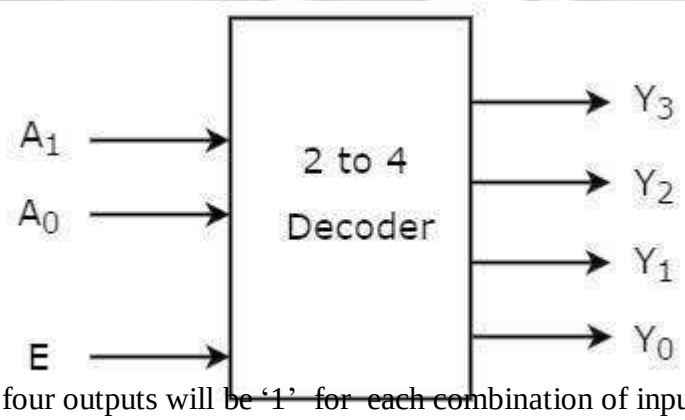
Applications of Multiplexer

Multiplexers are implemented in several fields where there is a necessity of transmitting large amount of data with use of single line. **Computer Memory** In computer, the huge quantity of memory is implemented by means of **multiplexers**. It also has advantage of reduction in number of copper lines which are used for the connection of memory to other parts in the computer. **Communication System** Multiplexer is implemented in this system to increase efficiency. Using a single transmission line, various types of data (video, audio etc) are transmitted at the same instant. **Telephone Network** Here, the multiple audio signals are brought into a single line and transmitted with the implementation of multiplexer. By this method, the numerous audio signals are made isolated and ultimately the recipient will receive the required audio signals. **Computer System of a Satellite Transmission Multiplexers** are implemented for the data signals to be transmitted from space craft or computer system of satellite to the earth by means of GPS.

Decoder

Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code. The outputs of the decoder are nothing but the **min terms** of 'n' input variables (lines), when it is enabled 2 to 4 Decoder

Let 2 to 4 Decoder has two inputs A_1 & A_0 and four outputs Y_3, Y_2, Y_1 & Y_0. The **block diagram** of 2 to 4 decoder is shown in the following figure.



One of these four outputs will be '1' for each combination of inputs when enable, E is '1'.

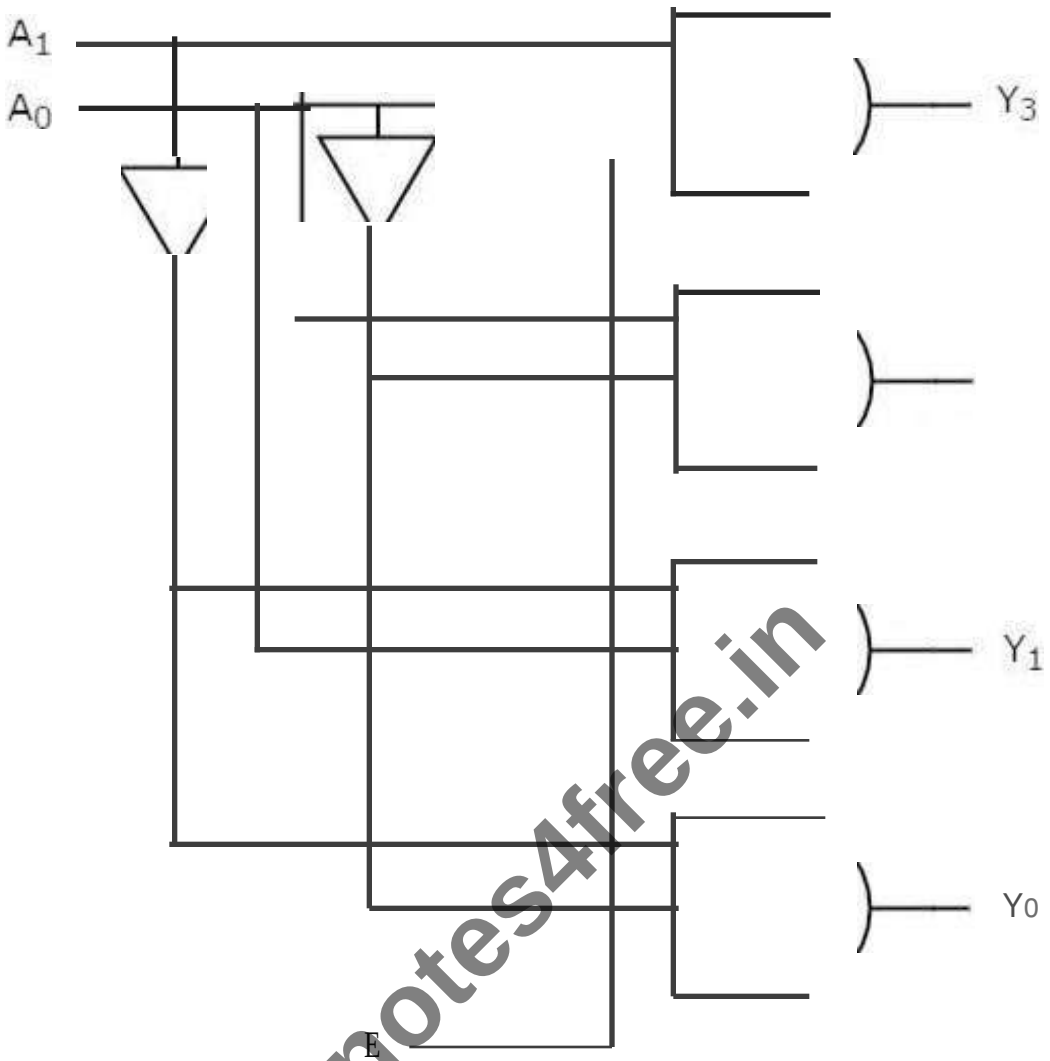
The **Truth table** of 2 to 4 decoder is shown below.

Enable	Inputs		Outputs			
E	**A_1**	**A_0**	**Y_3**	**Y_2**	**Y_1**	**Y_0**
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

From Truth table, we can write the **Boolean functions** for each output as

Y3=E.A1.A0Y3=E.A1.A0
Y2=E.A1.A0′Y2=E.A1.A0′
Y1=E.A1′.A0Y1=E.A1′.A0
Y0=E.A1′.A0′Y0=E.A1′.A0′

Each output is having one product term. So, there are four product terms in total. We can implement these four product terms by using four AND gates having three inputs each & two inverters. The **circuit diagram** of 2 to 4 decoder is shown in the following figure.

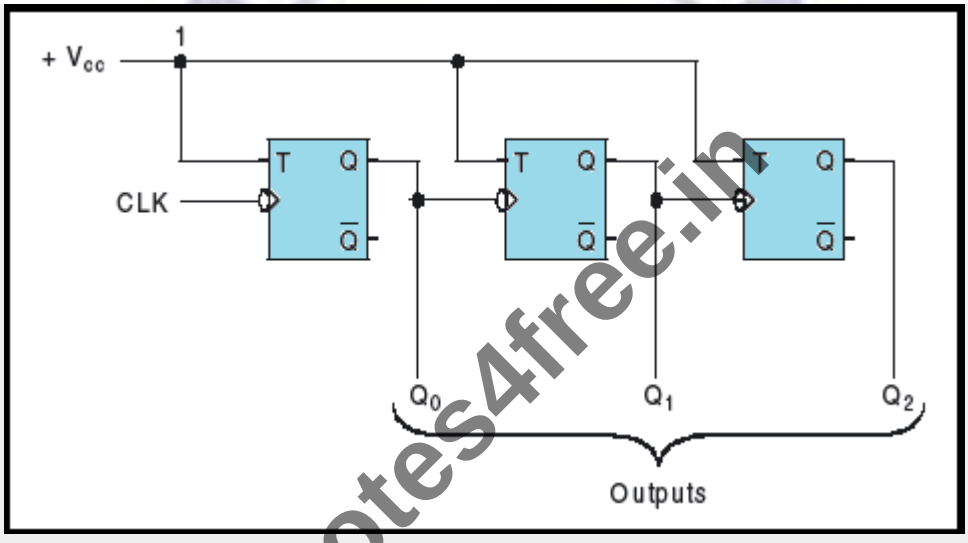


Therefore, the outputs of 2 to 4 decoder are nothing but the **min terms** of two input variables A_1 & A_0, when enable, E is equal to one. If enable, E is zero, then all the outputs of decoder will be equal to zero.

Similarly, 3 to 8 decoder produces eight s of three input variables A_2, A_1 & A_0 and 4 to 16 decoder produces sixteen min terms of four input variables A_3, A_2, A_1 & A_0.

Ripple counter

The main property of a ripple counter has in this counter all the flip flops are not driven by the same clock pulse. Here the clock pulse is applied to the first flip flop. And the successive **flip flop** is triggered by the output of the previous flip flop. So by this property it is very much clear that ripple counter has cumulative settling time, which limits its speed of operation. As the first stage of the counter changes its state first with the application of the clock pulse to the flip flop and the successive flip flops change their states in turn causing a ripple through effect of the clock pluses. As the signal propagates through the counter in a ripple fashion, it is called a ripple counter.in bellow you will find the block diagram of 3-bit ripple counter.

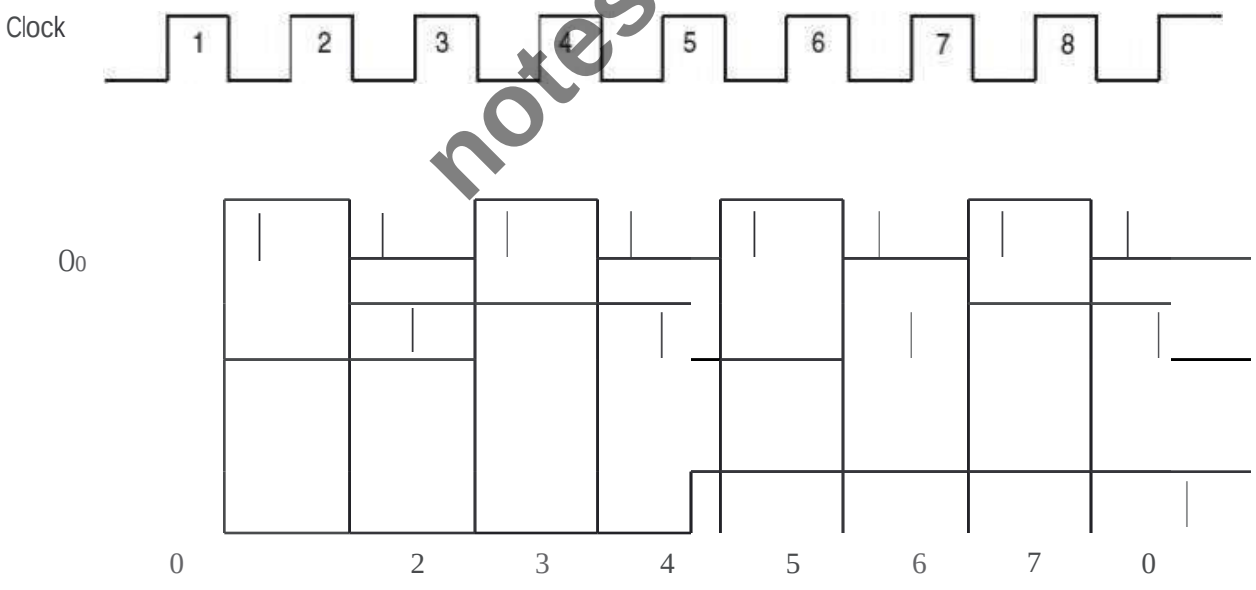


counter

By 3-bit ripple counter we can count 0-7. Because we know by 3 bit we can represents minimum 0 (000) and maximum 7 (111). The clock inputs of the three flip flops are connected in cascade. The T input of each flip flop is connected to a constant 1, which means that the state of the flip flop will toggle at each negative edge of its clock. Thus the clock input of the first flip flop is connected to the Clock line. The other two flip flops have their clock inputs driven by the Q output of the preceding flip flop. Therefore, they toggle their state whenever the preceding flip flop changes its state from Q = 1 to Q = 0, which results in a negative edge of the Q signal. So as we take the output from Q_0,Q_1,Q_2then we get the count sequence with different counter state as mention bellow on table.

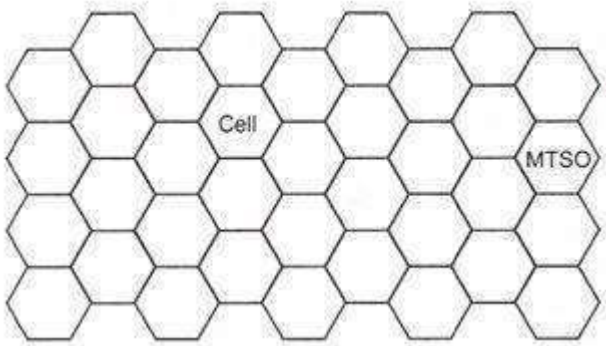
Counter State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Another very important thing we should know when we study ripple counter that the timing diagrams for it. Here in bellow you will see the timing diagram of three bit ripple counter.



Principle of operation of Mobile Phone

A cellular/mobile system provides standard telephone operation by full-duplex two-way radio at remote locations. It provides a wireless connection to the Public Switched Telephone Network (PSTN) from any user location within the radio range of the system.



The basic concept behind the cellular radio system is that rather than serving a given geographical area within a single transmitter and receiver, the system divides the service area into many small areas known as cells, as shown in Fig. below. The typical cell covers only several square kilometers and contains its own receiver and low-power transmitter. The cell area shown in Fig. below is ideal hexagon. However, in reality they will have circular or other geometric shapes. These areas may overlap, and cells may be of different sizes.

Basic cellular system consists of mobile stations, base stations and a mobile switching center (MSC). The MSC is also known as Mobile Telephone Switching Office (MTSO). The MTSO controls ’11 the cells and provides the interface between each cell and the main telephone office. Each mobile communicates via radio with one of the base stations and may be handed off (switched from one cell to another) to any other base station throughout the duration of the call.

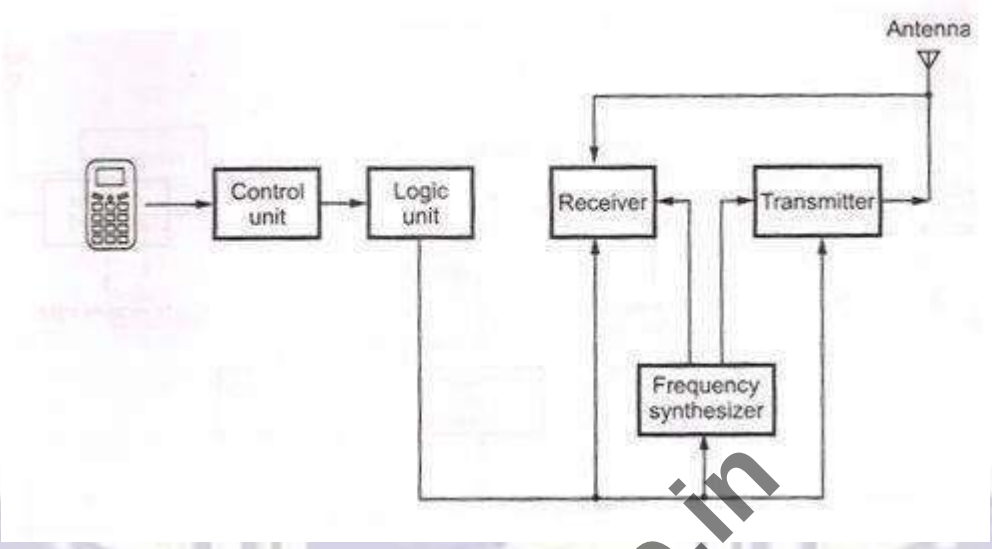
Each mobile station consists of a transceiver, an antenna and control circuitry. The base station consists of several transmitters and receivers which simultaneously handle full duplex communication and generally have towers which support several transmitting and receiving antennas. The base station serves as a bridge between all mobile users in the cell and connects the simultaneous mobile calls via telephone lines or microwave link to the MSC. The MSC co- ordinates the activities of all the base stations and connects the entire cellular system to the PSTN, most of the cellular system also provide a service known as roaming.

The cellular system operates in the 800-900 MHz range. The newer digital cellular systems have even greater capacity. Some of these systems operate in 1.7-1.8 GHz bands.

Cellular Telephone Unit

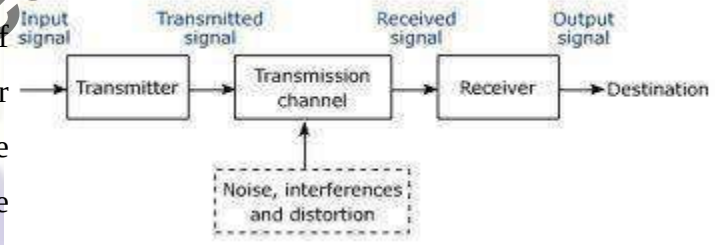
The Fig. below shows the block diagram of a cellular mobile radio unit. The unit consists of five major sections:

Transmitter, receiver, synthesizer, logic unit, and control unit. The mobile unit contains built-in rechargeable batteries to Provide operating power. The transmitter and receiver in the unit share the common antenna.



Components of communication system

The **communication system** basically deals with the transmission of information from one point to another using the well defined steps which are carried out in sequential manner. The system for data transmission makes use



of the sender and destination address, In this other so many elements are also there that allows it to transfer data from one set of point to another set of point after dividing the **elements of communication system** in groups and these interface elements acts as the main **component for data communication** and all these interface elements are given below-

Informationsource

The communication system which we are using is act as the main communication source for data transmission between two machines. Firstly, the source of data code is generated either in numeric form or in character form such that it should be in encrypted manner that does not provide information access to unknown or unauthorized user, this unit uses the specialized tools

and utilities for the generation of messages which is to be transmitted over the communication channel such that the signal can either be analog or digital in nature and it is converted from one form to another according to the compatibility of transmission medium that represents the signal nature. Moreover, the data source which is generated using the encoder has filter component that refines the data packets and removes data redundancy using the normalization technique.

Input Transducer

As you know that basic **work of the transducer** is to convert one form of energy into another form that can be electrical in nature. Let us consider that input source signal is non- electrical in nature then you have to first convert these signals in time varying electrical signal. For example- the microphone which we use in seminars and presentations converts message information into sound waves which is electrical in nature. Once you have successfully converted it into electrical signals then data compression technique is used which will compress data packets into single package so that it can be easily transmitted over the transmission lines because data compression reduces the size of the data packets to be transmitted.

Transmitter

The source generated electrical signals are then used by the **transmitter** after refining them and removes the noise and distortion there in it and makes signal in form that can be easily amplified, for the purpose of amplification in **transmitter circuit** we uses the digital modulator that converts sequence into electrical signals so that it can be easily transmitted over long distance. For example- In the wire telephony system, the modulation is used for the enhancement of the signal strength without the loss of the original data because using the ordinary antenna's it is not possible to reduce the noise and distortion during transmission of data signal.

Communication channel

The physical medium which is used for the **transmission of communication data signals** from sender to receiver is referred as **communication channel** and we can also say that it is the platform that allows the sending and receiving of the data packets using the well established path between two machines that can either be wire oriented or wireless such that both types of connections are supported by the point to point and broadcast channel, the various **communication channels** are used in it for the **data transmission** that depends on the type of the

network topology and circuit which we are using. Instead of this, the optical media is the best communication channel that provides fast and safe **data transmission** because tracing of the signals in it is impossible.

Receiver

The receiver machine work is to reproduce the message signal in electrical form from the noised and distorted signal such that digital demodulator is used that process the waveform signals into the sequence of numbers that represents the discrete values which is in form of zeros and ones and then these discrete signals are used for the reconstruction of information code from the attenuated signal.

Destination machine

The last stage of the **communication system** is destination machine which converts these electrical signals into its original form for the data broadcasting so that it can be easily understand by the end user or receiver and then this same sort of **communication process** is used for the acknowledgment of signals to sender machine.