EC 8453 - Linear Integrated Circuits

Unit - I

Basics of operational Amplifiers.

1.1. Current mirror & current source

A constant current source makes use of the fact that for a transistor in the active region of operation, the collector ct is relatively independent of collector Vce.

The transistors Q_1 & Q_2 are identical the base are tied together & the emitters are grounded. The two transistors have the same base to emitted voltage

$$V_{BE1} = V_{BE2}.$$

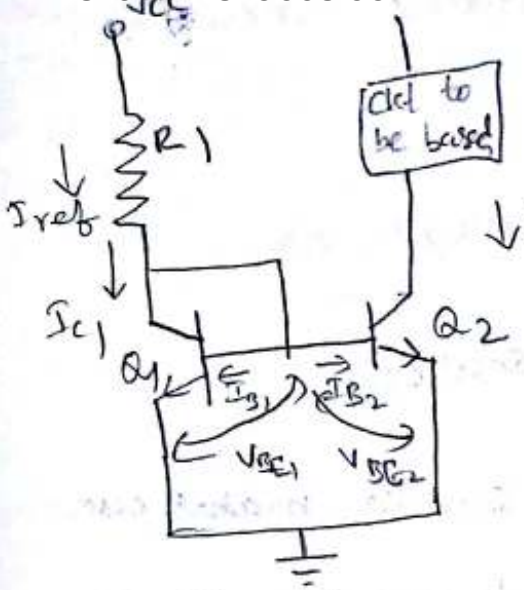
Q_2 is also active region & the collector cts of the two transistors will be approximately equal,

$$I_{C1} = I_{C2}$$

Analysis:

$$I_{C1} = \alpha_f I_{ES} e^{V_{BE1}/V_T} \longrightarrow (1)$$

$$I_{C2} = \alpha_f I_{ES} e^{V_{BE2}/V_T} \longrightarrow (2)$$



$\downarrow I_{C2} = I_0$

÷ by eqn ① & ②

$$\frac{I_{C2}}{I_{C1}} = e^{(V_{BE2} - V_{BE1})/V_T}$$

Since $V_{BE1} = V_{BE2}$

$$I_{C1} = I_{C2} = I_C = I_0$$

Since transistor are identical

$$\beta_1 = \beta_2 = \beta$$

Apply KCL at collector of Q_1 gives

$$I_{ref} = I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2}$$

$$I_{ref} = I_C \left(1 + \frac{2}{\beta}\right)$$

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}$$

$$I_{ref} = \frac{V_{CC}}{R_1}$$

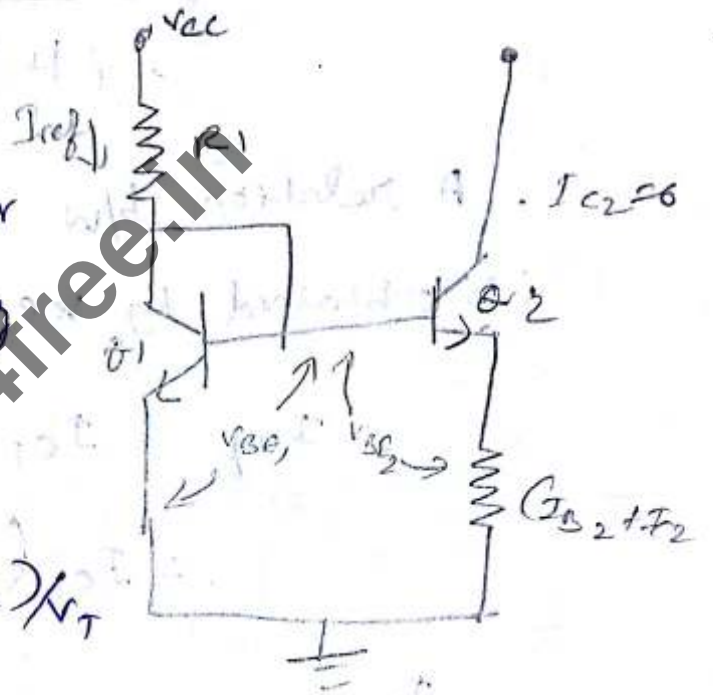
$$I_{ref} = I_C \left(\frac{\beta + 2}{\beta}\right)$$

$$\boxed{I_C = I_{ref} \left(\frac{\beta}{\beta + 2}\right)}$$

widlar current source

The operational amplifiers require very small input current. Therefore, the emitter coupled pair of transistors at the input are needed to be biased at, very low current with the collector current of order of 1uA.

Analysis:-



The ratio of collector current I_{C1} & I_{C2} using eqn is given by

$$\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T}$$

log of both sides.

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

KVL to the emitter based lobp :

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2}) R_E$$

Rearrange the above eqn.

$$V_{BE1} - V_{BE2} = \left(\frac{I_{B2}}{I_{C2}} + 1\right) I_{C2} R_E$$

By the circuit $\beta = \frac{I_{C_2}}{I_{B_2}}$

$$V_{BE_1} - V_{BE_2} = \left(\frac{1}{\beta} + 1\right) I_{C_2} R_E$$

$$\left(\frac{1}{\beta} + 1\right) I_{C_2} R_E = V_T \ln\left(\frac{I_{C_1}}{I_{C_2}}\right)$$

$$R_E = \frac{V_T}{\left(1 + \frac{1}{\beta}\right) I_{C_2}} \ln\left(\frac{I_{C_1}}{I_{C_2}}\right)$$

. A relation b/w I_{C_1} & the Ref current is obtained by KCL

$$I_{ref} = I_{C_1} + I_{B_1} + I_{B_2}$$

$$= I_{C_1}\left(1 + \frac{1}{\beta}\right) + \frac{I_{C_2}}{\beta}$$

$\frac{I_{C_2}}{\beta}$ is neglated.

$$I_{ref} = I_{C_1}\left(1 + \frac{1}{\beta}\right)$$

$\beta >> 1$

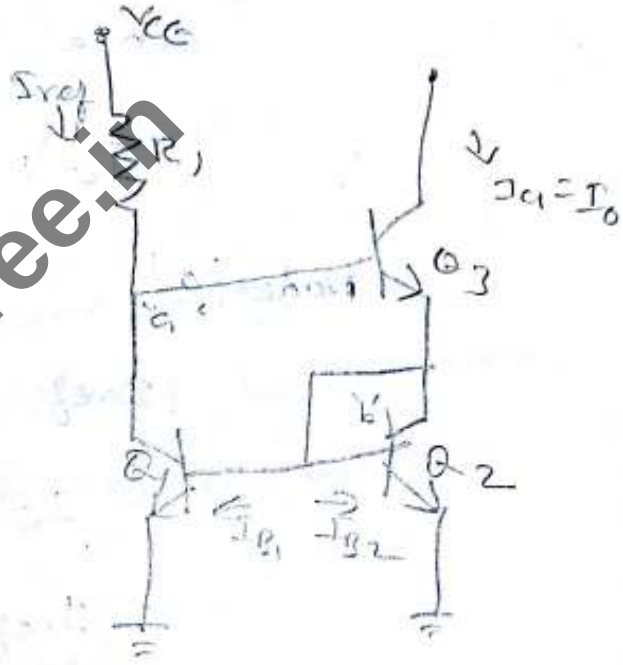
$$I_{C_1} = I_{ref}.$$

$$\boxed{I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}}$$

Current source as active load:-

This current source provides an o/p current (I_o) which is nearly equal to I_{ref} & also exhibits a very high o/p resistance.

An additional transistor Q_3 is connected to form a -ive feedback path which reduces the o/p resistance



Analysis:-

Since $V_{BE_1} = V_{BE_2}$

$I_{C_1} = I_{C_2}$

& $I_{B_1} = I_{B_2} = I_B$

At node 'b'

$$I_{E_3} = 2I_B + I_{C_2}$$

$$= \frac{2I_{C_2}}{\beta} + I_{C_2}$$

$$= \left(\frac{2}{\beta} + 1\right) I_{C_2} \quad \left(I_B = \frac{I_{C_1}}{\beta} = \frac{I_{C_2}}{\beta}\right)$$

$$= \left(\frac{2}{\beta} + 1\right) I_{C_2} \rightarrow (1)$$

$$I_{E_3} = I_{C_3} + I_{B_3} \rightarrow (2)$$

Compare eqn (1) & (2)

$$I_{C3}\left(1+\frac{1}{\beta}\right) = I_{C2}\left(1+\frac{2}{\beta}\right)$$

$$I_{C3}\left(\frac{\beta+1}{\beta}\right) = I_{C2}\left(\frac{\beta+2}{\beta}\right)$$

$$I_{C3} = I_o = I_{C2}\left(\frac{\beta+2}{\beta+1}\right)$$

since $I_{C1} = I_{C2}$

$$I_o = I_{C1}\left(\frac{\beta+2}{\beta+1}\right)$$

Node 'a'

$$I_{ref} = I_{C1} + I_{B3}$$

$$I_{C1} = I_o\left(\frac{\beta+1}{\beta+2}\right)$$

$$I_{ref} = I_o\left(\frac{\beta+1}{\beta+2}\right) + \frac{I_o}{\beta}$$

$$I_o = I_{ref}\left(\frac{\beta^2+2\beta}{\beta^2+2\beta+2}\right)$$

$$\boxed{I_o = I_{ref}\left(\frac{\beta^2+2\beta}{\beta^2+2\beta+2}\right)}$$

Voltage Source:-

A voltage source is a circuit that produces an output voltage V_o, which is independent of the load driven by the voltage source, or the output current supplied to the load. The voltage source is the circuit dual of the constant current source.

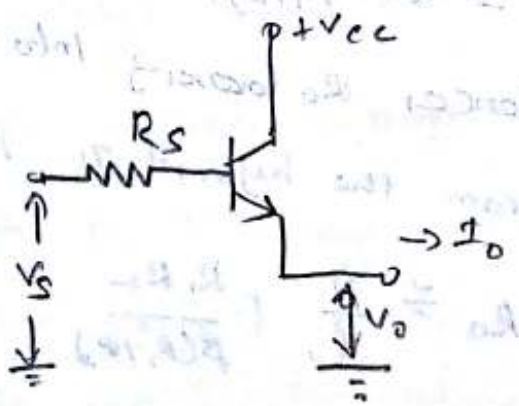
Voltage source circuit using impedance Transformation.

The voltage source circuit using the impedence transforming property of the transistor.

The output of AC resistance looking into emitter is given by

$$\frac{dV_o}{dI_o} = R_o = \frac{R_s}{\beta+1} + r_{eb}$$

The load regulation parameter indicates the changes in V_o resulting from large changes in O/p current I_o, Reduction in V_o occurs as I_o goes from no load current to full load current.



Emitter follower or Common collector type

Voltage source.

This voltage source is suitable for the different gain stage used in op-amps.

This circuit advantages of

i) producing low ac impedence.

ii) resulting in effective decoupling of adjacen gain stages.

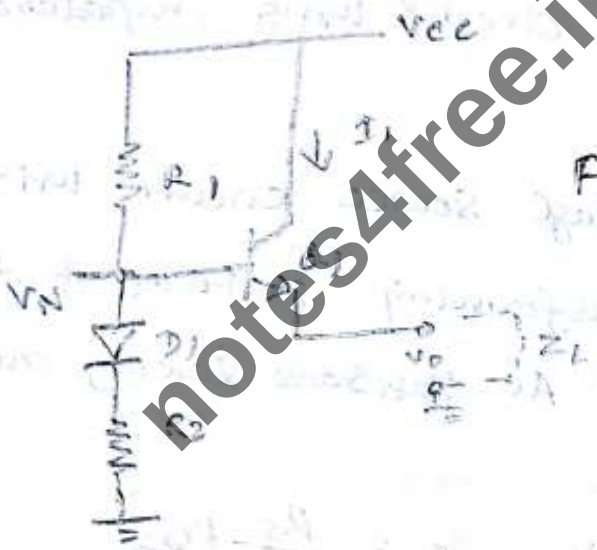


Fig. Voltage source using Common-Collector stage.

The low o/p impedance of the Common-collecto stage simulates a low impedance vge source with an output voltagelevel of V_o represented by

$$V_o \cong V_{cc}\left(\frac{R_2}{R_1+R_2}\right)$$

The impedance R_o looking into the emitter of Q_1 derived from the hybrid π model is given by

$$R_o \cong \frac{V_T}{I_1} + \frac{R_1 R_2}{\beta(R_1+R_2)}$$

Voltage Reference.

The ckt that is primarily designed for providing a constant vge independent of changes in temperature is called vge reference.

The function of a voltage reference is to provide a stable dc voltage starting from a less stable power source.

The temperature co-efficient of the output reference vge, it is given by

$$T_{C\cdot R} = \frac{dV_R}{dT}$$

Performance specification of vge reference

→ line regulation.

→ load regulation.

→ Ripple Rejection ratio

→ Thermal Co-efficient.

Bandgap voltage reference.

The reference voltage is constant & determined by the VBG which is bandgap voltage, this circuit is called band gap voltage reference circuit.

If the supply voltage is 6V (or) less than the reference voltage is developed from highly predictable V_{BE}.

$$V_R = V_{BE3} + I_2 R_2$$

Assume all transistors all identical.

$$I_b = I_2 e^{\Delta V_{BE}/V_T}$$

$$= I_2 e^{\left(\frac{V_{BE1} - V_{BE2}}{V_T}\right)}$$

$$= I_2 e^{\left(\frac{I_2 R_3}{V_T}\right)}$$

$$(\text{or}) \quad I_2 R_3 = V_T \ln \frac{I_1}{I_2}$$

Neglating the base current of Q_2

$$I_{E2} = I_{C2}$$

$$I_2 R_2 = I_2 R_3$$

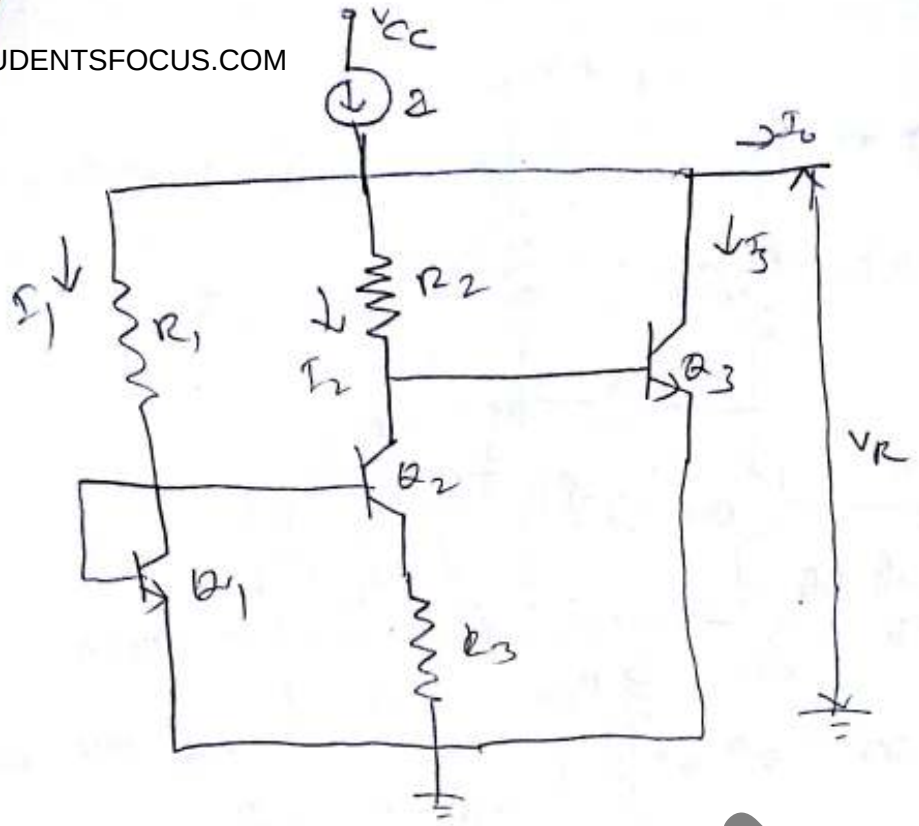
$$\frac{R_3}{R_3} R_2$$

$$= \frac{R_2}{R_3} V_T \ln \left(\frac{I_1}{I_2}\right)$$

$$V_R = V_{BE3} + \frac{R_2}{R_3} V_T \ln \left(\frac{I_1}{I_2}\right)$$

$$V_R = V_{GO} + 3V_T$$

V_{GO} -> bandgap voltage at absolute zero



1. Differential amplifier using BJT.

- Differential amplifier with resistive loading
- Differential amplifier with active loading.

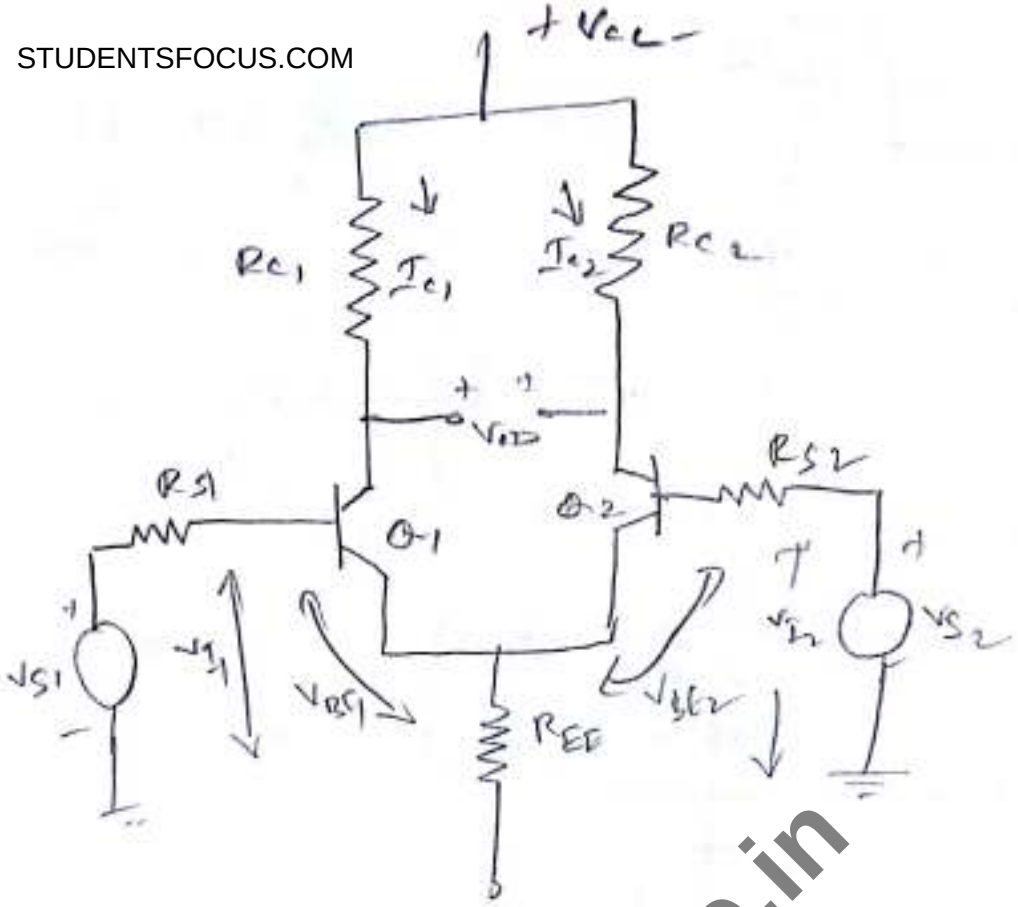
DC analysis of an emitter-coupled pair.

In dc analysis the transistors Q_1 & Q_2 are assumed as identical.

Let us consider $\beta >> 1$

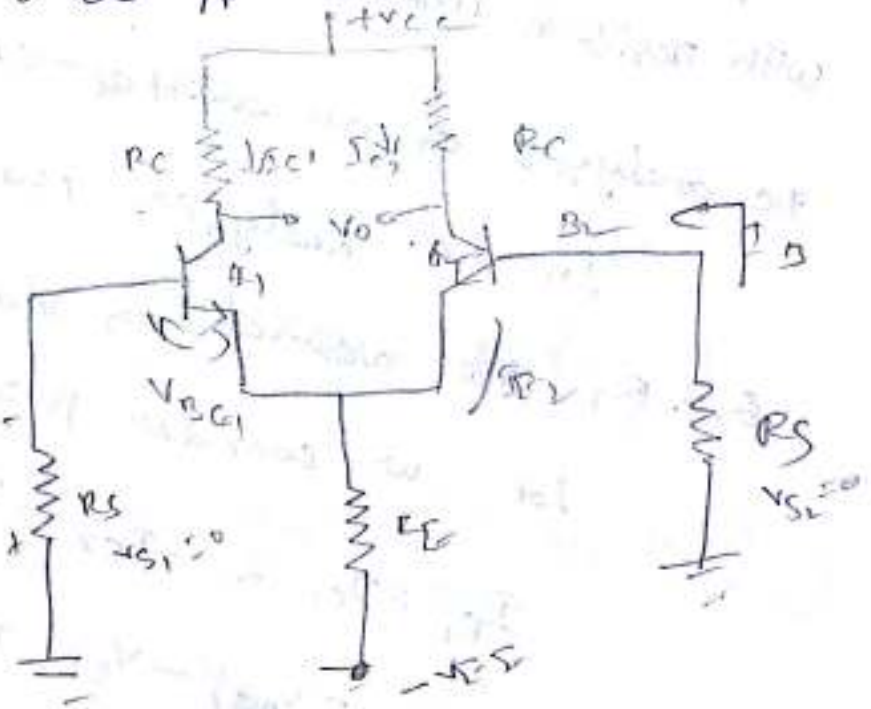
$$I_{E1} = I_{C1} \;\&\; -I_{E2} = I_{C2}$$

$$V_{I1} = V_{BE1} - V_{BE2} + V_{I2}$$



By using this analysis the operating point values can be obtained. ie V_{CQ} & V_{CEQ}

The DC equivalent ckt can be derived by making DC i/p zero.



1. (B)

or matched transistor pairs we have

$$R_E = R_{C1} \| R_{E2} \quad \text{since } R_{C1} = R_{E2}$$

$$R_{C1} = R_{C2} = R_C$$

$$|V_{CC}| = |V_{EE}|$$

Applying KVL to base emitter loop of Q1 we get

$$I_B R_S + V_{BE} + 2 I_E R_E = V_{EE} \rightarrow (1)$$

For common emitter configuration

$$\beta = \frac{I_C}{I_B} \quad \& \quad I_C = I_C$$

$$\beta = \frac{I_E}{I_B} \rightarrow (2)$$

Sub (2) in (1)

$$\frac{I_E}{\beta} R_S + V_{BE} + 2 I_E R_E = V_{EE}$$

$$I_E \left(\frac{R_S}{\beta} + 2 R_E \right) = V_{EE} - V_{BE}$$

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2 R_E}$$

$\frac{R_S}{\beta} << 2R_E$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E}$$

The emitter current I_E is independent of

When $I_E >> I_C$

Applying KVL to the collector based loop

we get

$$V_{C'} = V_{CC} - I_C R_C \rightarrow (1)$$

& $$V_{CE} = V_C - V_E \rightarrow (2)$$

(2) in (1)

$$V_{CE} = V_{CC} - I_C R_C - V_E$$

$V_E = -V_{BE}$

$$V_{CE} = V_{CC} + I_C R_C + V_{BE}$$

The above eqn

$$V_{CE\,Q} = V_{CC}$$

$\therefore$ When $I_E = I_C = I_{CQ}$.

DC Characteristics of op-amp.

The ideal op-amp does not allow the ct from the source & its response is also independent of temperature

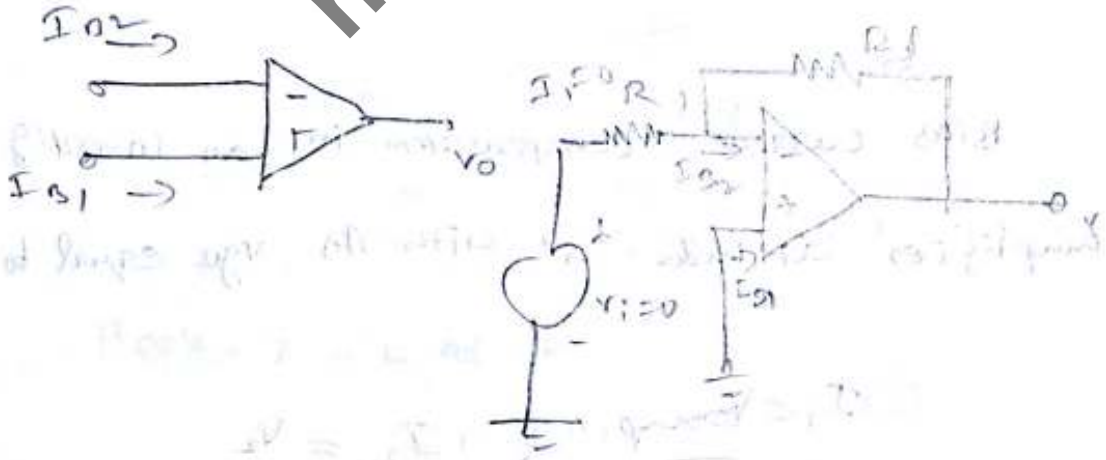
i) input bias current

The avg value of the two base currents flowing into the op-amp i/p terminals is called i/p bias current.

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

I_{B1} → DC bias ct flowing into the non inverting i/p

I_{B2} → DC " " " " inverting i/p.



Input bias current is equal to the input current I_{B1} & I_{B2}

$$I_B = I_{B1} = I_{B2}$$

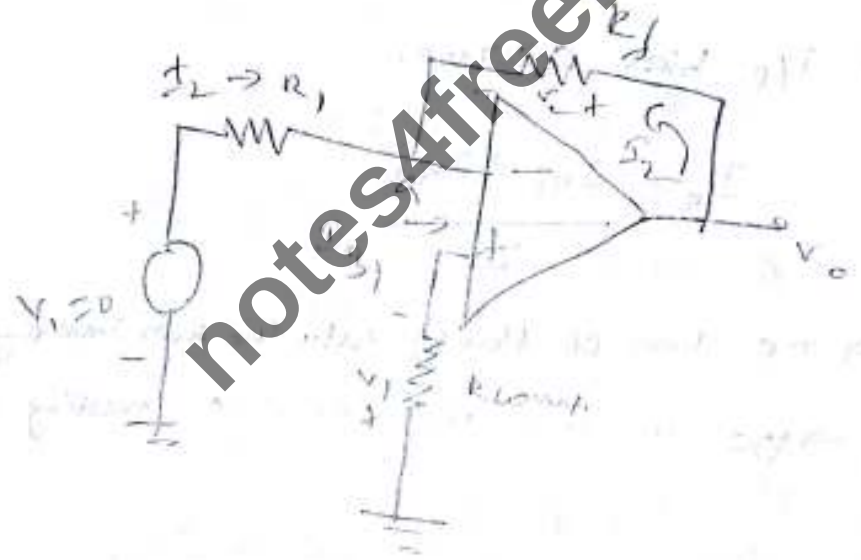
The O/p vge is given by

$$V_o = I_{B_2} R_f$$

The value of R_{comp} derived as

$$V_{comp} = I_{B1} R_{comp}$$

$$I_{B1} = \frac{V_{comp}}{R_{comp}}$$



Bias current compensation in an inverting amplifier at node 'a' with its vge equal to $-V_{comp}$

$$I_1 = \frac{V_{comp}}{R_1} \quad \& \quad I_2 = \frac{V_2}{R_f}$$

Applying KCL at node 'a' we get

$$I_{BL} = I_2 + I_1$$

$$= \frac{V_{comp}}{R_f} + \frac{V_{comp}}{R_1}$$

$$= V_{comp}\left(\frac{R_1 + R_f}{R_1 R_f}\right)$$

$$= \frac{V_{comp}}{R_{comp}}\left(\frac{R_1 * R_f}{R_1 + R_f} = R_{comp}\ (R_1 \| R_f)\right)$$

Input offset current (I_{OS})

The i/p transistors cannot be made identical & there always exists a small difference b/w the bias currents I_{B1} & I_{B2}. This difference is called the offset current.

$$I_{OS} = |I_{B1}| - |I_{B2}|$$

$$V_{comp} = I_{B1} \cdot R_{comp}$$

$$\& \quad I_1 = \frac{V_{comp}}{R_1} \quad \text{—(1)}$$

Applying KCL at node a

$$I_2 = I_{B2} - I_{B1} \quad \text{—(2)}$$

sub (2) in (1)

$$I_2 = I_{B2} - I_{B1}$$

$$= I_{B2} - \frac{I_{B1} R_{comp}}{R_1}$$

$$V_0 = I_2 R_f - I_{B1} R_{comp}$$

$$V_o = R_f (I_{B2} - I_{B1})$$

$$V_o = R_f I_{OS}$$

Input offset voltage

whenever both the i/p terminals are grounded ideally the o/p vge of the op-amp should be zero

This DC vge which makes the o/p vge zero when the other terminal is grounded is called i/p offset vge.

Thermal Drift :-

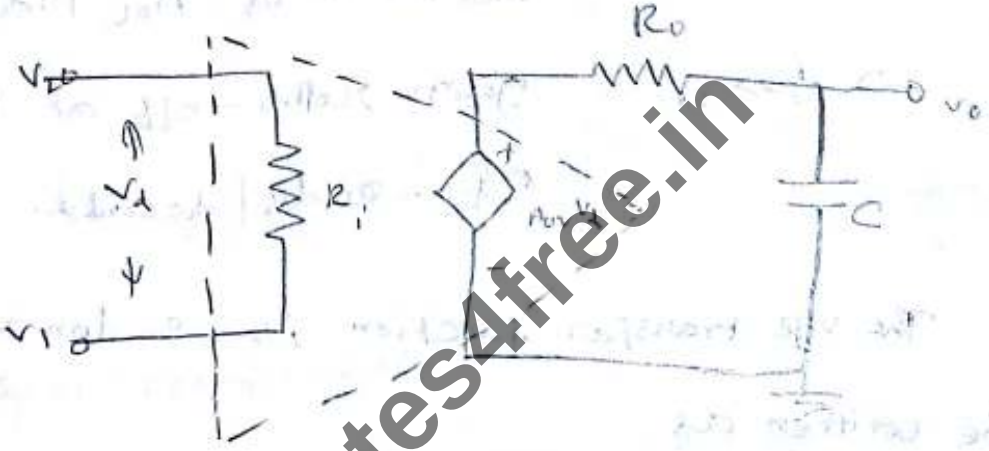
The op-amp parameters like bias current, offset current & offset vge will change with temperature.

The term thermal drift is used to identify such changes & it is defined as the avg rate of change of input offset voltage per unit change in temperature.

Characteristics of Op-amp.

Frequency response :-

Ideally an op-amp should have an ∞ bandwidth. This means the gain of op-amp must remain same for all the frequencies from 0 to ∞. But practically op-amp gain however yes at higher frequencies.



The open loop Vge gain of an op-amp is obtained from

$$V_o = \frac{-jX_c}{R_o - jX_c} A_{OL} V_d$$

$$A = \frac{V_o}{V_d} = \frac{A_{OL}}{1 + j2\pi f R_o C}$$

$$A = \frac{A_{OL}}{1 + j(f/f_1)} \qquad f_1 = \frac{1}{2\pi R_o C}$$

magnitude $|A| = \dfrac{A_{OL}}{\sqrt{1+(f/f_1)^2}}$

phase angle $\varphi = 0 - \tan^{-1}(f/f_1)$.

→ $f << f_1$ magnitude of the gain is 20log

→ $f = f_1$ gain is 3 dB down from the dc value of A_{OL} in dB.

→ $f >> f_1$ gain rolls-off at the rate of -20 dB / decade.

The vge transfer function is s-domain can be written as

$$A = \frac{A_{OL}}{1 + s(f/f_1)} = \frac{A_{OL}}{1 + j(\omega/\omega_1)}$$

$$= \frac{A_{OL}\cdot\omega_1}{j\omega + \omega_1} = \frac{A_{OL}\cdot\omega_1}{s+\omega_1}$$

$$A = \frac{A_{OL}\cdot\omega_1\cdot\omega_2\cdot\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}$$

Frequency compensation.

→ External compensation. → Dominat Pole
→ Pole zero
→ miller effect

→ Internal Compensation.

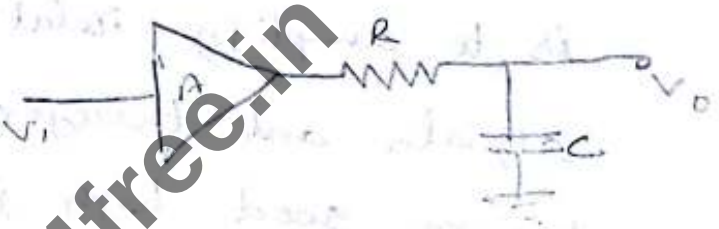
Dominant - pole compensation

Assume A is the uncompensated transfer function of an open loop op-amp with three break frequencies

$$A' = \frac{A_{OL}}{(1+j f/f_d)(1+j f/f_1)(1+j f/f_2)(1+j f/f_3)}$$

$$f_d < f_1 < f_2 < f_3$$

$$f_d = \frac{1}{2\pi RC}$$



Pole-Zero compensation

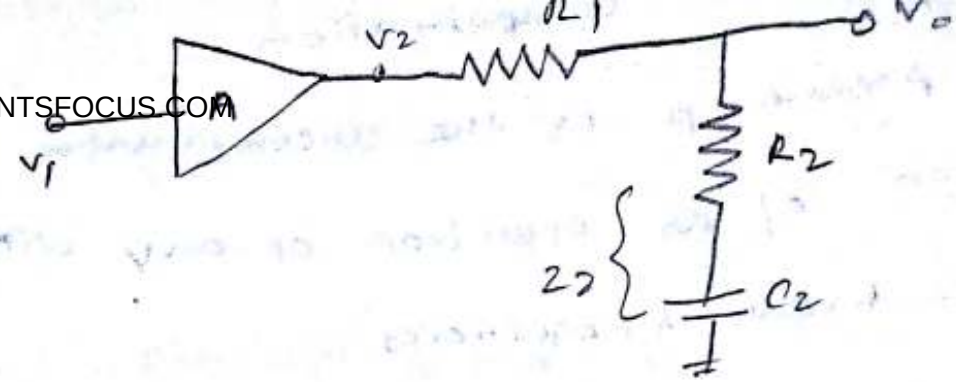
Consider the same op-amp described by open loop gain

$$A' = \frac{V_0}{V_1} = A \cdot \frac{R_2}{R_1+R_2} \cdot \frac{1+j\frac{f}{f_1}}{1+j\frac{f}{f_0}}$$

$$= \frac{A_{OL}}{(1+j\frac{f}{f_0})(1+j\frac{f}{f_2})(1+j f/f_3)}$$

$$(0 < f_0 < f_1 < f_2 < f_3)$$

$R_2 >> R_1$ so that $\frac{R_2}{R_1+R_2} \approx 1$.



Internally frequency compensation :-

Broad bw may not be the only excitation required in some applications instrumentation ckt. The op-amp required is to amplify relatively slow changing signals and therefore it does not require good high frequency response in such case internally compensated op-amps are used.

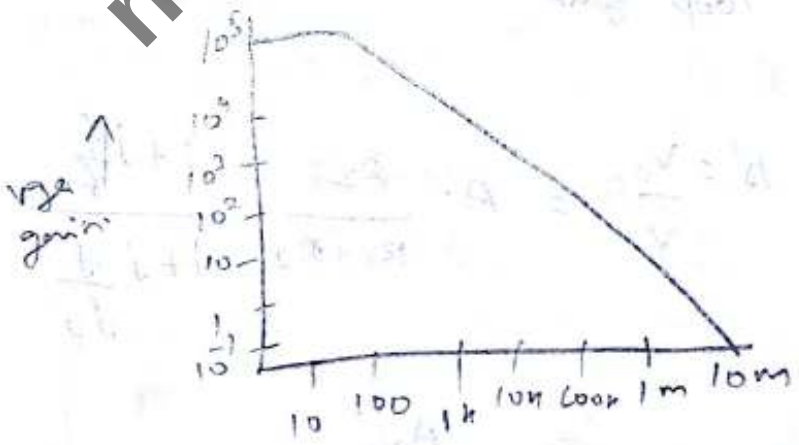


Fig Frequency respons of MA 7 op-

The 741 op-amp internally contains a capacitance of 30 PF that cuts off the sgl current at higher frequencies.

Slew rate:-

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μs

The rate at which the voltage across the capacitor v_c rises is given by

$$\frac{dv_c}{dt} = \frac{I}{C}$$

$$SR = \left.\frac{dv_c}{dt}\right|_{max} = \frac{I_{max}}{C}$$

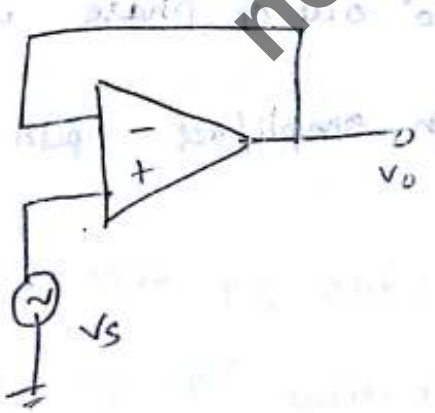


Fig:- Voltage follower

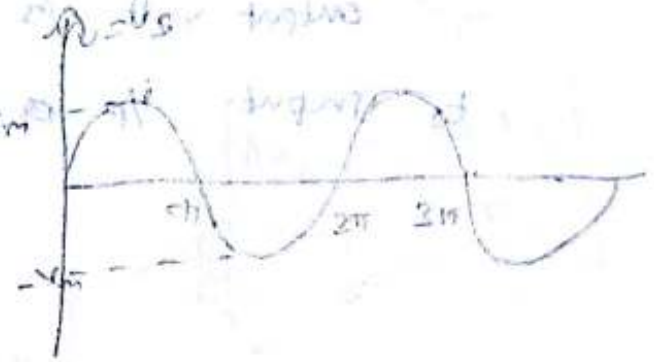


Fig i/p & o/p waveform

The max rate of change of the o/p occurs

$$SR = \left.\frac{dv_o}{dt}\right|_{max} = \omega V_m .$$

$$\boxed{\text{Slew rate} = 2\pi f V_m \ V/s}$$

open loop op-amp configuration:

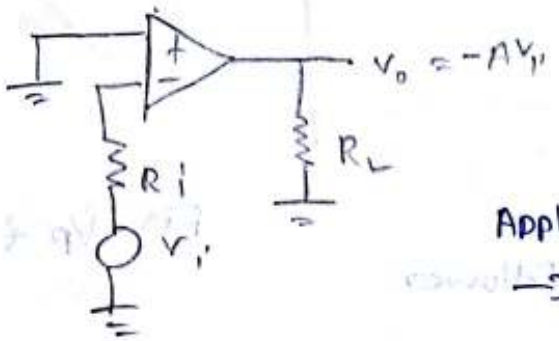
open loop is defined as there is no f/b to the i/p to o/p. In this op-amp has a very high gain.

Differential:

$$V_o = A(V_{i1} - V_{i2})$$

Inverting Amp:

output volt is 180° out of phase with respect to input. i/p sign amplified open loop gain



Application:

→ wave shaping.

→ filtering etc.

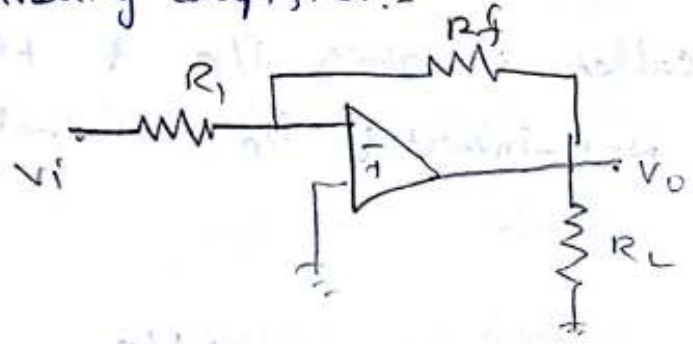
→ Solving mathematical operation

Closed loop Configuration:-

It is defined as providing f/b from o/p & i/p directly (or) through another n/w.

F/b is divided into two type -ive f/b & +ive f/b.

Inverting amplifier:-



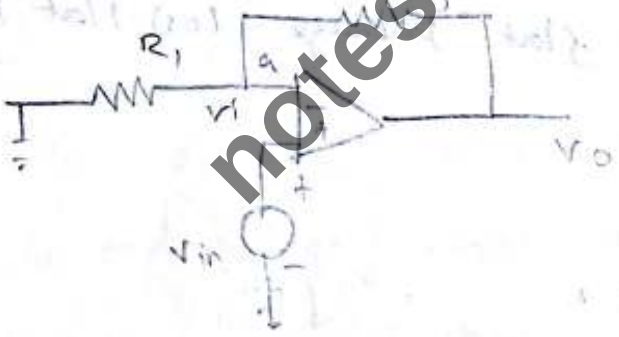
$i = \frac{V_i}{R_1}$

$V_o = -i_1 R_f$

$A_{CL} = \frac{V_o}{V_i} = \frac{-R_f}{R_i}$

$\boxed{V_o = -\frac{V_i R_f}{R_1}.}$

Non-inverting amplifier.

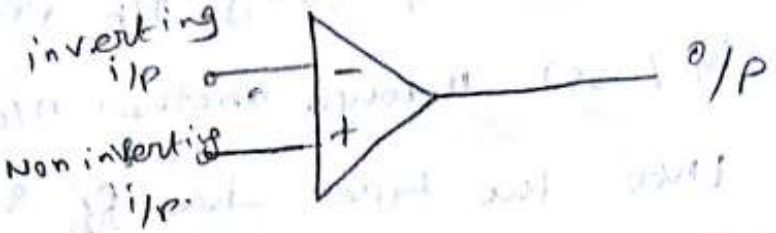


$A_{CL} = \frac{V_o}{V_{in}}$

$\boxed{A_{CL} = 1 + \frac{R_f}{R_1}}$

If sign f/b is out of phase by 180° with respect to i/p it is called as -ive f/b (or) degenerative feedback.

Basic information about op-amp:-



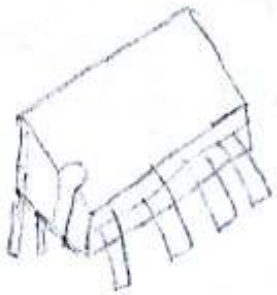
It has two i/p & one o/p terminal -ive sign is called inverting i/p & +ive sign is called Non-inverting i/p terminal.

Packages:-

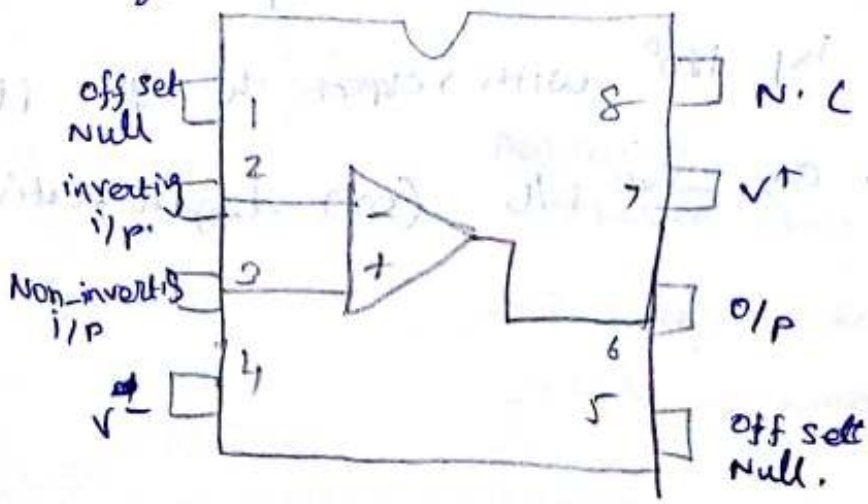
Three popular packages available

1) The metal can (To) package
2) The dual-in-line Package (DIP)
3) The flat package (or) Flat pack.

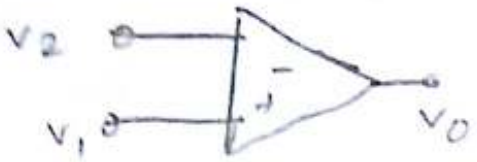
TO-5 Style package with Straigh leads.



Dual-in-line plastic package



Block diagram:



If $V_1 = 0$ o/p V_0 is 180° out of phase with i/p sgl V_2

If $V_2 = 0$ V_0 inphase with i/p sgl applied at V_1.

Open loop voltage gain $A_{OL} = \infty$

input impedence $R_i = \infty$

output impedance $R_o = 0$

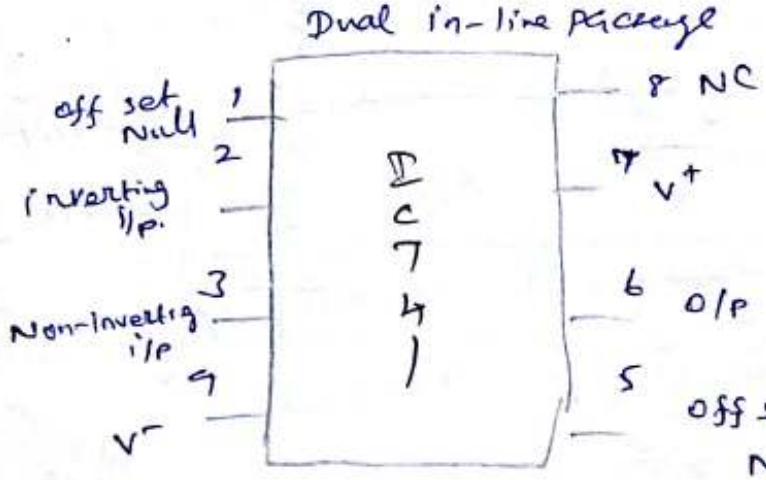
Bandwidth $BW = \infty$.

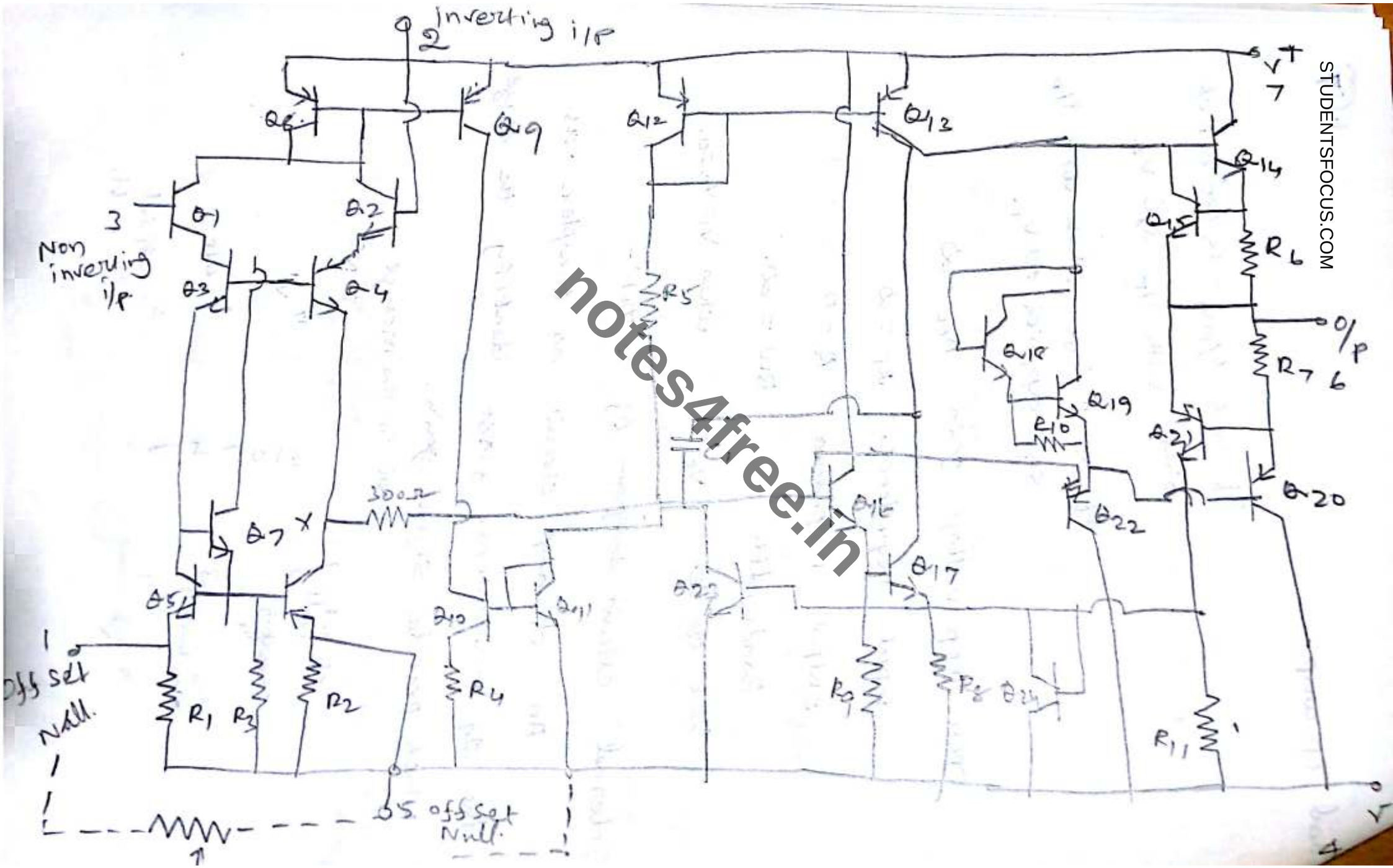
Zero off set $V_o = 0$ when $V_1 = V_2 = 0$.

Internal circuit diagram of IC 741 :-

An opamp circuit as complex as the 24 transistors. first identify the stage which provide signal gain.

Dual in-line package




2 inverting i/p
3
Non inverting i/p
1
offset Null
5 offset Null
4
6 o/p
7
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
R1
R2
R3
R4
R5
R6
R7
R8
R9
R11
300Ω
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General operational amplifier stages.

An operational amplifier generally consist of three stages.

i) differential amplifier

ii) additional amplifier stages to provide the required voltage gain and dc level shifting

iii) An emitter follower or source follower o/p stage to provide current gain.

Input Stage:

The input differential amplifier stage uses P-Channel JFET's and the three transistor active load formed. The bias current for the stage is provided by a two transistor current source using PNP transistors.

Gain Stage:-

The second stage or the gain stage uses Darlington transistor pair formed by the transistor. It is connected as an emitter follower, providing large input resistance. Therefore, it minimizes the loading effect on the input differential amplifier stage.

Output Stage:-

The final stage of the op-amp is a class AB Complementry push pull output stage. The emitterfollower, providing a large input resistance for minimizing the loading effects on the gain stage.

The overall voltage gain A_v of the op-amp is the product of voltage gains of each stage as given by

$$A_v = |A_1||A_2||A_3|.$$

$A_1 \rightarrow$ gain of the differential amplifier stage.

$A_2 \rightarrow$ gain of the second gain stage.

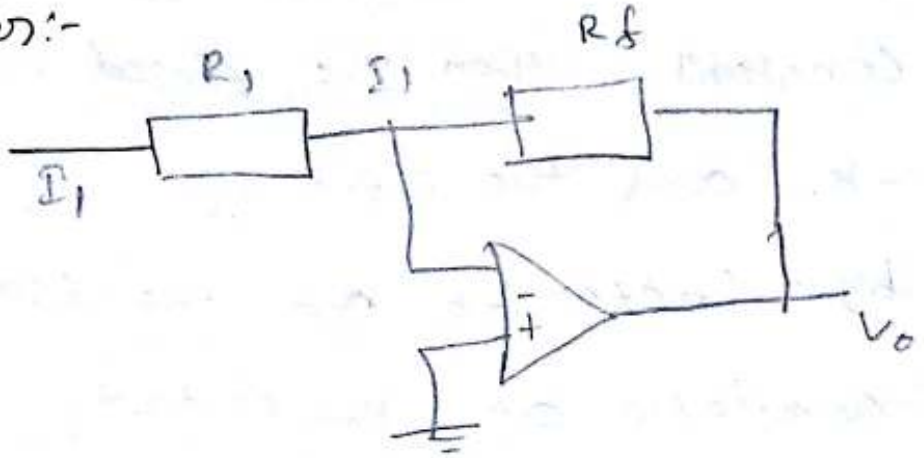
$A_3 \rightarrow$ gain of the output stage.

8/11/12

Unit - II

APPLICATION OF OPERATIONAL AMPLIFIE

Sign changer:-



An op-amp with input impedance Z_1 and Feed back impedance Z_f. If the impedance Z_1 and Z_f are equal in magnitude & phase then the closed loop voltage gain is -1 and i/p sgl will undergo a 180° phase shift at the output Hence such a circuit is also called phase inverter.

If two such amplifier are connected in cascade, then the o/p from the second stage is the same as the input sgl without any change of singn.

Scale changer:-

If the ratio $Z_f / Z_1 = k$ a real constant, then the closed loop gain is $-k$. and the input voltage is multiplied by a factor $-k$ and the scaled o/p is available at the output. usually in such applications Z_f and Z_1 are selected as precision resistors for adding obtaining precise and scaled value of input voltage.

Phase Shift circuits:-

The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain.

This circuit's are also called constant-delay filter (or) All pass filters.

Two types

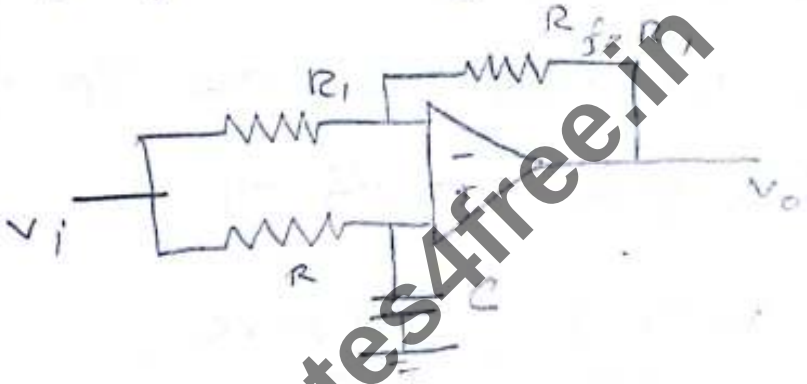
lagging phase angle

leading phase angle.

Phase lag Circuit.

The phase-lag circuit constructed using an op-amp connected in both inverting & Non-inverting mode.

To analyze the circuit operation it is assumed that the I/P Vge v_i drives a simple inverting amplifier.



The relationship b/w O/P and I/P can be expressed by

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \left(\frac{1-j\omega RC}{1+j\omega RC}\right)$$

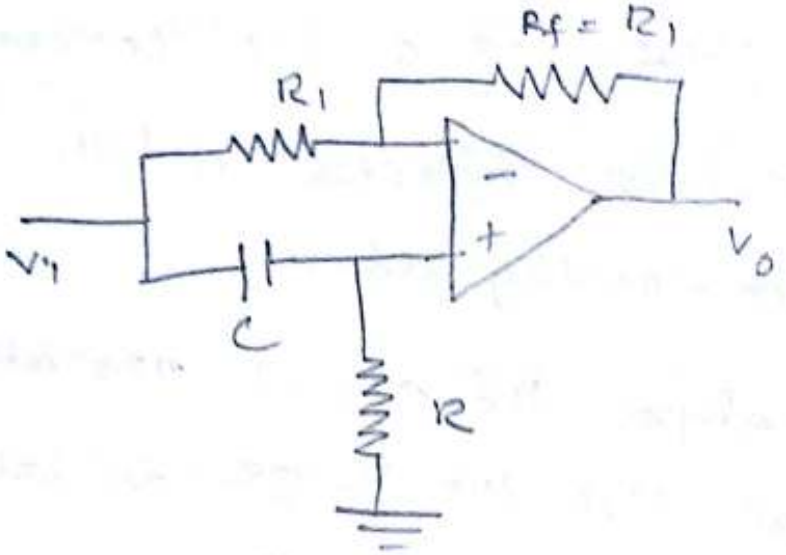
The phase angle is then given by

$$\theta = -\tan^{-1}(\omega RC) - \tan^{-1}(\omega RC)$$

$$= -2\tan^{-1}(\omega RC)$$

$$\boxed{\theta = -2\tan^{-1} f/f_0}$$

Phase lead circuit:



Phase lead ckt which the RC ckt forms a high pass N/w. the O/p vge is derived and expressed by

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1+j\omega RC}{1+j\omega RC}$$

It is to be noted that the numeral has a -ive real part & overall phase is given by.

$$\theta = 180^\circ - \tan^{-1}(\omega RC) - \tan^{-1}(\omega RC)$$

$$= 180^\circ - 2\tan^{-1}(\omega RC)$$

$$\boxed{\theta = 180^\circ - 2\tan^{-1}(f/f_o)}$$

Voltage follower :-

If $R_i \to \infty$ and $R_f = 0$ in the non inverting amplifier configuration, than the amplifier acts as a unity gain amplifier (or) voltage follower.

(ie)

$$A_v = 1 + \frac{R_f}{R_1} \quad (\text{or}) \quad \frac{R_f}{R_1} = A_v - 1$$

Since $\frac{R_f}{R_1} = 0$. ($\because A_v = 1$).

The circuit consists of an op-amp and a wire connecting the o/p vge to the i/p.

(ie) The o/p vge is equal to the input vge both in magnitude & phase.

($V_o = V_i$)

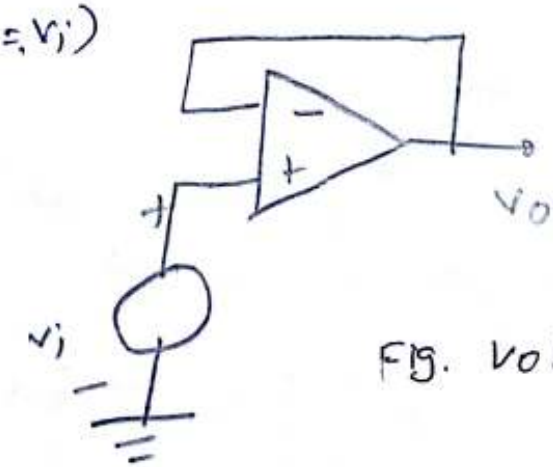


Fig. Voltage follower.

since the output voltage of this circuit follows the input voltage, the circuit is called voltage follow

It offer very high input impedence of the order of MΩ & very low output impedence. Therefore this circuit draws negligible current from the source.

Thus the voltage follower can be used as a buffer b/w a high impedenc source and a low impedence load for impedance matching application

Voltage to current converter:-

One may have a to convert a vge sgl to a proportional o/p current. (Photo conductance amplifier).

Two types → of ckt possible

- V-I converter with floating load.
- V-I converted with grounded load.

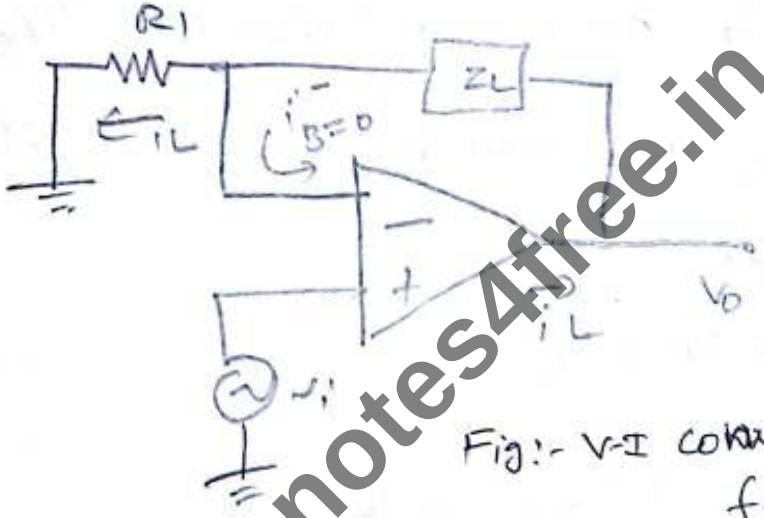


Fig:- V-I converter with floating load.

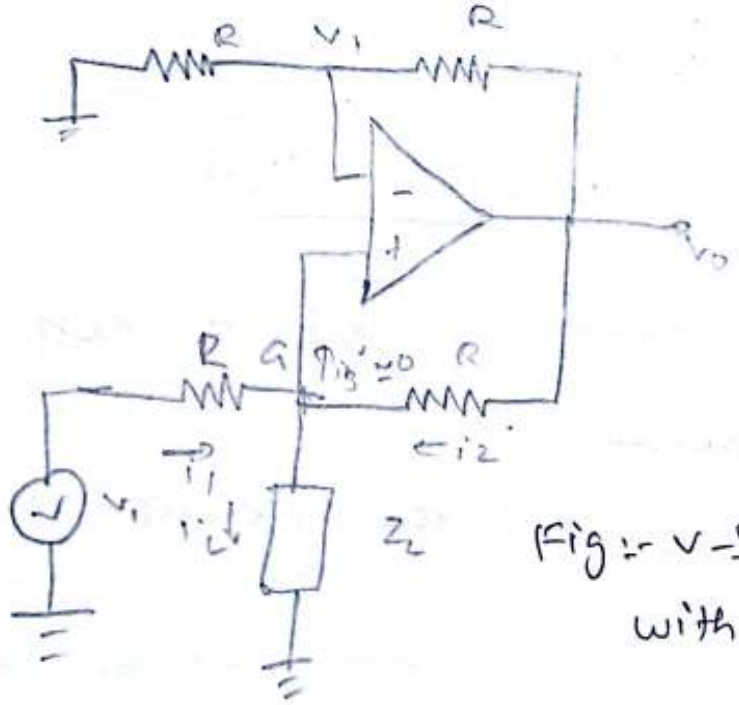


Fig:- V-I converter with grounded load.

practical circuit fig shows a V/I to current converter in which load Z_L is floating.

V/I node a is V_1

$$V_i = i_L R_1 \quad (I_B = 0)$$

$$i_L = \frac{V_i}{R_1}$$

That is the input voltage V_i is converted into an output current of V_i/R_1

Let V_1 be the voltage node 'a' writing KVL, we get.

$$i_1 + i_2 = i_L$$

$$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = i_L$$

$$V_i + V_o - 2V_1 = i_L R$$

$$V_1 = \frac{V_i + V_o - i_L R}{2}$$

The op-amp is used in non inverting mode

The gain of the circuit is $1 + R/R$

$= 2$.

O/p voltage is

$$v_o = 2v_i = v_i + v_o - i_L R$$

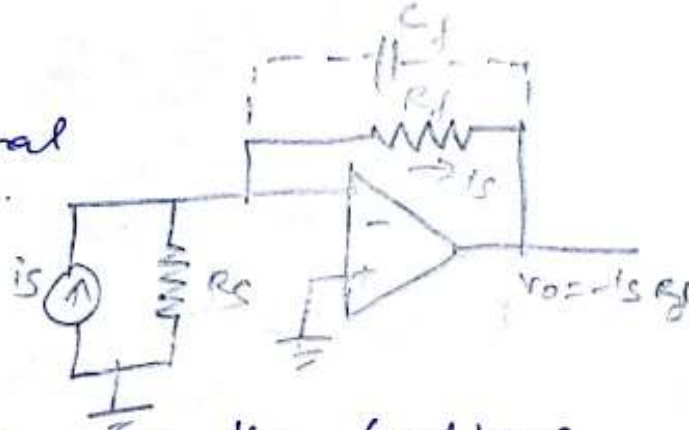
$$v_i = i_L R$$

$$\boxed{i_L = \frac{v_i}{R}}$$

current to voltage converter.

photocell, photodiode & photo voltaic cell give an o/p current that is proportional to an incident radiant energy or light.

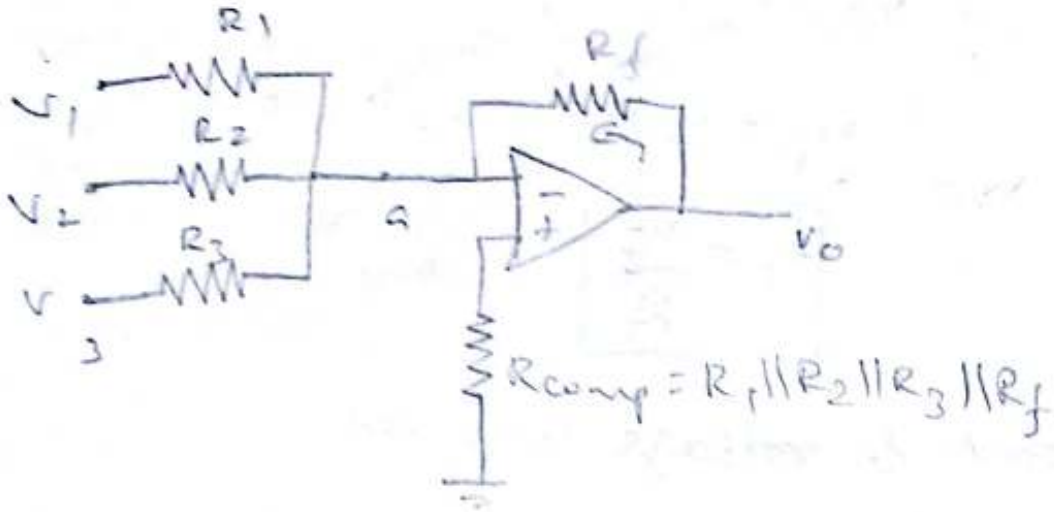
The current through these devices can be converted to voltage by using a I-V converter & thereby the amount of light or radient energy incident on the photo-device can be measured.



-ive i/p terminal is at virtual gnd No current flows through R_s and current i_s flows through the feedback resistor R_f. Thus the o/p vge $v_o = 0 - i_s R_f$.

It may be pointed out that the lowest current that this circuit can measure will depend upon the bias current I_B of the operational amplifier

Adder:-



· The following analysis is carried out assuming that the op-amp is an ideal one

$A_{OL} = \infty$ and $R_i = \infty$

input bias current is zero (assumed)

V_{ge} at node a is zero. Nodal equation by KCL at node 'a' is

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

$R_1 = R_2 = R_3 = R_f$

$$V_o = -(V_1 + V_2 + V_3)$$

$R_1 = R_2 = R_3 = 3R_f$

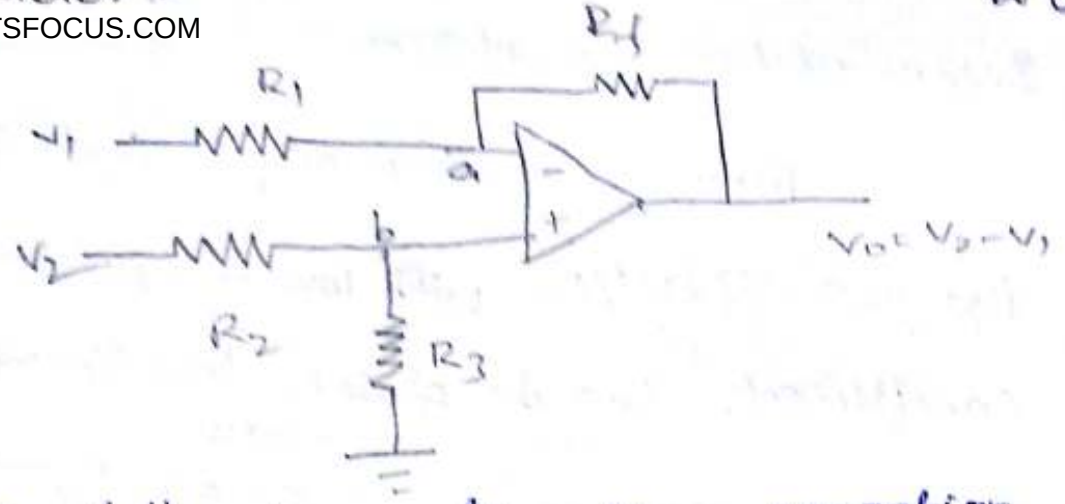
$$V_o = -\left(\frac{V_1 + V_2 + V_3}{3}\right)$$

To find R_{comp} make all i/ps $V_1 = V_2 = V_3 = 0$

So the effective i/p resistance $R_i = R_1 || R_2 || R_3$

Therefore $R_{comp} = R_i || R_f = R_1 || R_2 || R_3 || R_f$

Subtractor:-



The following analyze the operation of the circuit assume that all resistors are of equal value R

(ie) $R_1 = R_2 = R_3 = R_f = R$.

output voltage is given by

$$V_{o1} = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) = V_1$$

III^ly the o/p V_{o2} due to V_2 alone (with V_1 grded) can be written simply for an inverting amplifier as

$$V_{o2} = -V_2$$

Thus the o/p voltage V_o due to both the inputs can be written as

$$V_o = V_{o1} + V_{o2}$$

$$\boxed{V_o = V_1 - V_2}$$

Instrumentation amplifier.

High gain accuracy, High CMRR, High gain stability with low temperature co-efficient, low dc offset, low o/p impedance

The o/p voltage v_o is given by

$$v_o = -\frac{R_2}{R_1} v_2 + \frac{1}{1+(R_3/R_4)} v_1 \left(1+\frac{R_2}{R_1}\right)$$

Therefore

$$v_o = -\frac{R_2}{R_1}\left(v_2 - \frac{(1+R_4/R_2)}{1+(R_3/R_4)} v_1\right)$$

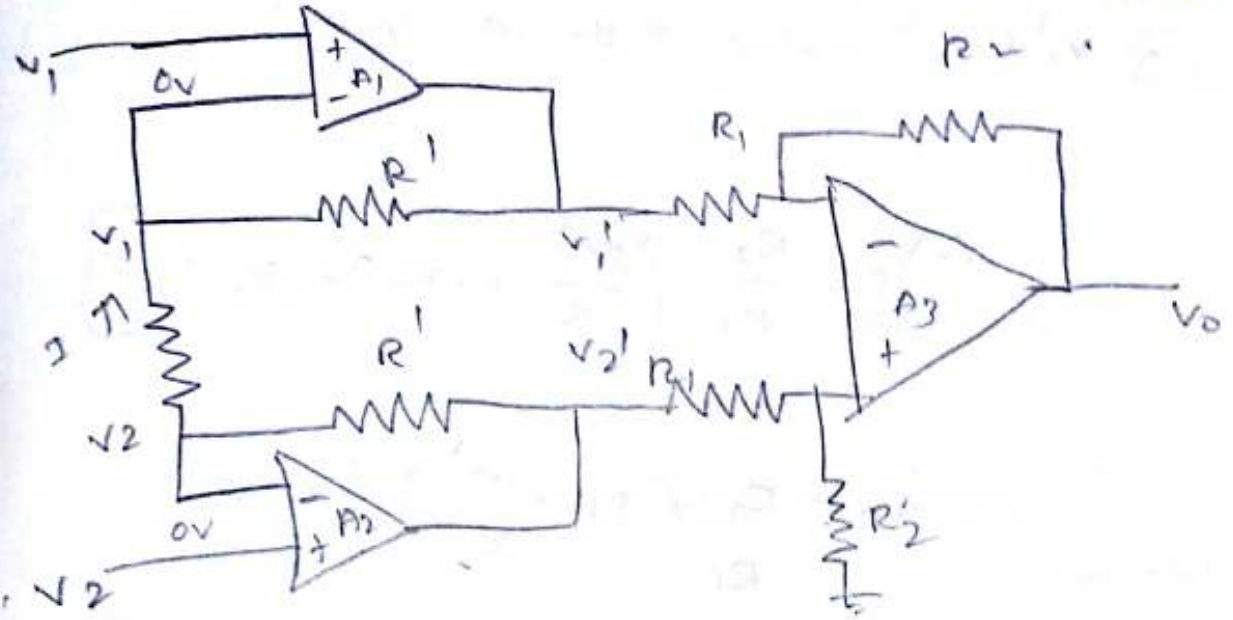
If $\frac{R_1}{R_2} = \frac{R_3}{R_4}$ then $v_o = \frac{R_2}{R_1}(v_1 - v_2)$

(ie) the o/p voltage v_o is difference of the two input voltage with the voltage at the non-inverting terminal of Op-amp A_3 is

$$\frac{R_2 v_1'}{R_1+R_2}$$

By using superposition theorem

$$v_o = -\frac{R_2}{R_1} v_1' + \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_2 v_2'}{R_1+R_2}\right)$$



$$V_o = \frac{R_2}{R_1}(V_1' - V_2')$$

Since there is no current entering the op-amp the current $I = \frac{V_1 - V_2}{R}$, which flows through the resistor R'.

$$V_1' = -R' I + V_1$$

$$V_1' = \frac{R'}{R}(V_1 - V_2) + V_1$$

$$V_2' = -R' I + V_2$$

$$V_2' = -\frac{R'}{R}(V_1 - V_2 + V_2$$

V_1 & V_2 value sub in $V_0 = \frac{R_2}{R_1}(V_1' - V_2')$

$$\therefore V_0 = \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right]$$

$$V_0 = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)(V_1 - V_2).$$

The bridge initially balanced by a d.c supply vge V_{dc} so that $(V_1 = V_2)$

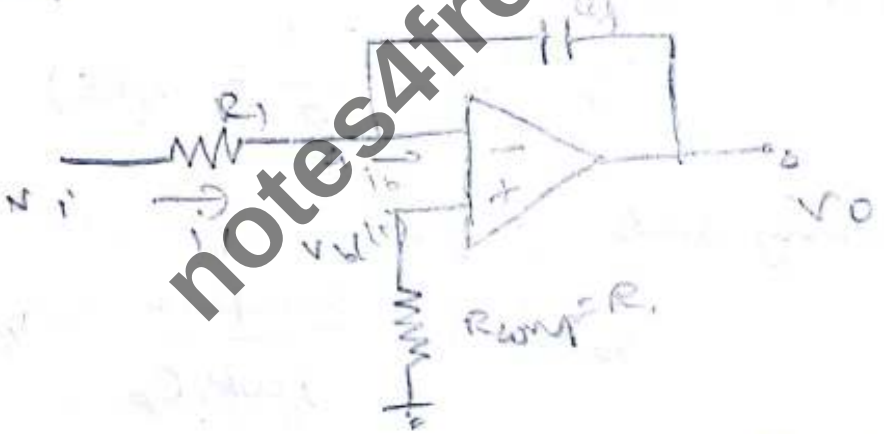
AS the physical quantity Changes the resistance R_T of the transducer also changes causing an unbalance in the bridge $(V_1 \neq V_2)$

Application → temperature indicator
→ temperature controller
→ light intensity meter.

Integrator :-

A circuit in which the o/p voltage waveform is the time Integral of the input voltage waveform is called integrator.

Integrator produces a summing action over a required time interval & the circuit is based on the general parallel - inverting voltage feedback model.



The Nodal eqn at node "a" is given by

$$\frac{V_i}{R_1} + C_F \frac{dV_o}{dt} = 0$$

$$\frac{dV_o}{dt} = -\frac{1}{R_1 C_F} V_i$$

Sing on both sides.

$$\int_0^t dv_o = -\frac{1}{R_1 C_F} \int_0^t v_i \, dt$$

$$V_o(t) = -\frac{1}{R_1 C_F}\int_0^t v_i(t)\,dt + v_o(0)$$

Where $v_o(0)$ is the initial o/p voltage

A resistance $R_{comp} = R_1$ is usually connected to the (+) input terminal to minimize the effect of i/p bias curre

The operation of the integrator can al be studied in the frequency domain In phasor notation

$$V_o(s) = -\frac{1}{sR_1C_F}V_i(s)$$

Steady state $s = j\omega$

$$V_o(j\omega) = -\frac{1}{j\omega R_1 C_F}V_i(j\omega)$$

The magnitude of the gain (or) integrator transfer function

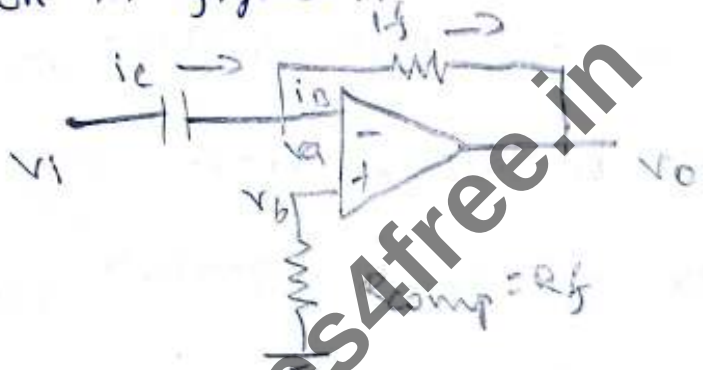
$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|-\frac{1}{j\omega R_1 C_F}\right|$$

$$\boxed{|A| = \frac{1}{\omega R_1 C_F}}$$

Differentiator:-

The differentiator can perform the mathematical operation of diffrentiation (ie) the output voltage is the diferentiation of the i/p vge.

The ideal differentiator may be constructed from a basic inverting amplifier shown in figure.



The expression for the output voltage can be obtained from KCL

$$i_c = I_B + i_f$$

Since $I_B = 0$

$$i_c = i_f$$

$$C_1 \cdot \frac{d}{dt}(V_i - V_a) = \frac{V_a - V_o}{R_f}$$

But $V_a = V_b$ since A is very large

Therefore

$$C_1 \cdot \frac{dv_i}{dt} = -\frac{V_o}{R_f}$$

(or)

$$V_o = -R_f C_1 \frac{dV_i}{dt}$$

Thus the output V_o is equal to the $R_f C_1$ times the -ve instantaneous rate of change of the input voltage V_i with time. A differentiator performs the reverse of the integrator's function.

The upper cut-off frequency is given by

$$f_a = \frac{1}{2\pi R_f C_1}$$

At $f = f_a$, $|A| = 1$ (or) 0dB and the gain increases at a rate of +20 dB/dec

Thus at high frequency, a differentiator may become unstable & break into oscillation

Log amplifier:-

log amplifier a grounded base transistor is placed in the feedback circuit.

Since the collector is held at virtual ground and the base is also grnded. the transistor v_{ge} - i_c relationship become that of a diode and is given by

$$I_E = I_S(e^{qV_E/kT} - 1)$$

$I_C = I_E$

$$I_C = I_S(e^{qV_E/kT} - 1)$$

$$\frac{I_C}{I_S} = (e^{qV_E/kT} - 1)$$

$$e^{qV_E/kT} = \frac{I_C}{I_S} + 1 = \frac{I_C}{I_S}$$

$(\text{as } I_S = 10^{-13}\text{A},\ I_C >> I_S]$

The base to emitter voltage of transistors Q_1 and Q_2 can be written as

$$V_{Q_1\,B-E} = \frac{kT}{q} \ln\left(\frac{V_0}{R_1 I_S}\right)$$

$$V_{Q_2(B-E)} = \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

since the base of Q_1 is tied to gnd

we get $V_A = -V_{Q1\ B-E}$

$$= -\frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right)$$

The base voltage V_B of Q_2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i$$

The voltage at the emitter of Q_2 is

$$V_{Q2\ B-E} + V_B + V_{Q2\ E-B}$$

(or)

$$V_{Q2\ B-E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

But the emitter voltage of Q_2 is V_A,

thats is $V_A = V_{Q2\ B-E}$

$$-\frac{kT}{q} \ln \frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln \frac{V_{ref}}{R_1 I_s}$$

Take log on both side

$$V_E = \frac{kT}{q} \ln\left(I_C / I_s\right)$$

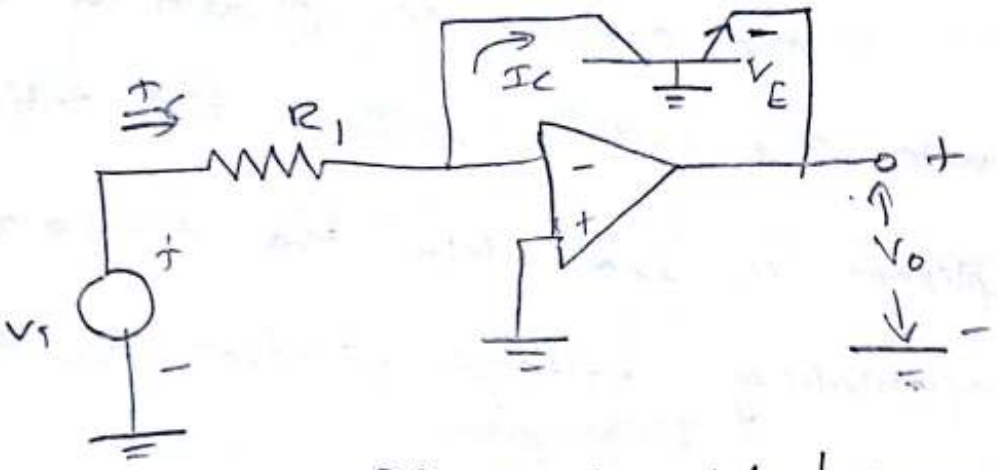


Fig. Fundamental log-amp circuit.

$$I_C = \frac{V_i}{R_1}$$

$$V_E = -V_o$$

So $$V_o = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$$

$$= -\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

where $V_{ref} = R_1 I_S$.

The output voltage is thus proportional to the logarithm of input voltage.

antilog amplifier :-

The circuit is shown in the figure. The input V_i for the antilog amplifier is fed into the temperature compensating voltage divider R_2 and R_{TC}

$$V_{Q_1\,B-E} = \frac{KT}{q} \ln\left(\frac{V_o}{R_1 I_S}\right)$$

$$V_{Q_2\,B-E} = \frac{KT}{q} \ln\left(\frac{V_o}{R_1 I_S}\right)$$

The base of Q_1 is tied to gnd

$$V_A = V_{Q_1\,B-E} = -\frac{KT}{q} \ln\left(\frac{V_o}{R_1 I_S}\right)$$

The base voltage V_B of Q_2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i$$

The voltage at the emitter of Q_2 is

$$V_{Q_2\,B-E} = V_B + V_{Q_2\,E-B}$$

$$V_{Q_2\,B-E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{KT}{q} \ln\left(\frac{V_{ref}}{R_1}\right.$$

But the emitter voltage of Q_2 is V_A

$$V_A = V_{Q_2\,B-E}$$

$$-\frac{KT}{q} \ln\frac{V_o}{R_1 I_S} = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{KT}{q} \ln\frac{V_{ref}}{}$$

$$\frac{R_{TC}}{R_2+R_{TC}} v_i = -\frac{kT}{q}\left(\ln\frac{V_o}{R_1 I_S} - \ln\frac{V_{ref}}{R_1 I_S}\right).$$

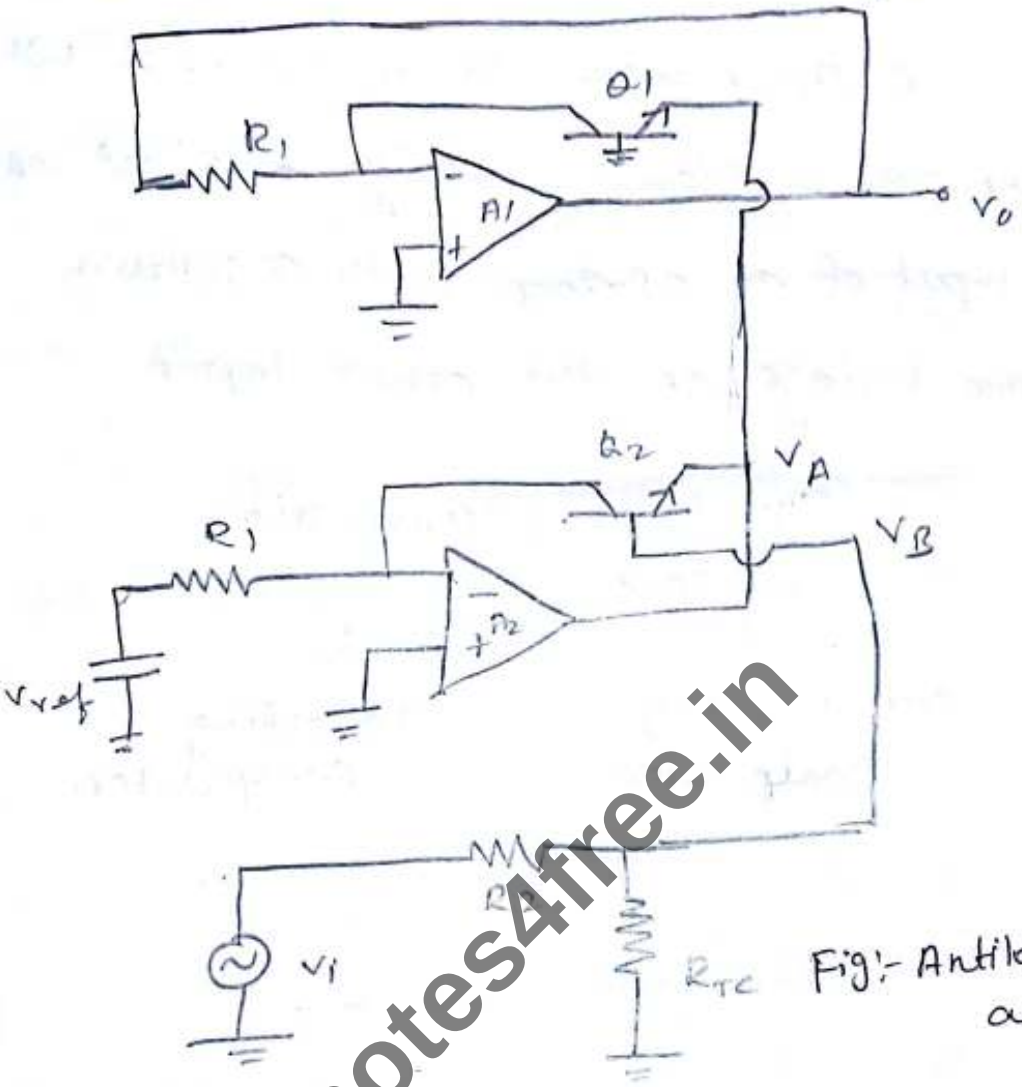


Fig:- Antilog amplifier.

$$-\frac{q}{kT}\frac{R_{TC}}{R_2+R_{TC}} v_i = \ln\left(\frac{V_o}{V_{ref}}\right)$$

log on both sides.

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2+R_{TC}}\right) v_i = 0.4343 \times \ln\left(\frac{V_o}{V_{ref}}\right)$$

$$-k' v_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

$$\frac{V_o}{V_{ref}} = 10^{-k' v_i}$$

$$\boxed{V_o = V_{ref}\left(10^{-k' v_i}\right)}$$

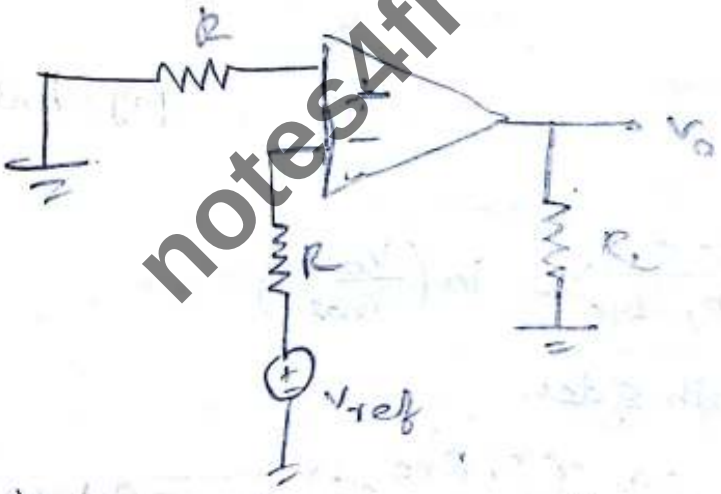
$$\boxed{k' = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2+R_{TC}}\right)}$$

Comparator:-

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input

Two types of comparator

- Non-inverting Comparator.
- Inverting Comparator.



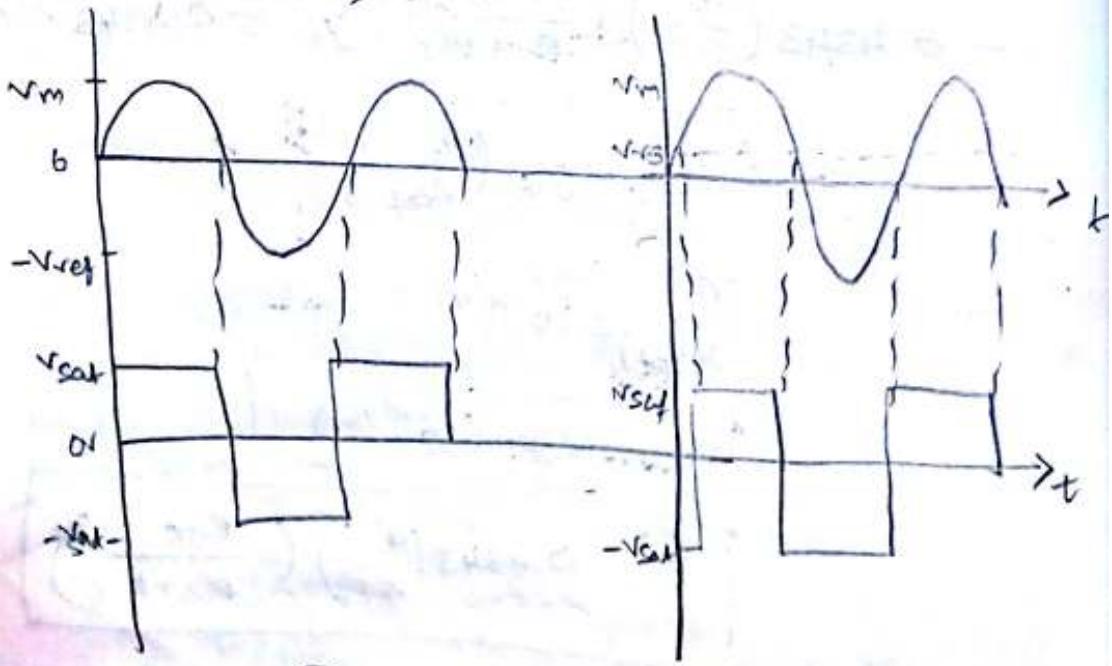


Fig. Non-inverting Comparator

A fixed Reference voltage V_{ref} is applied to -ive input & a time varying sig(v_i is applied +ive input.

The o/p voltage is at $-V_{sat}$ for $v_i < V_{ref}$ and v_o goes to $+V_{sat}$ for $v_i > V_{ref}$.

Inverting comparator in which the reference voltage V_{ref} is applied to the +input and v_i is applied to -ive input.

output voltage levels independent of Power supply voltages can also be obtained by using a resistor R and two back to back zener diodes at the output of op-amp.

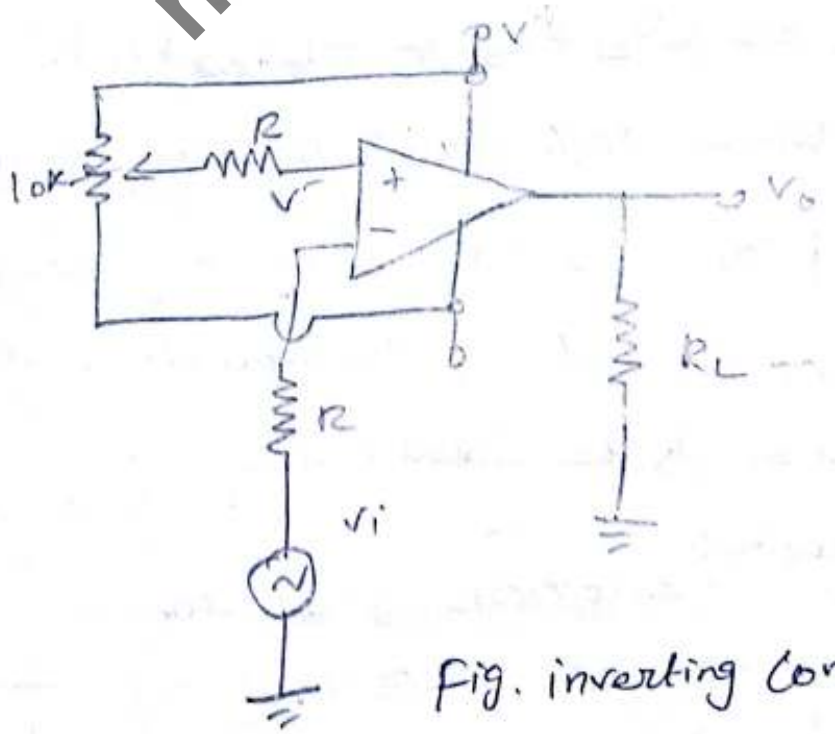


Fig. inverting Comparator.

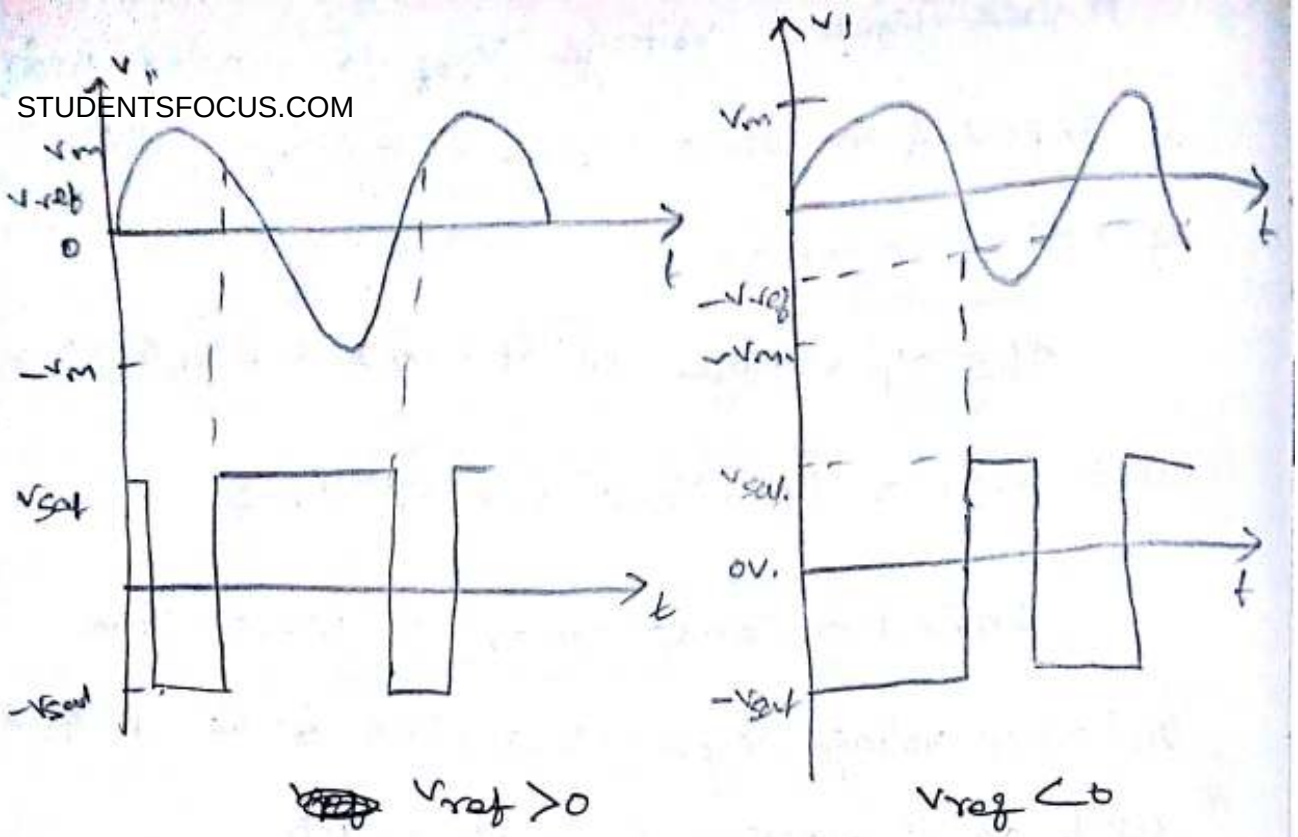


Fig :- Inverting comparator output waveform.

The value of resistance R is chosen so that the zener diodes operate at the recommended current. It can be seen that the limiting voltages of v_o are $(V_{Z1} + V_D$ & $-(V_{Z2} + V_D)$.

Where V_D (≈0.7V) is diod Forward voltage.

If 741 the internally compensated OP-amp is used as comparator, the primary limitation is the Slew rate.

Application :

- → zero crossing detector.
- → window detector.
- → Time marker generator
- → phase meter.

Schmitt Trigger:-

If +ive feedback is added to the comparator circuit, gain can be fed greatly, the transfer curve of comparator becomes more close to ideal curve. If the loop gain $-\beta A_{OL}$ is adjusted to unity. This also gives an o/p waveform virtually discontinuous at the comparison vge. This circuit, however now exhibits a phenomenon called hysteresis.

The circuit is also known as Schmitt Trigger. The input vge is supplied to the -ive input terminal and f/b vge to the +ive i/p terminal. The o/p $V_o = +V_{sat}$ The voltage (+) input terminal can be obtained by using superposition.

$$V_{UT} = \frac{V_{ref} R_1}{R_1 + R_2} + \frac{R_2 V_{sat}}{R_1 + R_2}$$

V_{UT} - upper threshold vge.

$$V_{LT} = \frac{V_{ref} R_1}{R_1 + R_2} - \frac{R_2 V_{sat}}{R_1 + R_2}$$

V_{LT} - lower threshold vge.

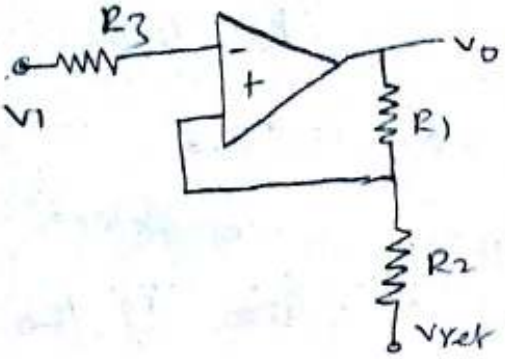


Fig. inverting Schmitt trigger

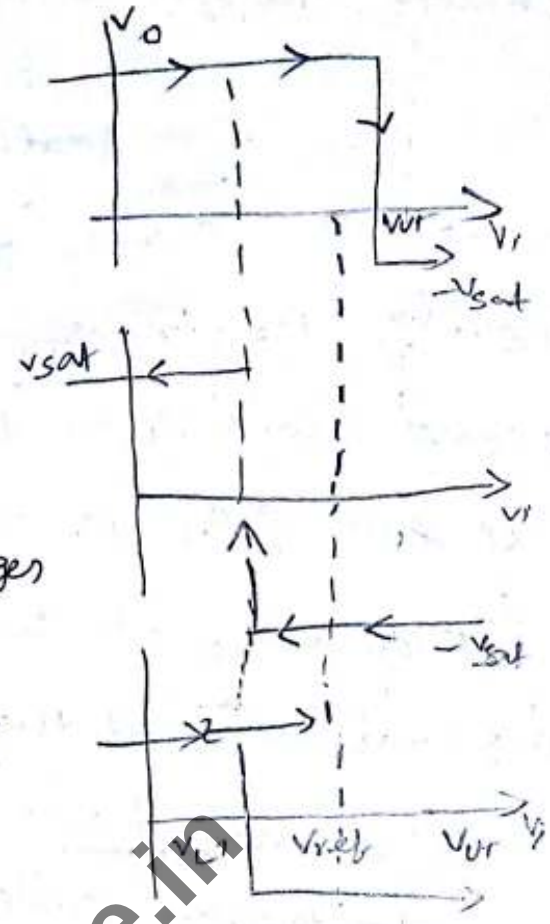


Fig. Transfer characteristics.

$V_{LT} < V_{UT}$ and the difference b/w these two voltage is the hysteresis width V_H and can be written as

$$V_H = V_{UT} - V_{LT} = \frac{2R_2 V_{sat}}{R_1 + R_2}$$

Because of the hysteresis, the circuit triggers at a higher Vge for increasing signal then for decreasing one. Further note that if peak to peak input sgl V_i were smaller than the V_H then the Schmitt trigger circuit.

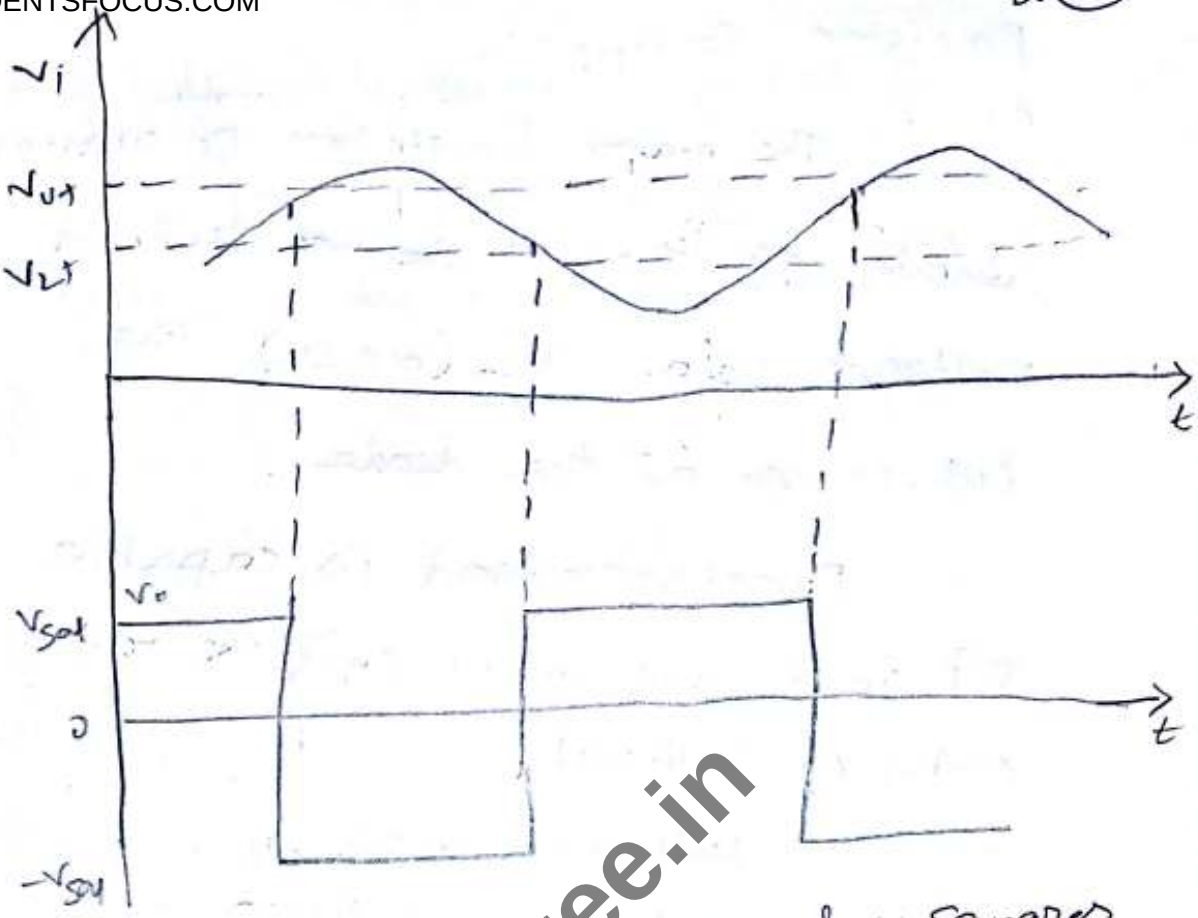


Fig:- Schmitt trigger used as Squares.

The hysteresis width V_H is independent of V_{ref}. The resistor R_3 in the figure is chosen equation to $R_1 \| R_2$ to compensate for the input bias current. A non-inverting Schmitt trigger obtained if V_i and V_{ref} are interchanged. The most important application of Schmitt trigger circuit is to convert a very slowly varying input vge into a square wave output

$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$

Precision Rectifier :-

The major limitation of ordinary diode is that it cannot rectify voltages below V_γ (or 0.6V), the cut-in voltage of the diode.

Precision diod is capable of rectifying input sgls of the order of millivolt.

Half wave rectifier.

Full wave rectifier.

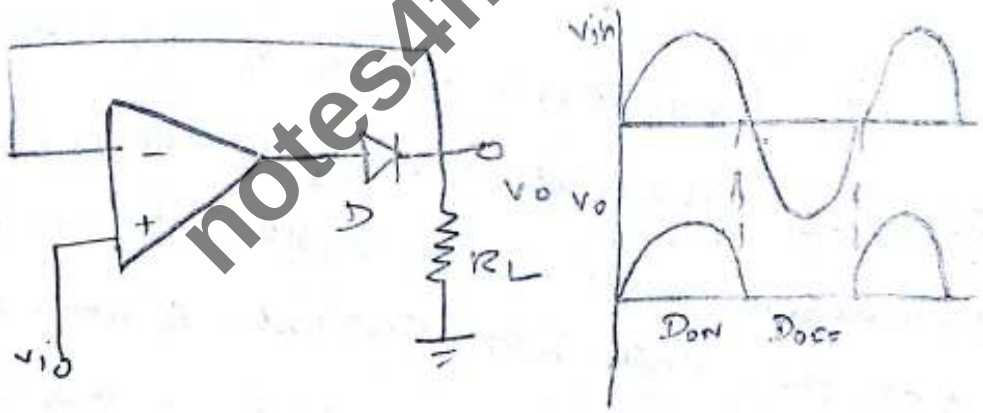
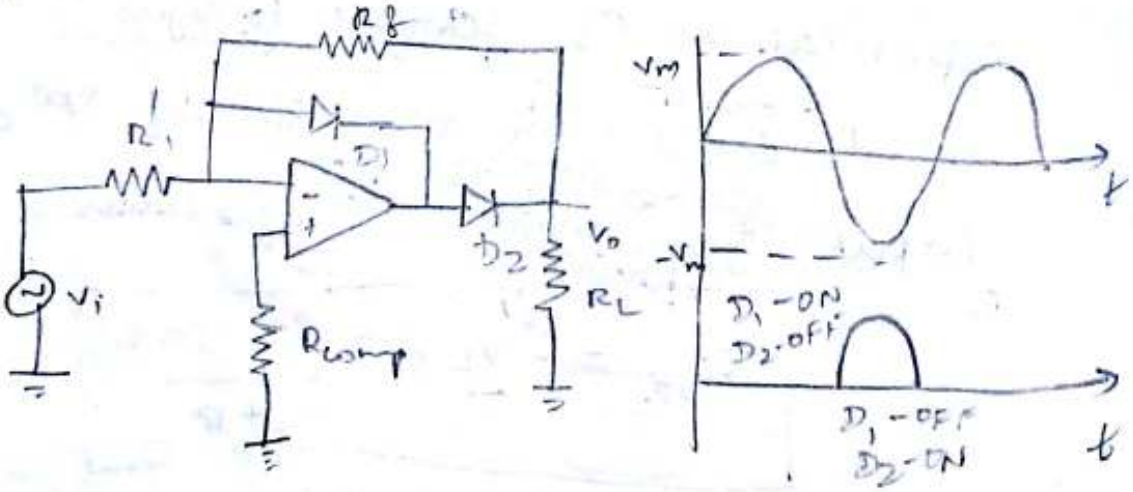


Fig:- Precision Rectifier i/p & o/p waveforms

Half wave rectifier :-

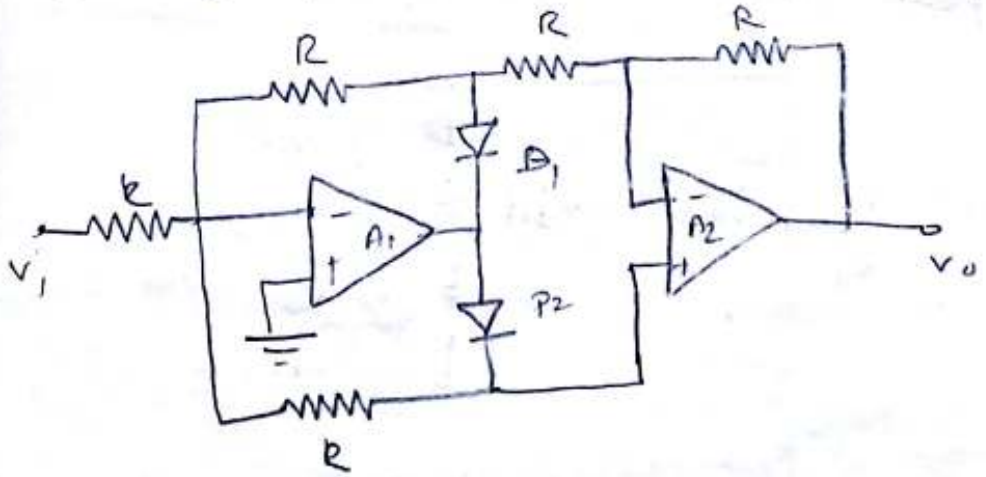


An inverting amplifier can be converted into an ideal half-wave rectifier by adding two diodes. when v_i is +ive. diode D_1 conduct causing V_{OA} to go to -ive by one diode drop (≈0.6V). Hence diode D_2 is reverse biased. The output voltage V_o is zero. because for all practical purpose no current flows through R_f and input current flows through D_1.

Full wave rectifier:-

A full-wave rectifier or absolute value circuit shown in figure

$V_i > 0$, diode D_1 is on and D_2 is off. Both the op-amp A_1 and A_2 act as inverting as shown in equivalent circuit. It can $V_o = V_i$



For -ive input (ii) $V_i \geq 0$

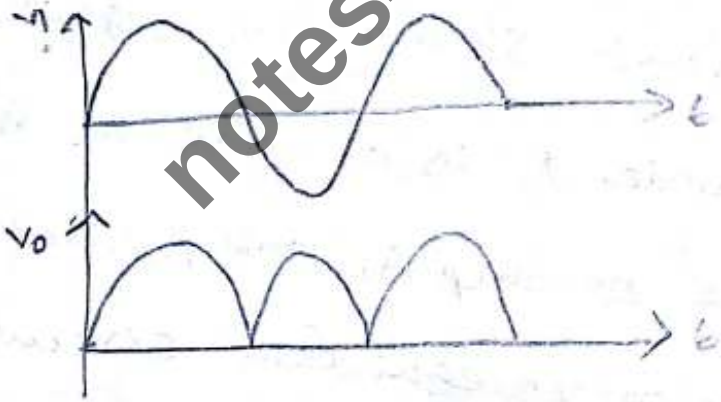
off and D_2 is on. The equivalent circuit is shown in figure. Let the output voltage of op-amp A_1 be V. Since the differential input to A_2 KCL at node 'a' gives

$$\frac{V_i}{R} + \frac{V}{2R} + \frac{V}{R} = 0$$

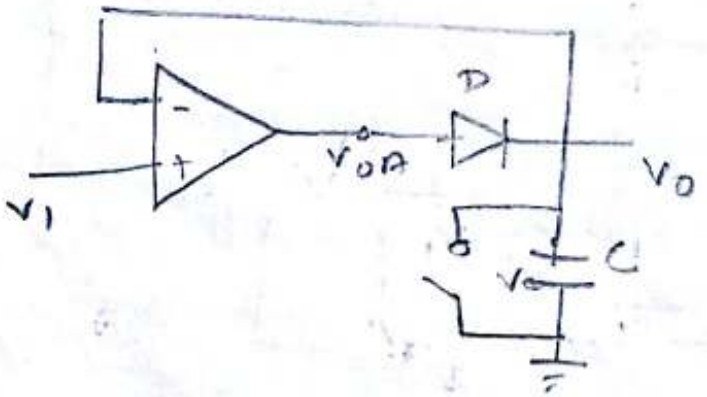
$$\boxed{V = -\frac{2}{3} V_i}$$

The output v_o is

$$v_o = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3} V_i\right) = -V_i$$



Peak detector:-



The function of a peak detector is to compute the peak value of the input. The circuit follows the voltage peaks of a signal & stores the highest value on a capacitor.

If a higher peak signal value comes along this new value is stored. The highest peak value is stored until the capacitor is discharged.

The circuit can be reset - that is capacitor vge can be made zero by connecting a low leakage MOSFET switch across the capacitor.

The circuit can be modified to hold the lowest or most negative vge of a signal by reversing the diode. Peak detectors find application in test & measurement instrumentation as well as Amplitud modulation

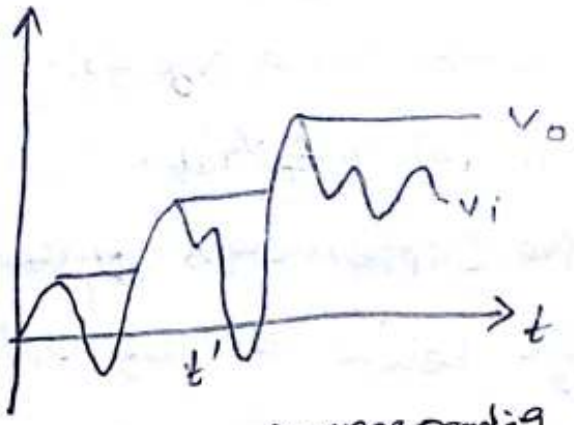
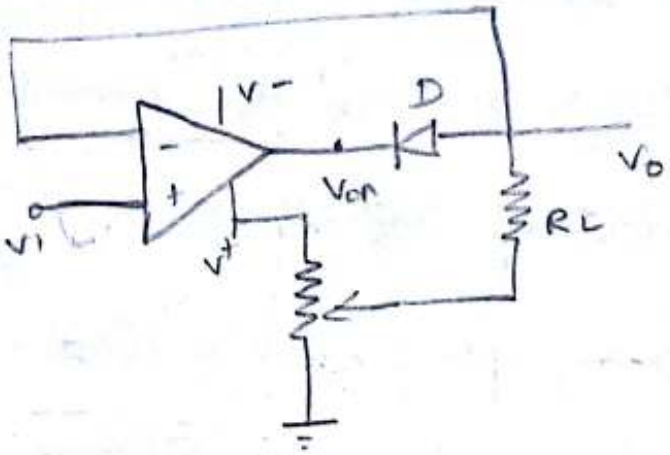
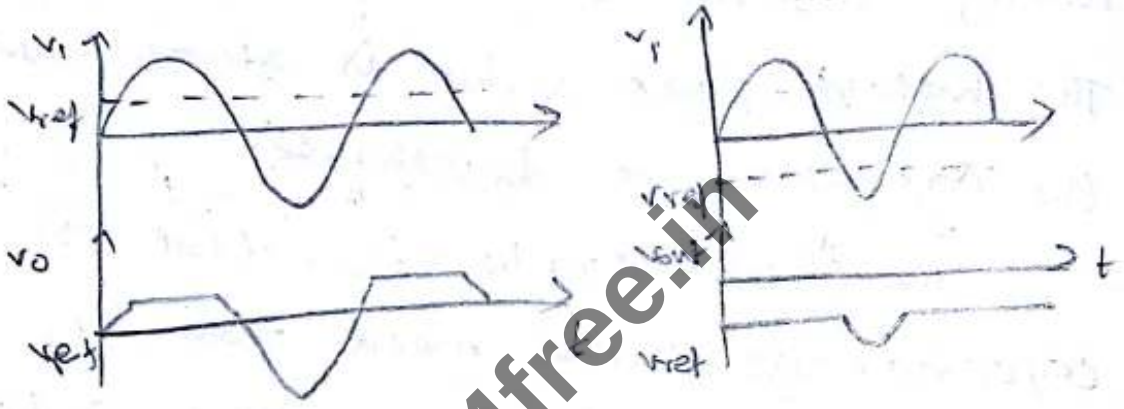


Fig. output V_o corresponding to arbitrary input V_i

Clipper:-





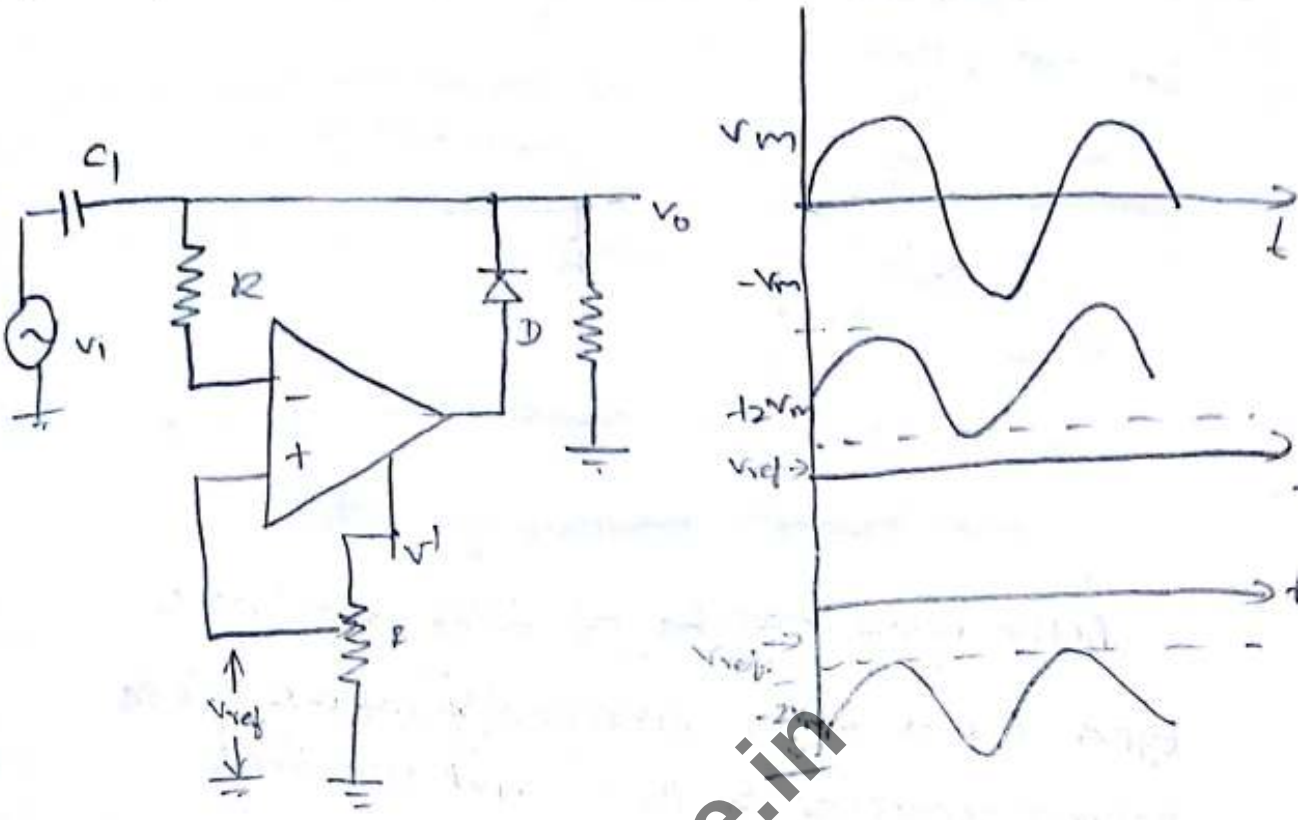
A precision diode may also be used to clip-off a certain portion of the input signal to obtain a desired o/p waveform

The clipping level is determined by the reference voltage V_{ref} and could be obtained from the fixed supply vge V^+. The o/p vge for $V_o > V_{ref}$ are clipped off.

$V_i < V_{ref}$ i/p vge diode D conducts. The op-amp works as a vge follower & o/p V_o follows i/p V_i till $V_i \leq V_{ref}$.

The -ive Clipper clips off the -ive parts of the i/p sgl below the ref voltage.

Clamper:



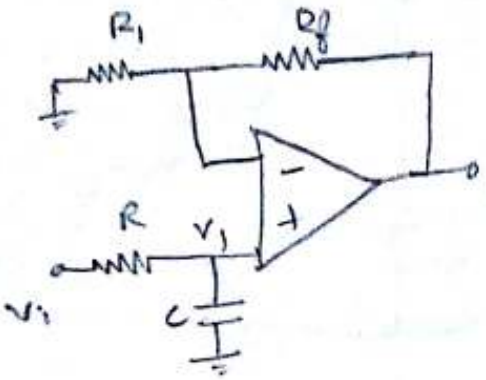
The clamper is also known as dc inserter or Restorer. The circuit is used to add a desired dc level to the o/p vge. If the clamped dc level is +ive it is called +ive clamper. If the clamped dc level is -ive the clamper is Negative clamper.

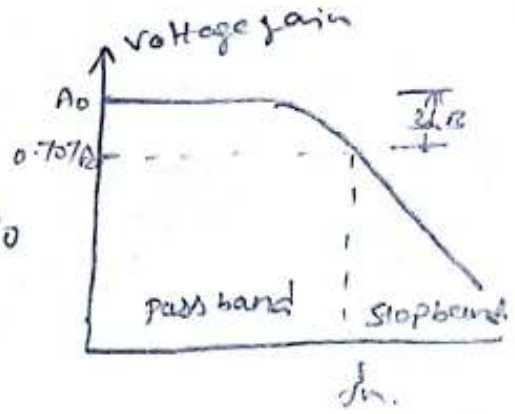
The AC i/p sgl $v_i = V_m \sin \omega t$ applied at the -ive i/p terminal. During the -ive half cycle of v_i diode D conducts. The capacitor C, charges through did D to the -ive peak vge V_m.

The Resistor R is used for protecting the op-amp against excessive discharge currents from capacitor especially when the dc supply voltages are switched off.

Low pass - High pass - Band pass filter.

Low pass filter:-





Active filters may be of different orders & types. A first order filter consists of a single RC network connected to the (+) input terminal of a non-inverting op-amp amplifier.

The voltage V_1 across the capacitor 'C' in the S-domain is

$$V_1(S) = \frac{\frac{1}{SC}}{R+\frac{1}{SC}} V_i(S)$$

$$\frac{V_1(S)}{V_i(S)} = \frac{1}{RCS+1}$$

The closed loop gain A_0 of the op-amp

$$A_0 = \frac{V_0(S)}{V_1(S)} = \left(1+\frac{R_F}{R_i}\right)$$

$$H(S) = \frac{V_0(S)}{V_i(S)} = \frac{V_0(S)}{V_1(S)} \cdot \frac{V_1(S)}{V_f(S)}$$

$$= \frac{A_0}{RCS+1}$$

$$\boxed{\omega_h = \frac{1}{RC}}$$

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_0}{\frac{s}{\omega_h} + 1} = \frac{A_0 \omega_h}{s + \omega_h}$$

$$|H(j\omega)| = \frac{A_0}{1 + j\omega RC} = \frac{A}{1 + j(f/f_h)}$$

put $s = j\omega$

$$f_h = \frac{1}{2\pi RC} \quad \& \quad f = \frac{\omega}{2\pi}$$

At very low frequency $f << f_h$

$$|H(j\omega)| = A_0$$

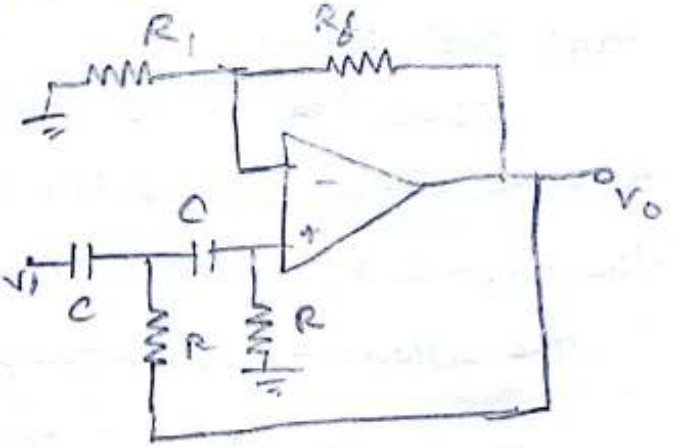
$f = f_h \Rightarrow |H(j\omega)| = \frac{A_0}{\sqrt{2}} = 0.707 A_0$.

At very high frequency $f >> f_h$

$$|H(j\omega)| << A_0 = 0.$$

High pass Active filter:

High pass filter is the complement of the low pass filter & can be obtained simply by interchanging R & C. in the low pass configuration



$Y_1 = Y_2 = sC$

$Y_3 = Y_4 = G = \frac{1}{R}$

Transfer function $H(s) = \frac{A_0 s^2}{s^2 + (3 - A_0)\omega_l s + \omega_l^2}$

$\omega_L = \frac{1}{RC}$

$$H(s) = \frac{A_0}{1 + \frac{\omega_L}{s}(3 - A_0) + \left(\frac{\omega_L}{s}\right)^2}$$

for $\omega = 0$ we get $H = 0$ & $\omega = \infty$

$$f_L = f_{3dB} = \frac{1}{2\pi RC}.$$

Putting $s = j\omega$. $3 - A_0 = \alpha = 1.414$.

$$|H(j\omega)| = \left|\frac{V_0}{V_i}\right| = \frac{A_0}{\sqrt{1 + (f_L/f)^4}}$$

$$\left|\frac{H(j\omega)}{A_0}\right| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^4}}$$

As in the case of low pass filter, the generalized expression for n^{th} order maximally flat Butterworth ($\alpha = 1.414$)

$$\left|\frac{H(j\omega)}{A_0}\right| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^{2n}}}$$

Band pass filter.

Classified in to Narrow band ($Q > 10$) & wide band pass filter ($Q < 10$) as per the figure of merit (or) Quality factor

The following Relationship

$$Q = f_0/BW = f_0/f_h - f_L$$

$$f_0 = \sqrt{f_h f_L}$$

f_h – upper cut off frequency
f_L – lower cut off frequency.
f_0 – central frequency

P. Balaji

3.1

unit-III

Analog multiplier & PLL

Analog multiplier using Emitter coupled transistor pair:-

* A basic multiplier schematic symbol shown in figure. Two signals inputs (V_x & V_y) are provided.

* The output is the product of the two i/p's divided by a reference voltage V_{ref}.

* Thus o/p voltage is scaled version of x & y inputs.

The o/p voltage is given by

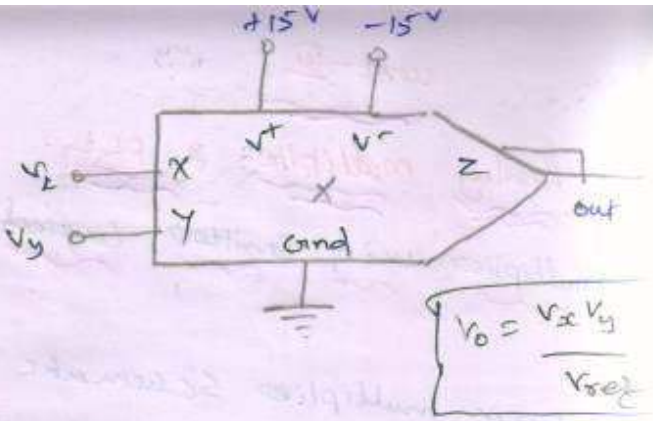
$$V_o = \frac{V_x V_y}{V_{ref}}$$

Sub $V_{ref} = 10$ volts.

$$\therefore V_o = \frac{V_x V_y}{10}$$

As long as

$$V_x < V_{ref}$$



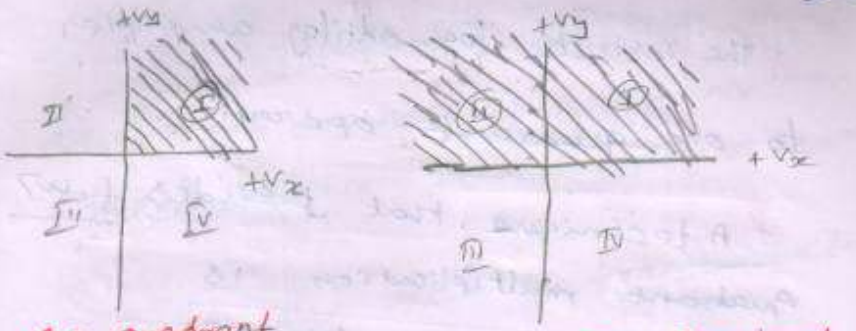
* The output of the multiplier will saturate, power supply voltage can from ±8V to ±18V.

* multipliers are designed for the sa of power supplies as used for op namely ±15V

* If both inputs are positive, it to be a one quadrant multiplier two quadrant multiplier will function if one i/p is held positive, and the other is allowed to swing both +ive

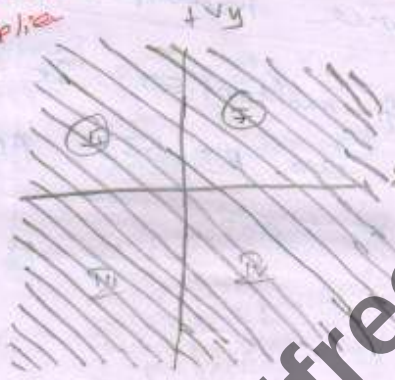
* The Ic is called a four quadrant multiplier.

3.3



One quadrant multiplier

Two quadrant multiplier



Four quadrant multiplier.

* One commonly used techniques used for log and anti log method.

* The log & Antilog relies on the mathematical relationship that the sum of the logarithm of two numbers equals the logarithm of the product of those numbers

$$\ln V_x + \ln V_y = \ln (V_x V_y)$$

* Log amplifiers require the input and reference voltages to be of the

* The restricts log-antilog amplifier to one quadrant operation.

* A technique that provides for quadrant multiplication is transconductance multipliers.

* Some of multiplier Ic chips available are AD 533, AD 534, AD633.

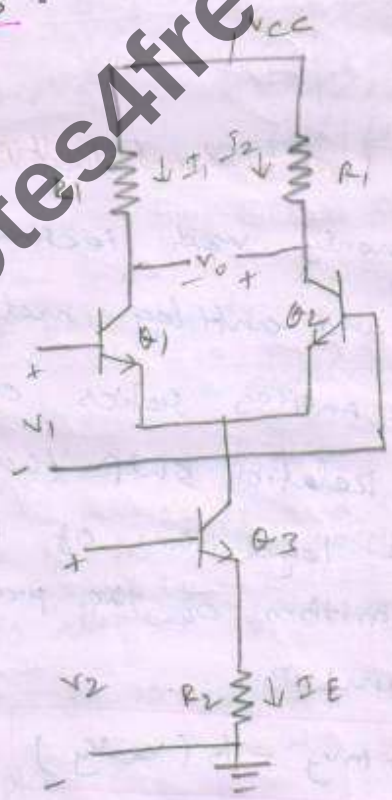


fig:- Analog multiplier using emitter

*It can be easily constructed using a load connected differential amplifier. it produces an output depends of the transistor transconductance or the emitter current-bias.

*It is also known as transconductance multiplier.

$$V_o = g_m V_1 R_1$$

* Transconductance of transistor g_m is directly proportional to the emitter current and Inversely proportional to the thermal voltage V_T.

$$g_m = \frac{I_E}{V_T}$$

Then input voltage $V_2 = I_E R_2$ (when $R_2 I_E >> V_{EE}$)

The output can be expressed as

$$V_o = g_m V_1 R_1$$

$$= \frac{I_E}{V_T} V_1 R_1$$

$$= \frac{R_1}{R_2 V_T} V_1 V_2$$

$$V_o = k V_1 V_2$$

where k is a scale factor of multiplier.

Gilbert multiplier cell

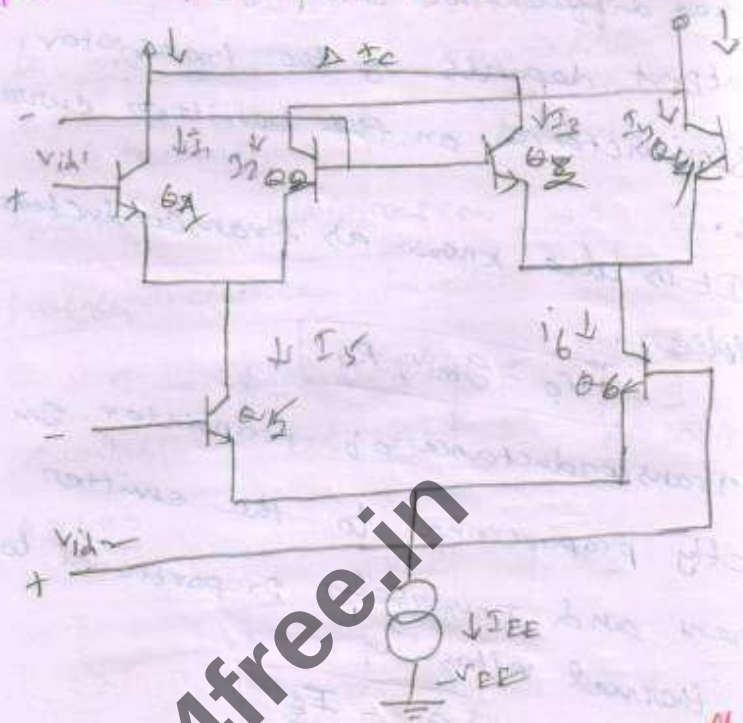


Fig:- Gilbert multiplier cell.

The bias current I_{EE} is emitter bias current for Q_1 & Q_2. The current ΔI_c is related to the two i/p voltages V_{id_1} & V_{id_2}. This cell is used to obtain complete Gilbert cell multiplier circuit.

The two inputs are V_1 & V_2. The two i/p determine the division of the total current I_E among the various branches of the circuit.

The devices are symmetrically cross coupled & the current I_E is constant, the large common mode shift at the output gets eliminated.

$$I_1 + I_2 = I_5 \quad \rightarrow (1)$$

$$I_3 + I_4 = I_6 \quad \rightarrow (2)$$

$$I_5 + I_6 = I_E \quad \rightarrow (3)$$

Assume $|V_1| << V_1$, the current unbalance in the differential pairs can be expressed as

$$I_1 - I_2 = (g_m)_{12} V_1 \quad \rightarrow (4)$$

$$I_3 - I_4 = (g_m)_{34} V_1 \quad \rightarrow (5)$$

Where $(g_m)_{12}$ – Variable transconductance of the transistor pairs $(Q_1 - Q_2)$

$(g_m)_{34}$ – Variable transconductance of the transistor pairs $(Q_3 - Q_4)$

$$(g_m)_{12} = \frac{I_5}{V_T} \quad \rightarrow (6)$$

$$(g_m)_{34} = \frac{I_6}{V_T} \quad \rightarrow (7)$$

The total differential o/p voltage V_o

$$V_o = R_L[(I_1 - I_2) - (I_3 - I_4)]$$

Sub eqn (4) & (5) in (8)

$$V_o = R_L[(g_m)_{12} v_1 - (g_m)_{34} v_1]$$

$$= R_L v_1 \left[(g_m)_{12} - (g_m)_{34}\right]$$

$$= R_L v_1 \left[\frac{I_5}{V_T} - \frac{I_6}{V_T}\right]$$

$$V_o = \frac{R_L v_1}{V_T}[I_5 - I_6] \quad \rightarrow (9)$$

If the emitter series resistance R_E is choosen sufficiently high

$$R_E I_5 >> V_T.$$

$$R_E I_6 >> V_T$$

then $(I_5 - I_6) = \frac{V_2}{R_E}$ $\rightarrow (10)$

Sub (10) in (9)

$$V_o = \frac{R_L v_1}{V_T}\left(\frac{V_2}{R_E}\right)$$

3.9

$$V_0 = \frac{R_L}{R_E} \frac{V_1 V_2}{V_T}$$

$$\boxed{V_0 = K V_1 V_2}$$

where $K = \frac{R_L}{R_E V_T}$ Scale factor

Thus the output is proportional to the product of the two input voltage.

Advantage :-

* All the transistors are well matched
* The h_{fe} for the transistor is very high. (i.e) $h_{fe} >> 1$.

Limitation :-

* The input V_1 should be small $|V_1| \ll V_T$ hence the input V_1 cannot be more than several mV.
* Thus the circuit functions as a balanced modulator and can be used in a linear multiplier.

variable Transconductance technique:-

The Symmetrical differential amplifier is the main part of the variable transconductance technique

It uses the principle of the dep Of the transistor transconductance the emitter current bias.

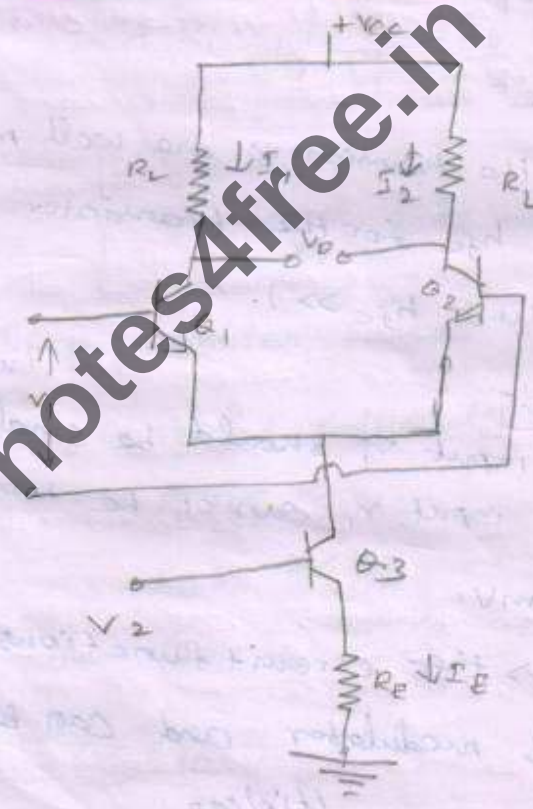


Fig:- One quadrant variable transconductance multiplier

3.11

Differential amplifier is formed by transistor Q_1 & Q_2 for very small values of differential i/p voltage V_1, $V_1 << V_T$

under this condition

$$V_0 = g_m R_L V_1$$

g_m - Transconductance.

$g_m = I_E / V_T$ the transconductance g_m depends on emitter current I_E which can be controlled by applying second voltage V_2 to the transistor Q_3

If $I_E R_E >> V_{BE}$ then

$$V_2 = I_E R_E$$

The overall voltage transfer expression can be written as

$$V_0 = \frac{I_E}{V_T} R_L V_1$$

$$V_0 = \left(\frac{V_2}{R_E V_T}\right) R_L V_1$$

$$V_o = \left(\frac{R_L}{R_E V_T}\right) \cdot V_1 V_2$$

$$V_o = k V_1 V_2$$

where $k = \frac{R_L}{R_E V_T}$ Scale factor.

Thus the o/p is proportional to the product of the two i/p vges.

limitation:-

* The Scale factor k is temperature dependent.
* The total current I_E varies as a function of voltage V_2
* The large common mode voltage swing in the circuit which is highly objectionable. If a single ended o/p (or) d.c coupling is required.

3.13

Analog multiplier Ic's & their applications:-

i) AD 533 as multiplier:-

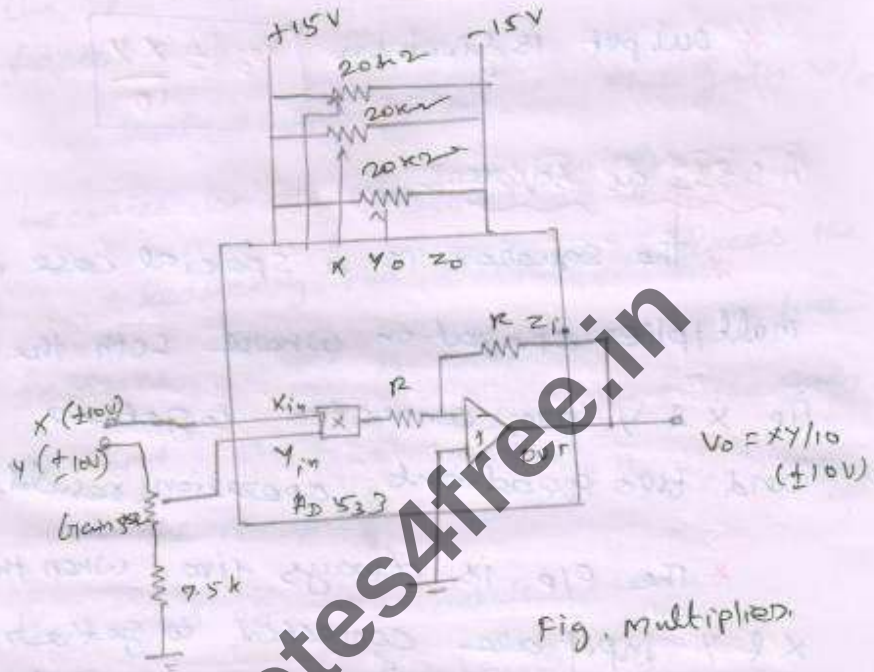


Fig. Multiplier

* The multiplier operation is possible by closing the loop around the internal op-amp with the Z input connected to the output

* The X_0 null pot balanced the X i/p Channel to minimize Y feed through and the Y_0 null pot balances the Y input to minimize X feedthrough.

* The Zo Pot compensates the o/p op-amp offset voltage. The gain pot set the full scale o/p level.

* Output is given by $V_o = \frac{XY}{10}$

AD533 as squrer:-

* The squarer is a special case multiplier operation where both the i/p X & Y are connected together and two quadrant operation result.

* The o/p is always +ive, when X & Y input are connected together then combained offset which is algebraic sum of the individual offsets result.

* This can be nulled using the X_o pot alone. The o/p is given as

$$V_o = \frac{XY}{10} = \frac{X^2}{10}$$

3.15

AD533 as Divider:-

* The divide mode utilises the multiplier in a feed back configuration where the Y input controls the feedback factor.
* With x full scale, the gain Vo/z becomes unity after trimming.
* Reducing the x input reduces the feedback around the op-amp by a like amount, thereby increasing the gain.
* The reciprocal relationship forms the basis of the divide mode.
* The output is given by

$$V_o = \frac{10z}{x}$$

AD 533 as Square Rooter:-

* AD 533 mode is also a feedback Configuration. Both x and y inputs are tied to the op-amp output through an external diode to prevent latch up.

*Accuracy, noise and the frequency response are proportional to the which implies a wider usable dynamic range than the divide mode.

AD 534 as Divider:

* AD 534 provides the differential operation on both numerator & denominator. This allows the ratio of two floating variables to be generated.

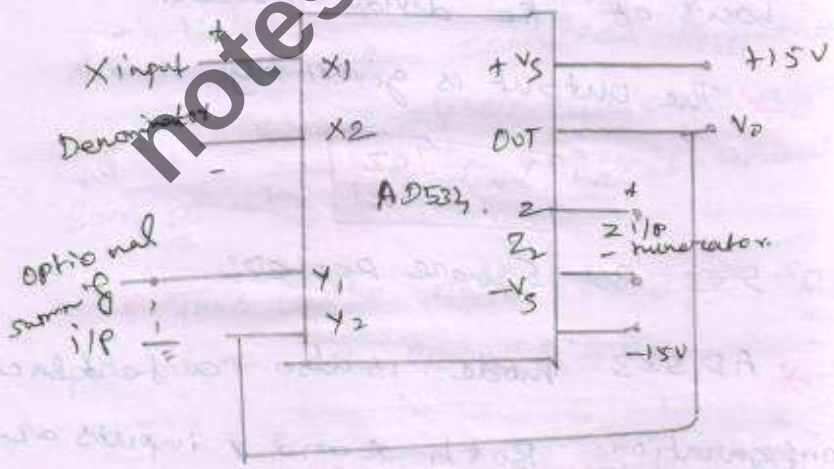


Fig:- Divider AD534.

*Flexibility is possible from access to high impedance summing i/p to Y_1. The ban... may...

without additional trimming, the accuracy of AD 534 is sufficient to maintain a 1% error over 1V to 10V denominator range.

* the overall gain can be introduced by inserting a simple attenuator between the output and V_2 terminal.

* The output of the AD534 as a divider circuit is

$$V_o = \frac{10(Z_2 - Z_1)}{(X_2)} + X_1$$

AD 534 as square rooter.

* The diode prevents a latching condition which could occur if the input momentarily changes the polarity the O/P is +ive.

* since the sgl i/p is differential, all the combination of i/p & O/p polarities can be realized but operation is restricted to the one quadrant associated with each combination of inputs.

* The output of the circuit is given as

$$V_o = \sqrt{10(Z_2 - Z_1) + X_2}$$

Operation of the Basic PLL

* The phase locked loop (PLL) is an important building block of linear S/m. Electronic PLL came in 1930s when it was used for radar synchronisation and combination applications.

The basic block schematic of the PLL system consists of

1. Phase detector / comparator
2. Low pass filter
3. error amplifier
4. voltage controlled oscillator

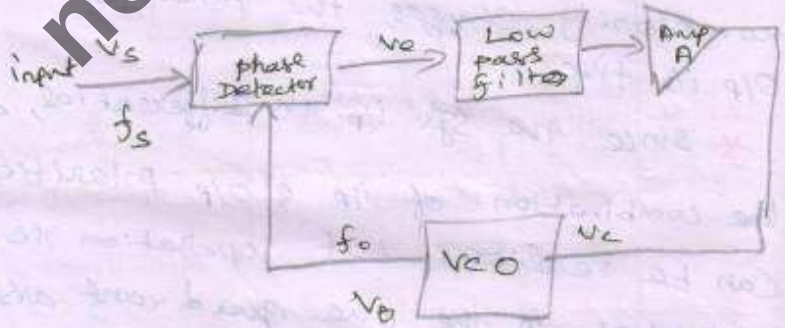


Fig:- Block schematic of the PLL

* The VCO is a free running multivibrator & operates at a set of fre fo called free running frequency

(3.19)

* f_o can be shifted to either side by applying a dc voltage V_c, the freq deviation is directly proportional to the DC ctrled voltage. it is called **Voltage Controlled Oscillator.**

* If an i/p sgl v_s of frequency f_s is applied to the PLL, the phase detector compares the phase & frequency of the incoming sgl to that of the o/p v_o of the VCO.

* The **phase detector** is basically a **multiplier** & produces the sum $f_s + f_o$ and difference $f_s - f_o$ components at its output.

* The high frequency component $f_s + f_o$ is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage V_c to VCO.

* The VCO continues to change frequency till its o/p frequency is exactly the same as the i/p sgl frequency. This circuit is said to be **Locked**.

* Once locked, PLL tracks the frequency changes of the i/p sgl. Thus a PLL goes through three stages.

i) free running
ii) Capture
iii) locked or tracking.

Important definition related to PLL:-

Lock-in Range:-

* once the PLL is locked, it can track frequency changes in the incoming sgls range of frequencies over which the PLL can maintain lock with the incoming sgl is called the Lock in Range (or) Tracking Range

Capture Range:-

* The range of frequencies over which the PLL can acquire lock with an i/p is called the capture range. This parameter is also expressed as Percentage of fo

Pull-in Time:-

* The total time taken by the to establish lock is called pull-in time

3.21

Closed loop analysis of PLL:

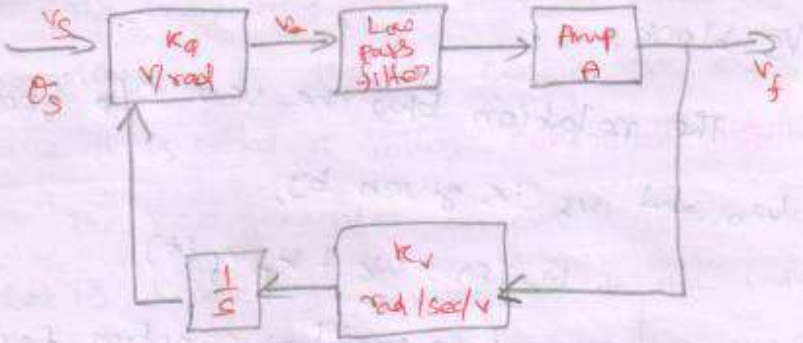


Fig. block diagram of PLL Sys.

* Under locked conditions a linear relationship can exist b/w the o/p volt of the phase detector & the phase of difference b/w the VCO & the i/p sig.

* K_ϕ - Conversion gain of phase detector in volt/rad

* F(s) - Loop filter transfer function.

* A - Gain of the amplifier.

* K_v - Vco to frequency transfer Co-efficient of VCO.

* The phase of the VCO o/p is equal to the time integral of the VCO o/p frequency

$$\omega_0(t) = \frac{d\theta_0 t}{dt}.$$

* An integration takes place within PLL. This integration is represented VS block.

* The relation b/w the VCO O/P ω_o and v_f is given by,

$$\omega_o(t) = \omega_c + k_o v_f(t)$$

* The close loop transfer function of PLL is given by

$$\frac{V_f}{\theta_s} = \frac{k_q F(s) A}{s + k_q F(s) \cdot A \cdot \frac{k_v}{s}}$$

$$\frac{V_f}{\theta_s} \cdot \frac{1}{s} = \frac{k_q F(s) A}{s + k_q F(s) A k_v}$$

$$\frac{V_f}{\omega_s} = \frac{k_q F(s) A}{s + k_q F(s) A k_v}$$

If loop-filter is not used ($\because \frac{V_f}{\omega_s}$)

$$F(s) = 1$$

$$\frac{V_f}{\omega_s} = \frac{k_q A}{s + k_q k_v A}$$

$$\frac{V_f}{\omega_s} = \left(\frac{k_L}{s + k_L}\right)\frac{1}{k_v}$$

k_L – is known as loop Bandwidth

3.23

Voltage Controlled Oscillator (VCO) - IC566

The frequency deviation is directly proportional to the dc control Vge and, hence it is called a Voltage controlled Oscillator.

The VCO generates an output frequency that is directly proportional to the input Vge

The VCO is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied Vge

The VCO provides the linear relationship b/w the applied Vge & the oscillation frequency Applied Vge is called Control voltage.

Fig. Pin Configuration of VCO

The total voltage on the capacitor

The $\Delta V = 0.25 V_{cc}$. The capacitor charges with a constant current source

$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

$$\Delta v = 0.25 V_{cc}$$

$$\frac{0.25 V_{cc}}{\Delta t} = \frac{i}{C_T}$$

$$\Rightarrow \Delta t = \frac{0.25 V_{cc} C_T}{i}$$

The time period T of the triangular waveform $= 2\Delta t$. The frequency of oscillator is

$$f_0 = \frac{1}{T} \Rightarrow f_0 = \frac{1}{2\Delta t}$$

$$f_0 = \frac{1}{2\left(\frac{0.25 V_{cc} C_T}{i}\right)}$$

$$f_0 = \frac{i}{0.5 V_{cc} C_T}$$ But $i = \frac{V_c}{R_T}$

Where V_c – is the voltage pin 5

$$f_0 = \frac{[(V_{cc} - V_c)/R_T]}{0.5 V_{cc} C_T}$$

$$f_0 = \frac{2[V_{cc} - V_c]}{}$$

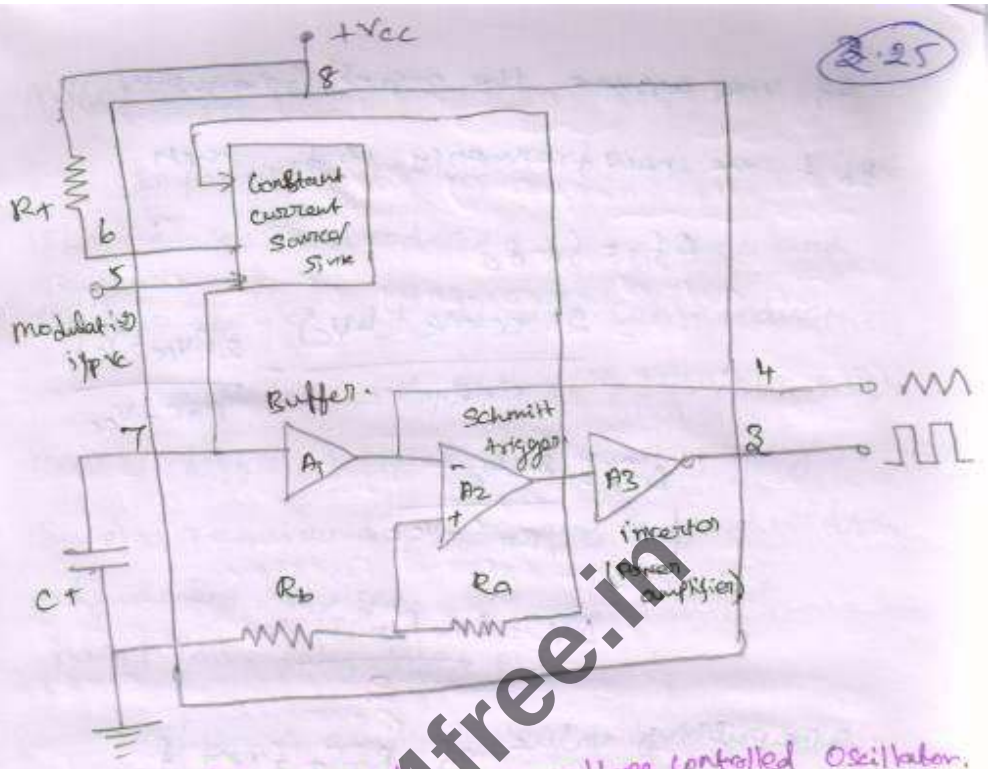


fig. Block diagram voltage controlled Oscillator.

The voltage V_c can be varied by connecting a R_1R_2 in the above circuit. The component R_T & C_T are first selected so that VCO o/p frequency lies in the centre of the operating frequency range

A parameter of importance for VCO is voltage to frequency conversion factor k_c & is defined as

$$k_v = \frac{\Delta f_0}{\Delta V_C}$$

ΔV_C – is the modulation i/p.

Δf_0 – is the produced frequency shift for a VCO.

If we assume the original frequency f_0 & the new frequency is f_1. then

$$\Delta f_1 = f_1 - f_0$$

$$= \frac{2(V_{CC} - V_C + \Delta V_C)}{C_T R_T V_{CC}} - \frac{2(V_{CC} - V_C}{R_T C_T V_{CC}}$$

$$\Delta f_0 = \frac{2\Delta V_C}{R_T C_T V_{CC}}$$

$$\Delta V_C = \Delta f_0 R_T C_T V_{CC} \quad \text{---(2)}$$

Then putting value of $R_T C_T$ from f_0

$$\Delta V_C = \frac{\Delta f_0 V_{CC}}{2(4 f_0)}$$

$$f_0 = \frac{1}{4 R_T C_T}$$

$$\Delta V_C = \frac{\Delta f_0 V_{CC}}{8 f_0}$$

$$\therefore R_T C_T = \frac{1}{4 f_0}$$

From the definition of voltage to frequency Conversion factor K_V is

$$K_V = \frac{\Delta f_0}{\Delta V_C}$$

sub the value of $\frac{\Delta f_0}{\Delta V_C}$ in the ΔV_C

$$\therefore K_V = \frac{8 f_0}{V_{CC}}$$

2.27

Monolithic PLL IC 565

Importance monolithic PLLs are SE/NE 560 series introduced by signetics and LM560 series by National Semiconductor.

The SE/NE 560, 561, 562, 564, 565 & 567 mainly differ in operating frequency range, power supply requirement, frequency & bandwidth adjustment ranges. But 565 is the most commonly used PLL.

565 is available as a 14-pin DIP package & 10-pin round can package.

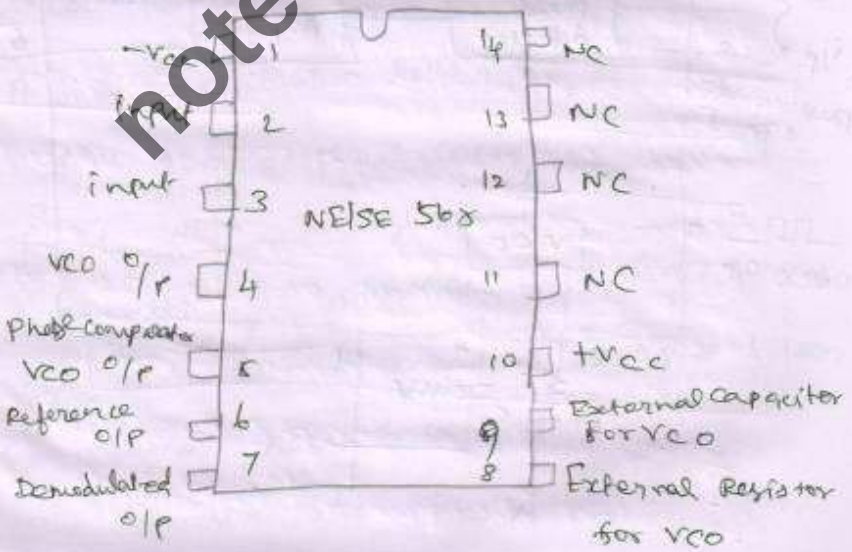


Fig. PIN diagram.

A value b/w 3kΩ & 20kΩ is recommended for R

adjusted with R_T & C_T to be at the c
of the i/p frequency Range

The output frequency of the VCO (i/p
can be written as

$$f_0 = \frac{0.25}{R_T C_T} \text{ Hz.}$$

Where R_T - external Resistor.

C_T - Capacitor connected b/w pin9 &
pin8.

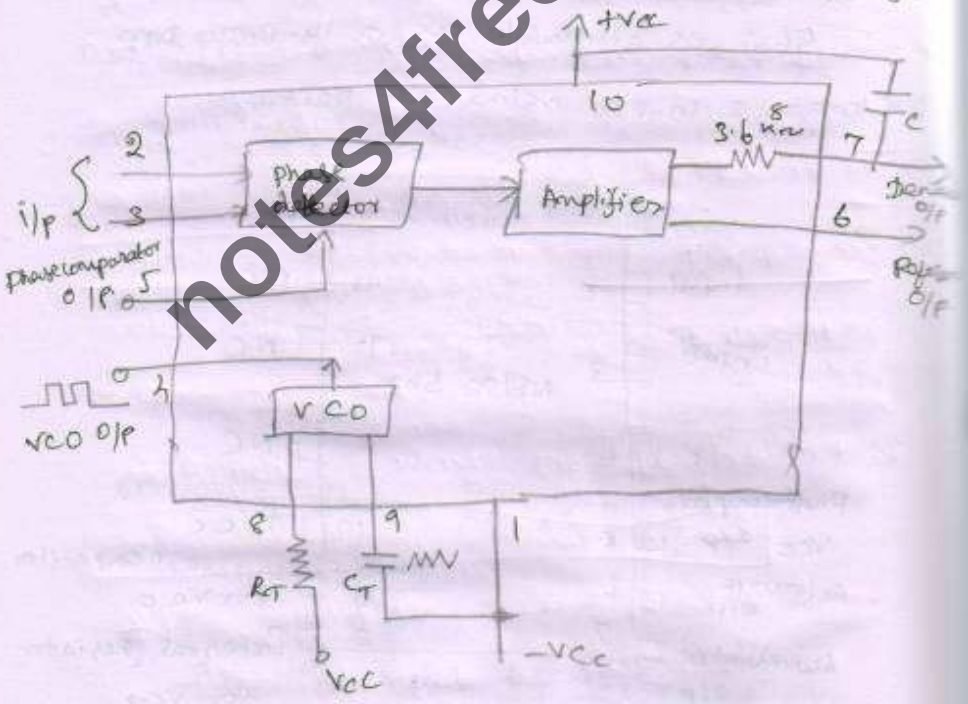


Fig :- NE/SE 565 PLL block diagram.

Important Electrical parameters of 565 PLL

1. operating frequency range - 0.001Hz to 500kHz
2. operating voltage range - ±6V to ±12V
3. input level - 10mV rms min to $3V_{pp}$ max
4. input impedance - 10 kΩ typical
5. output sink current - 1mA typical
6. triangle wave amplitude - $2kV_{pp}$ at ±6V supply vge
7. Square wave amplitude - $5.4V_{pp}$ at ±6V supply vge
8. Bandwidth adjustant range - ±1% to ±60%.

phase locked loop - internally broken b/w the VCO i/p & phase comparator o/p

A Short circuit b/w pins 4 & 5 connects the VCO output to the phase comparator & to compare f_o with i/p sgl f_o

A capacitor C is connected b/w pin 7 & pin 10 (supply terminal) to make a low pass filter with internal resistance

The conversion Ratio of the phase detector of 565 PLL as

$$k_\phi = \frac{1.4}{\pi}$$

Application of PLL

AM Detection:-

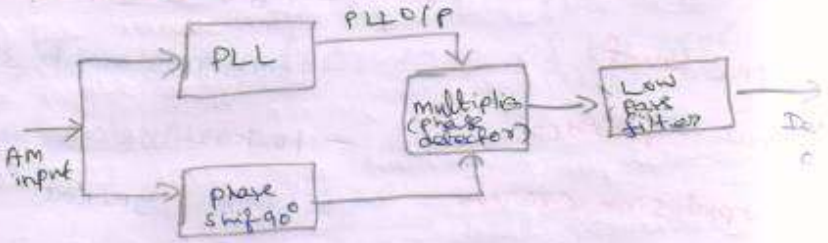


Fig. Block diagram of AM detection using PLL

* The block diagram of PLL connected AM detector is shown in figure that is used to demodulate AM signal
* AM i/p is applied to PLL it produces a carrier o/p with a same frequency locked to the carrier frequency of the in coming signal.
* A PLL always provides an output with 90° phase of an incoming signal.
* The multiplier accepts one input from the output of PLL & another i/p is connected directly from an AM i/p sgl through the 90° phase shifter.

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90° phase shifter is used to compensate the AM i/p sgl with the phase of PLL o/p.

Both the sum & difference signals are produced by a multiplier to the low pass filter.

After filtering low pass filter leaves the demodulated sgl to the o/p terminal of AM detector.

Advantage :-

A high selectivity and the noise immunity which is not supported by Conventional AM detector.

Fm detection :-

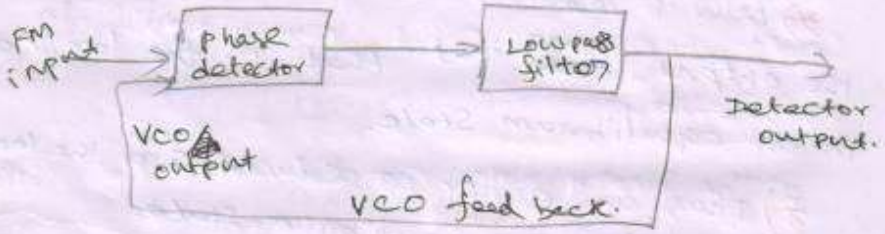


Fig :- Block diagram of FM detection using PLL.

*) FM detector is used to modulate FM signal.

*) The three major blocks of the detector are phase detector, low pass filter, and VCO

*) MOST PLLs are having phase detector and VCO on a chip and external terminals are provided to make a low pass filter.

*) An FM i/p sgl is applied as a one input to the phase detector.

*) Another input is connected with the output of VCO usually VCO provides 90° phase difference for its i/p.

*) The phase detector utilizes two i/p's with same frequency and 90° phase difference

*) Now it responds zero error voltage to the output terminal that is the loop locked in an equilibrium state.

*) Thus an error is reduced and the loop gets locked in an equilibrium state

*) However the loop error can be reduced significant level to produce a modulating sig

*) Usually the PLL connected FM detector is used in noise modulation process.

3.32

FSK modulation & Demodulation.

FSK modulation:-

*) FSK is a type of binary data transmission techniques that is widely used in radio teletype as a subcarrier tones, computer peripherals and communication fields.

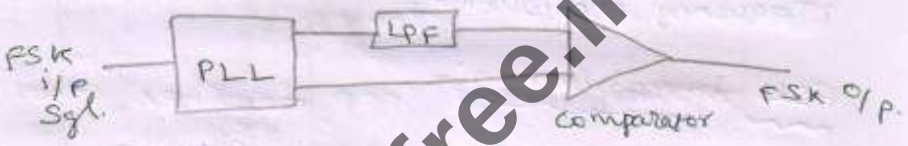


Fig:- FSK modulator.

*) In the FSK the above mentioned frequencies gives the total frequency deviation 200Hz and the center frequency of 1170Hz.

For the PLL the lock range is

$$\Delta f_L = \frac{1}{2\pi f} \frac{\Delta f_{vco}}{\Delta t}$$

where f is the break frequency of Low Pass filter.

The capture range is

$$\Delta f_{cap} = \sqrt{f \times \Delta f_L}$$

*) Normally in the FSK technique the binary data is transmitted b/w the two set of frequencies that allow retrie the binary data is receiving side usi Frequency modulation.

FSK demodulation:

*) In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequ which is shifted b/w two preset frequen

*) This type of data transmission is called frequency shift keying demodulat technique.

*) The binary data can be retrieved using a FSK demodulator at the receiving end.

*) the 565 PLL is very useful as FSK demodulator.

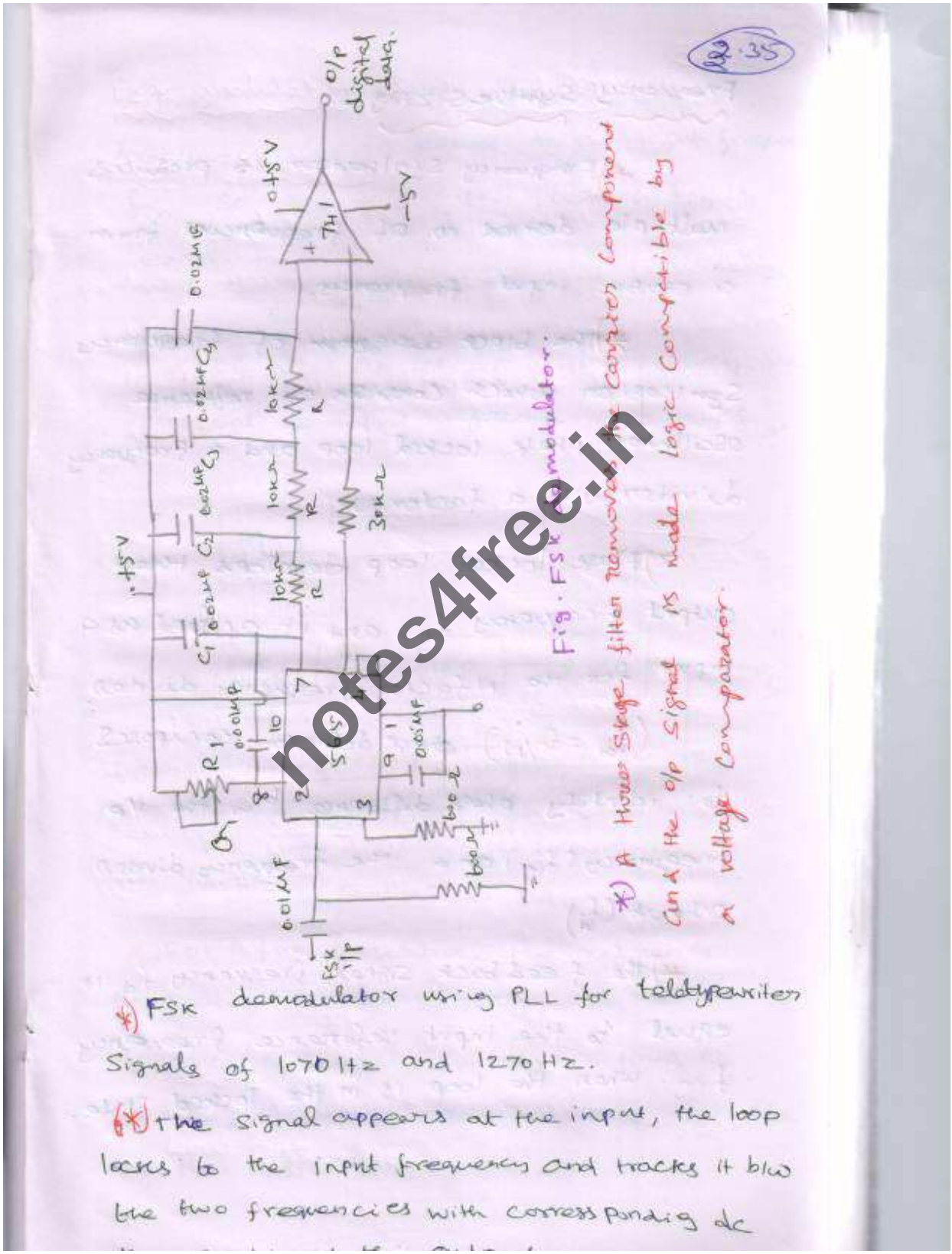


Fig. FSK demodulator.

*) A three stage filter removes the carrier component and the o/p signal is made logic compatible by a voltage comparator.

*) FSK demodulator using PLL for teletypewriter signals of 1070 Hz and 1270 Hz.

(*) the signal appears at the input, the loop locks to the input frequency and tracks it b/w the two frequencies with corresponding dc

Frequency Synthesizing:-

*) Frequency Synthesizer is produce multiple desired no. of frequencies from a stable input frequency.

*) The block diagram of frequency Synthesizer which consists of reference oscillator, phase locked loop and a frequency divider with a factor N.

*) Phase locked loop develops the output frequency f_o, and it applied as input to the N factor frequency divider ($f_d = f_o/N$). phase detector compares to identify phase difference b/w the i/p frequency (f_{in}) and the frequency divider output (f_d)

*) the feedback signal frequency f_d is equal to the input reference frequency f_{in}. when the loop is in the locked state

*) Thus the frequency divider output frequency f_d is equal to an input frequency f_{in}. So that the input frequency f_{in} is equal to f_o/N (ie) $f_o = N f_{in}$.

*) If N is an integer the frequency step is equal to input reference frequency f_{in}.

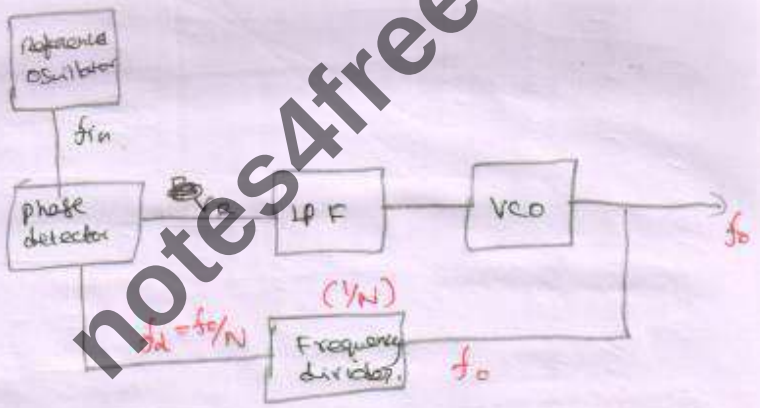


Fig. block diagram of frequency synthesizer using PLL.

*) For a fine resolution, the reference frequency should be very low.

*) Since a shorter switching time as desired, it limits the frequency resolution of this system.

4.1

UNIT - IV

ANALOG TO DIGITAL & DIGITAL TO ANALOG CONVERTERS.

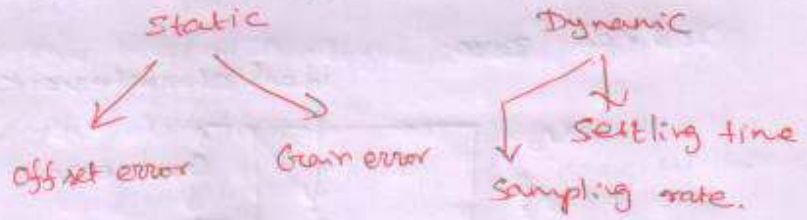
Analog & digital data conversion:-

- Digital to Analog Conversion (D/A)
- Analog to Digital Conversion (A/D).

Digital to Analog conversion specification:-

The internal circuitry of a digital to analog converter is subject to component mismatching drift aging, noise and other source of error, whose effect is to degrade conversion performance.

The DAC errors are classified into two types as i) static
ii) dynamic.



The accuracy of DAC is measured by the maximum deviation of the actual output from the ideal value and is expressed in

Off Set error:-

Offset error is defined as the ... of actual output from ideal output the ideal output should be zero.

The offset error is nulled by ... the actual signal to up or down ... goes through the origin.

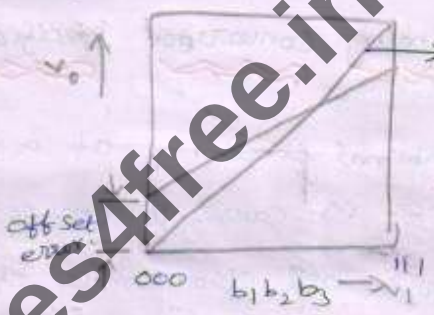
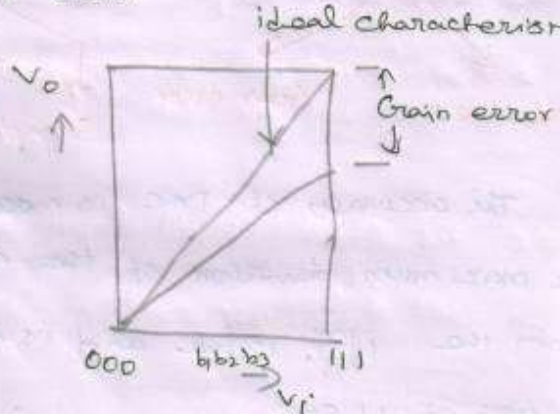


Fig DAC off... er...

Gain error:-

Grain error is a difference b/w ideal and actual value of output at full scale value, when the offset error has been reduced zero.



Monotonicity :-

A monotonic D/A Converter is one in which the output always increases as the input increases.

If the maximum DNL error is less than 1LSB, then a D/A Converter is guaranteed to be monotonic.

Settling Time

In D/A converter, the settling time is defined as the time it takes for the converter to settle with in some specified amount of the final value.

Sampling rate:

Sampling rate is the rate at which samples can be continously converted and is typically the inversion of the conversion time.

weighted Resistor DAC

Circuit uses a summing amplifier a binary weighted resistor network.

It has n-electronic switches d_1, d_2, Controlled by binary input word. These switches are Single pole double throw type

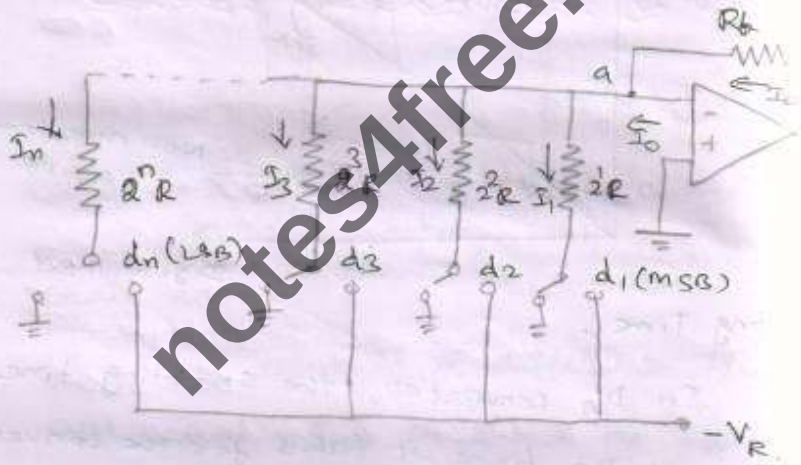


Fig:- Simple weighted resistor DAC

If the binary input to a particular S is 1. it connects the resistance to the ref voltage ($-V_R$)

If the input (binary digit) bit is 0, the switch connects the resistor to the ground

4.5

The output current I_o for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + I_3 + \dots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \dots + \frac{V_R}{2^n R} d_n$$

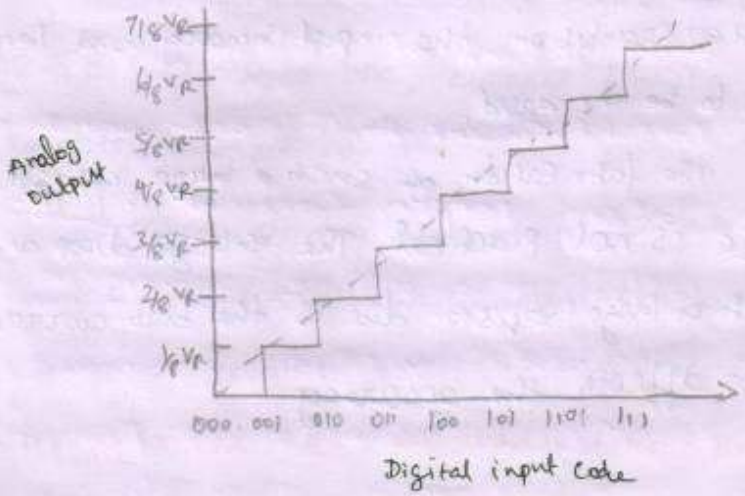
$$I_o = \frac{V_R}{R} \left(d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n} \right)$$

For a voltage output DAC, the D/A converter is described as

$$V_o = k V_{FS} \left(d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n} \right)$$

Compare the voltage and current eqns

if $R_f = R$ then $k = 1$ and $V_{FS} = V_R$



The circuit uses a negative reference

The analog output voltage is -ve staircase for a 3-bit weighted resistor DAC

i) Although the op-amp is connected in inverting mode, it can also be connected non-inverting mode

ii) The op-amp is simply working as a current to voltage converter.

iii) The Polarity of the reference voltage chosen in accordance with the type of the switch used.

Disadvantage:-

Wide range of resistor values required better resolution the input binary word length has to be increased.

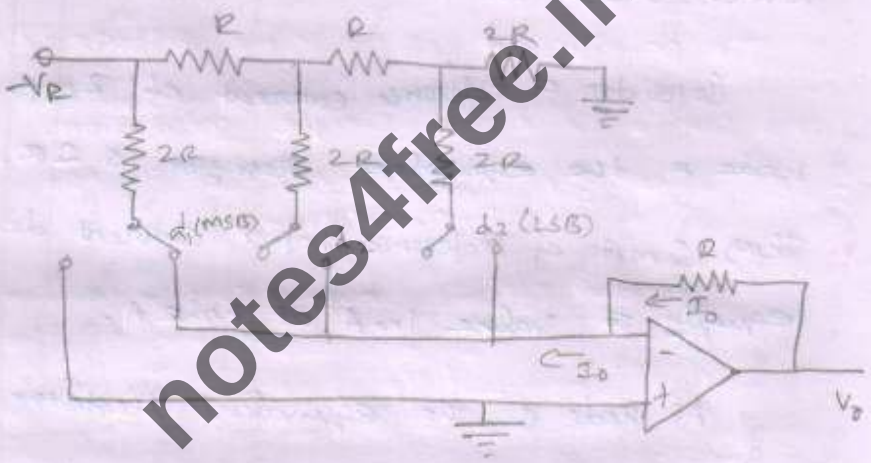
The fabrication of such a large resistance in IC is not practical. The voltage drop across such a large resistor due to the bias current also affects the accuracy.

4.7

R-2R Ladder DAC

- Current mode R-2R Ladder type
- Voltage mode R-2R Ladder type

Current mode R-2R ladder type:-



In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes

More power dissipation causes heating which creates non-linearity in DAC. The Serious problem can be avoided completely in Inverted R-2R ladder type DAC.

A 3-bit inverted R-2R ladder type DA where the position of MSB and LSB interchanged.

Each input binary word connects t Corresponding switch either to ground the inverting input terminal of the OP which is also at virtual ground.

Consider a reference current of 2m node A the equivalent resistor is 2R Thus 2mA of reference input current d equally to value 1mA at node A.

At node B. the equivalent resist 2R. Thus 1mA of current further di to value 0.5mA at nodes.

Constant Current in each branch the ladder implies constant voltage the ladder node voltage remain cons at $V_R/2^0$, $V_R/2^1$, $V_R/2^2$.

The circuit works on the princip of summing currents and is also said

where

I_{out} – output current

R_f – the feedback resistor of op-amp

I_{out} – currents resolution X D.

$V_o = -$ (current resolution $\times D$) R_f

$= -$ (current resolution $\times R_f$) D

The co-efficient of D is the voltage V_o and can be called as example resolution.

$V_o =$ resolution $\times D$.

In actual circuit output can be written

$$V_o = -\left(\frac{V_R}{R} \times \frac{1}{2^n} R_f\right) \times D$$

The resolution of R/2R Ladder type DAC current o/p is

$$\text{resolution} = \frac{1}{2^n} \times \frac{V_R}{R}$$

$$\text{resolution} = \left(\frac{1}{2^n} \times \frac{V_R}{R}\right) \times R_f.$$

Advantage:-

i) Easier to build accurately as only two precision metal film resistor are required

ii) Number of bits can be expanded by adding more sections of same R/2R valu

4.16

Switches for DAC converters:-

There is always a need for switches in circuits and systems involving analog signals.

The closing & opening of the switches control the signal flow.

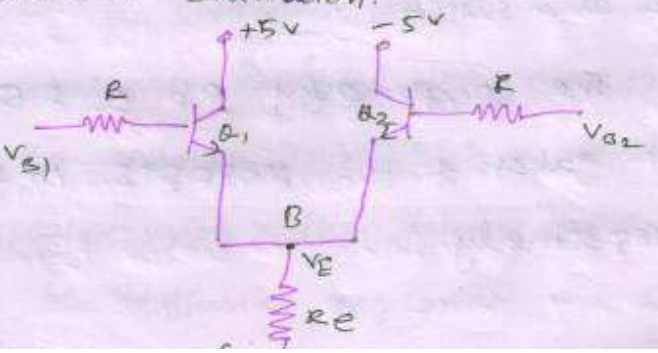
These switches are normally operated by digital signals.

Switches Emitter follower:-

The diodes & transistors can be used as switches in D/A convertors.

The characteristics of FETs acting as simple resistors make them ideal switches.

The Bipolar transistors also have negligible resistance when they are operated in Saturation.



The switching arrangement of a D/A converter using two transistors connected as emitter followers.

The Bipolar transistors offer neg resistance when operated in saturation

Switches of MOS transistor

The totem pole MOSFET switch is connected in series with the resistors of the 2R N/W.

Therefore the ON resistance of the switch must be very low & they should operate with zero offset voltage.

The inherent offset voltage of bipolar transistor, when in saturation limits use as a switch.

The complementary of Q & $\bar{Q}$ drive the gates of the MOSFETS M_1 & M_2 respectively

4.13

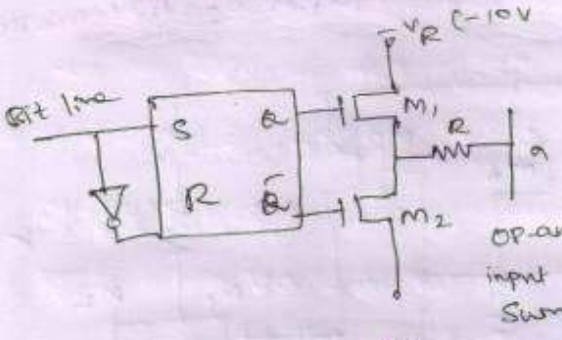


Fig. Totem pole MOSFET

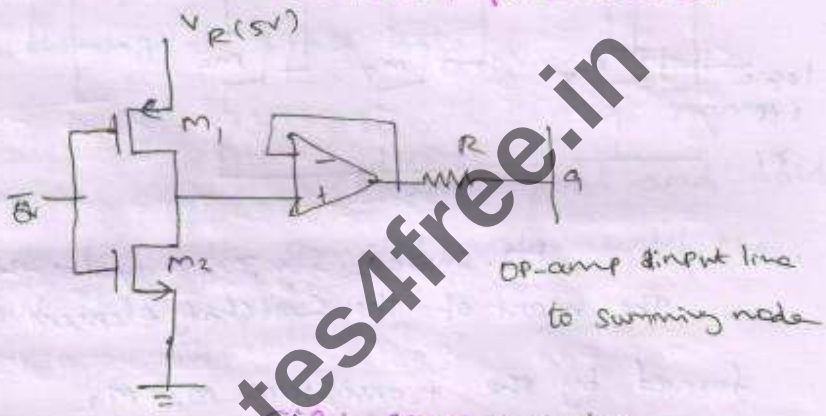


Fig:- CMOS inverter

Switches using CMOS inverter

R-2R ladder D/A Converter are suitable for monolithic fabrication in CMOS technology.

The switches for such D/A Converters are realized using CMOS transistors and the ladder resistors R and 2R fabricated using thin film deposition over the diffusion region in the CMOS die.

Switches for multiplying types of A/D co

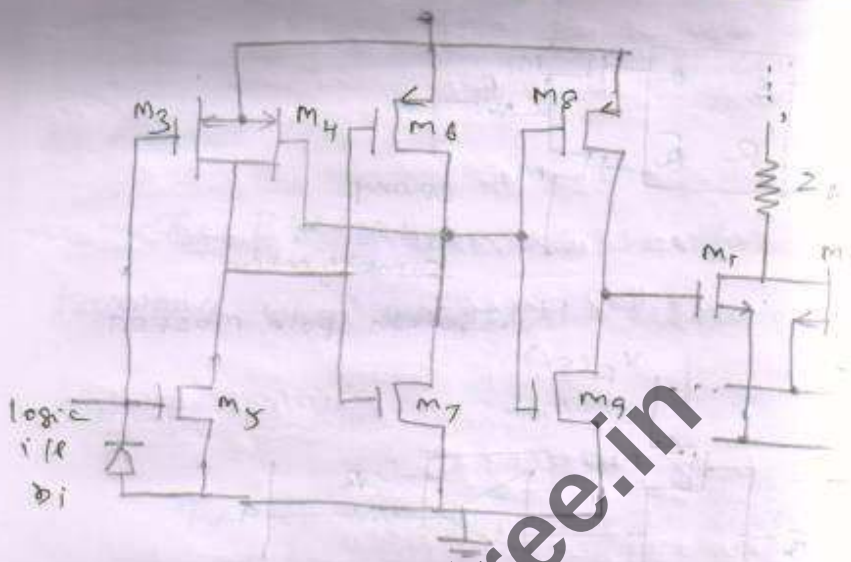


Fig. Switches for D/A Converter using

The heart of the switching element is formed by the transistors M_1 & M_2

The remaining transistors accept TTL or CMOS compatible logic inputs and provide the anti-phase gate drives for the transistors M_1 & M_2.

When the logic input is 0 M_1 is OFF and M_2 is ON. Therefore the current I_R is diverted to the I_0 bus.

When the logic i/p is 1 M_1 is ON & is OFF. Therefore the current I_R is diverted to the I_0 bus.

4.5

High Speed sample & Hold Circuit.

Accurate analog to digital conversion the analog input voltage should be held constant during the conversion cycle.

If the analog input voltage changes by more than $\pm \frac{1}{2}$ LSB an error can occur in the digital output code.

The sample and hold circuit name implies, sample an input signal and holds on to its last sampled value until the input is sampled again.

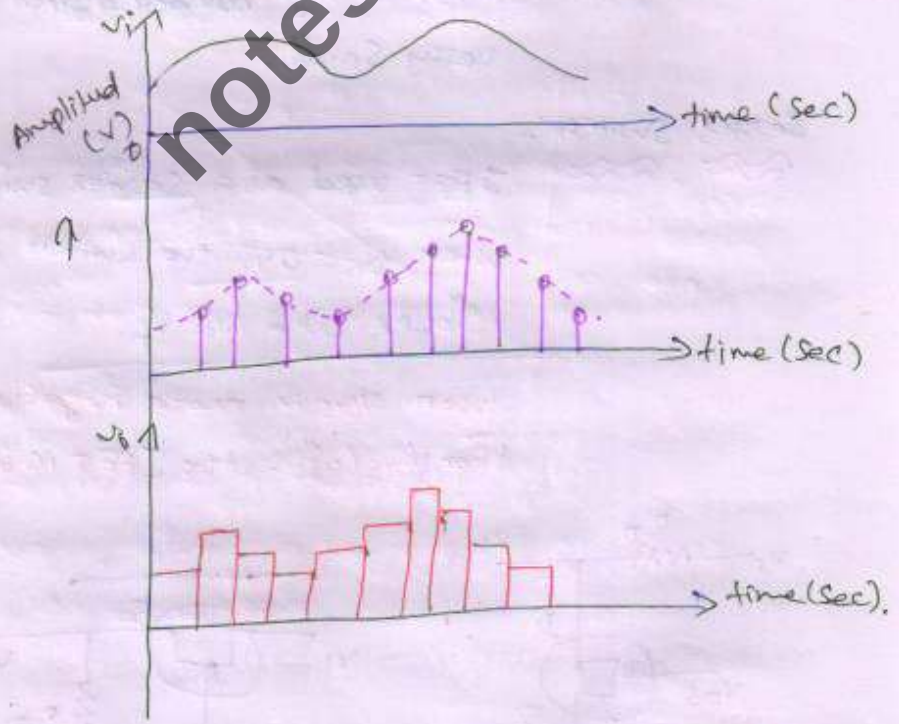


Fig:- input output response of sample & hold

Analog switches :-

JFET can be used as an analog switch. Gate – Source voltage V_{GS} is restricted two values :- 0V or a few negative voltage.

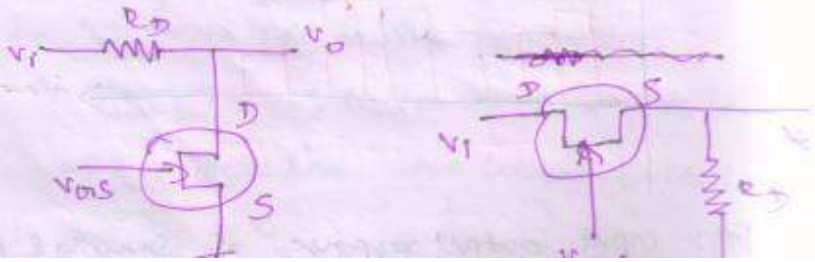
Shunt switch :-

JFET used shut switch when $V_{GS} = 0$. JFET acts as closed switch & $R_{DS} << R$ so the voltage divider action very small.

Series switch :-

JFET used as a series switch when $V_{GS} = 0V$. the switch closed and $V_o = V_i$.

When V_{GS} is more negative than $V_{GS(off)}$. the JFET is off



4.17

Performance :-

1) Acquisition time – (t_{ac})

2) Aperture Time – (t_{ap})

3) Hold mode Settling Time – (t_s)

4) Hold step – The time of switching b/w sample & hold mode

5) Feed through

6) Voltage droop.

Advantage :-

* Synchronization can be achived.

* It also reduces the cross talk in the multiplexer.

Application :

* Digital interfacing

* ADC circuits.

* Pulse modulation Sys.

* Analog demultiplexer

* ref – Stabilished OP-amp.

A/D Converter Specifications:-

Analog to digital converter S... to D/A converter performance also characterized interms of offset a... gain error:..

Offset error

The deviation of $V_{00\ldots01}$ fr... 0.5 LSB.

The offset error is the differe... between the actual location of the ... binary code transition and $\frac{1}{2}$ LSB. and the ideal separation of V_{FSR} -2 LSB.

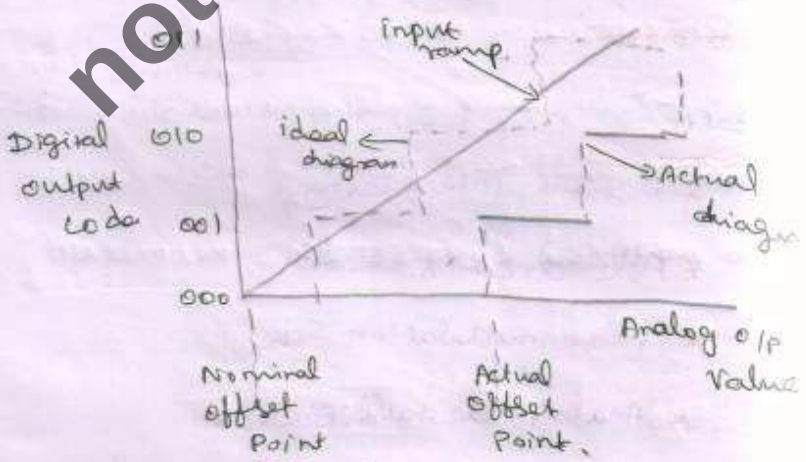


Fig. offset error of A/D con...

4.19

Gain Error :-

The gain error is the difference between the actual locations of the last and first transition and the ideal separation of V_{FSR} - 2LSB.

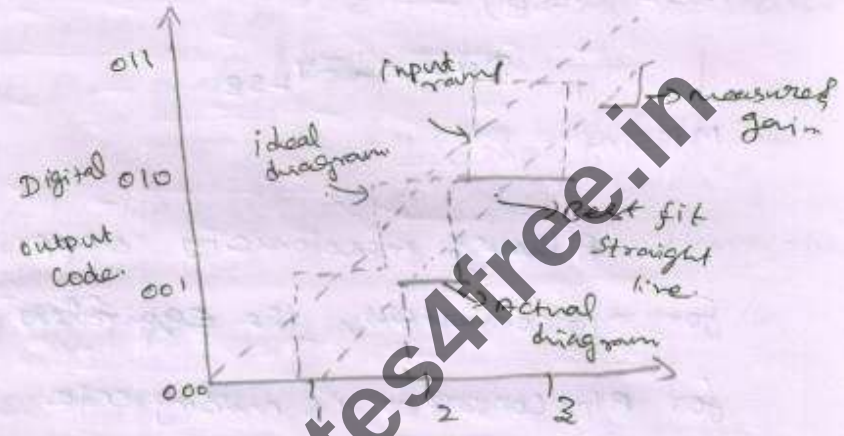


Fig Gain error of A/D converter.

Integral Non linearity Error :-

The largest vertical difference b/w the code center point of the actual transfer curve and the line connecting the endpoints on the curve is called as Integral Non-linearity Error.

Differential Nonlinearity Error:-

The largest deviation (d) between the actual difference of two adjacent threshold voltages and the ideal diff value (V_{LSB})

$$DNL = d - V_{LSB}$$

Missing Codes:-

Although monotonicity is appropriate for D/A converters, the equivalent term for A/D converter is missing code.

A/D converter is guaranteed not to have any missing code if the maximum DNL error is less than 1LSB or if the maximum INL error is less than 0.5LSB

Code width:-

The width of a given output code is the range of analog input voltages for which that code is produced.

4.21

The code widths are referenced to the weight of 1 least significant bit (LSB) which is defined by the resolution of the converter and the analog reference voltage.

Acquisition time:-

A successive approximation A/D converter will have a track and hold circuit at the analog input.

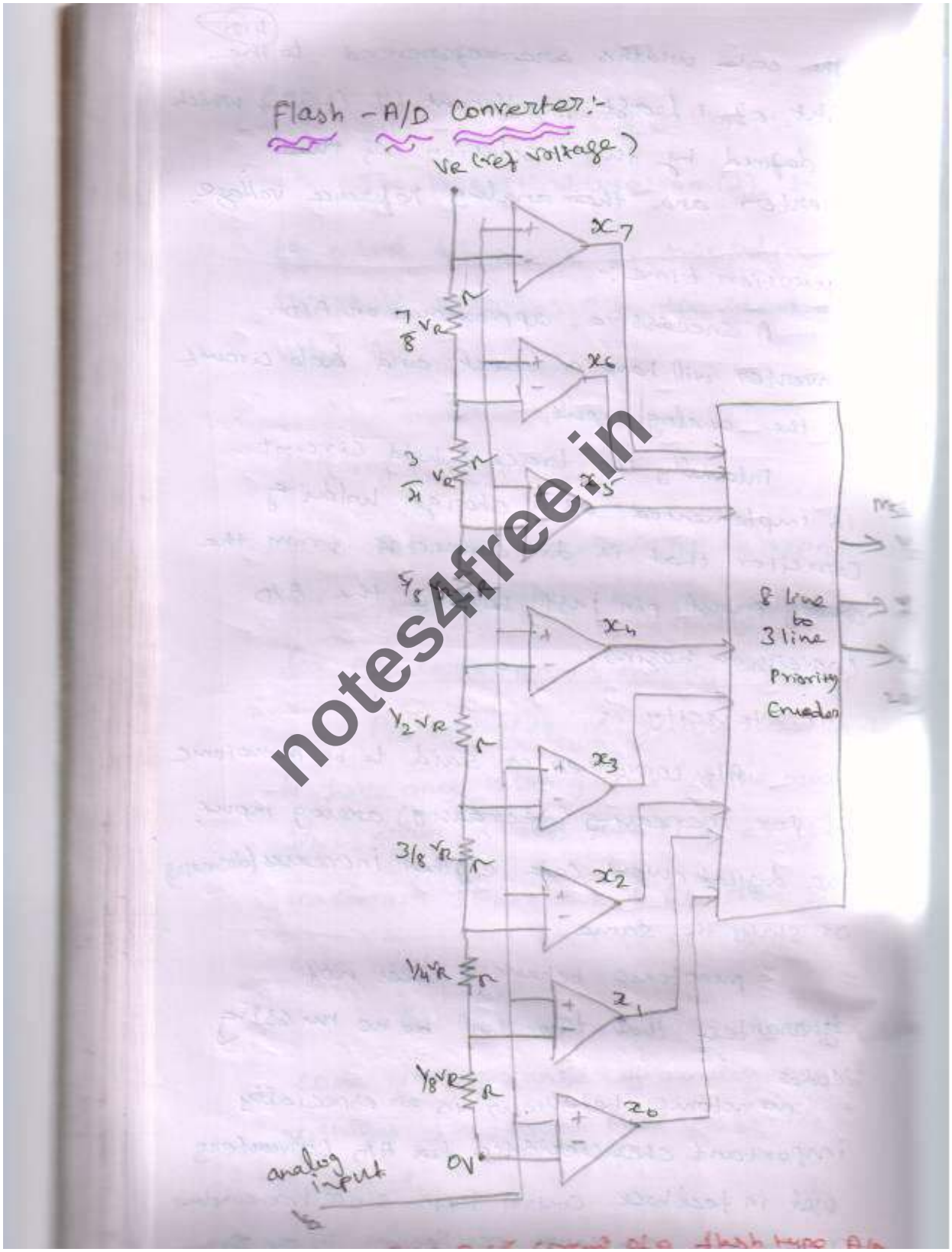
Internally the track & hold circuit is implemented as a charge holding capacitor that is disconnected from the analog input pin just before the A/D conversion begins.

Monotonicity:-

A/D converter is said to be monotonic if for increasing (decreasing) analog input, the digital output code either increases (decreases) or stays the same.

monotonic behaviour does not guarantee that there will be no missing codes.

monotonic behaviour is an especially important characteristic for A/D converters used in feedback control loops since non-monotonic response can cause oscillations in the



4.23

This is simple A/D converter and the fastest and most expensive technique

3 bit A/D converter consists of a resistive divider network & op-amp comparator and a 8 line to 3 line encoder (3 bit priority encoder).

If $V_a > V_d$ is voltage input
the logic o/p x = 1

If $V_a < V_d$ is voltage input
the logic o/p x = 0

If $V_a =$ is voltage input
the logic o/p is previous value.

At each node of the resistive divider a comparison voltage is available.

Advantage

High speed of conversion takes place.

The conversation time is 100ns or less.

Disadvantage

The number of comparators required almost doubles for each added bit.

Input voltage (va)	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to Vr/8	0	0	0	0	0	0	0	1	0	0	0
Vr/8 to Vr/4	0	0	0	0	0	0	1	1	0	0	1
Vr/4 to 3Vr/8	0	0	0	0	0	1	1	1	0	1	0
3Vr/8 to Vr/2	0	0	0	0	1	1	1	1	0	1	1
Vr/2 to 5Vr/8	0	0	0	1	1	1	1	1	1	0	0
5Vr/8 to 3Vr/4	0	0	1	1	1	1	1	1	1	0	1
3Vr/4 to 7Vr/8	0	1	1	1	1	1	1	1	1	1	0
7Vr/8 to Vr	1	1	1	1	1	1	1	1	1	1	1

4.25

Successive Approximation Converter.

Successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n clock periods.

An eight bit converter would require eight clock pulses to obtain a digital o/p

The block diagram consists of a DAC a comparator and a successive Approximation register (SAR)

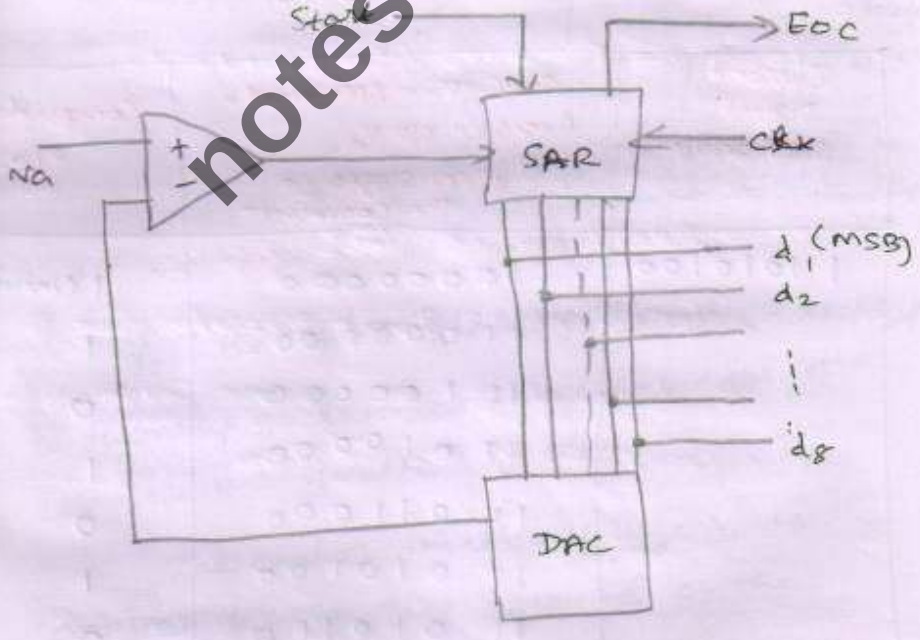


Fig:- Functional diagram of Successive Approximation ADC.

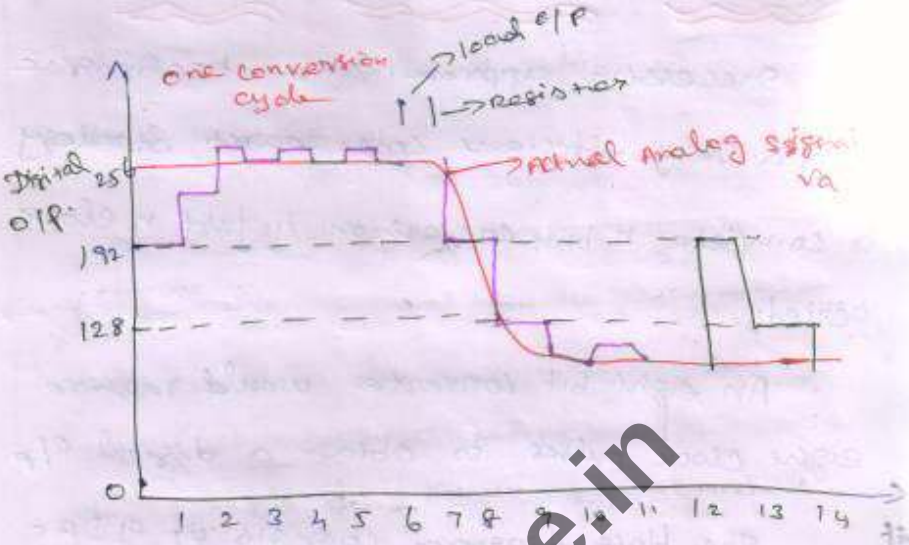


fig: Successive approximation conversion sequence for a typical analog input.

Current Digital Representation	Successive Approximation Register o/p V_a, different stages in the conversion	Comparator o/p
1 1 0 1 0 0	1 0 0 0 0 0 0 0	1 (initial)
	1 1 0 0 0 0 0 0	1
	1 1 1 0 0 0 0 0	0
	1 1 0 1 0 0 0 0	1
	1 1 0 1 1 0 0 0	0
	1 1 0 1 0 1 0 0	1
	1 1 0 1 0 1 1 0	0
	1 1 0 1 0 1 0 1	0
	1 1 0 1 0 1 0 1	

4.27

Single Slope ADC:

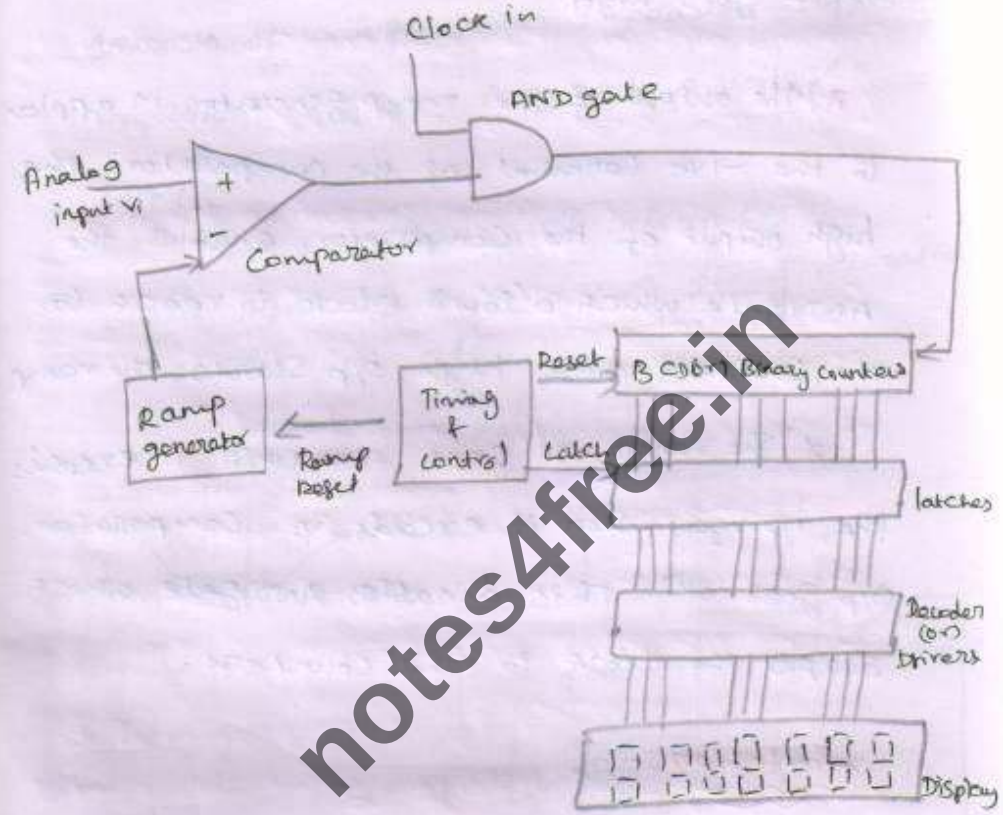


Fig. Single Slope ADC

At the start the reset signal is provided to the ramp generator and the counters. the counters are resetted to 0's.

The analog input's voltage V_i is applied to the +ive terminal of the Comparator.

*) If the analog input is more +ive than the -ive input of the comparator and comparator output goes high.

*) The output of the ramp generator is applied to the -ive terminal of the comparator. high output of the comparator enables the AND gate which allows clock to reach the counters and high o/p starts the counter.

*) The ramp vge goes +ive until it exceeds the i/p vge, when it exceeds Vi. Comparator o/p goes low. This disables AND gate which stops the clock to the counters.

Limitation :-

*) Resolution is less

*) variations in ramp generator due to time, temperature or i/p vge sensitivity also cause a lot of problem.

4.29

Dual slope ADC.

The analog part of the circuit consists of a high input impedance buffer A_1, precision integrator A_2, and a voltage comparator.

The converter first integrates the analog input signal V_a for a fixed duration of 2^n clock periods.

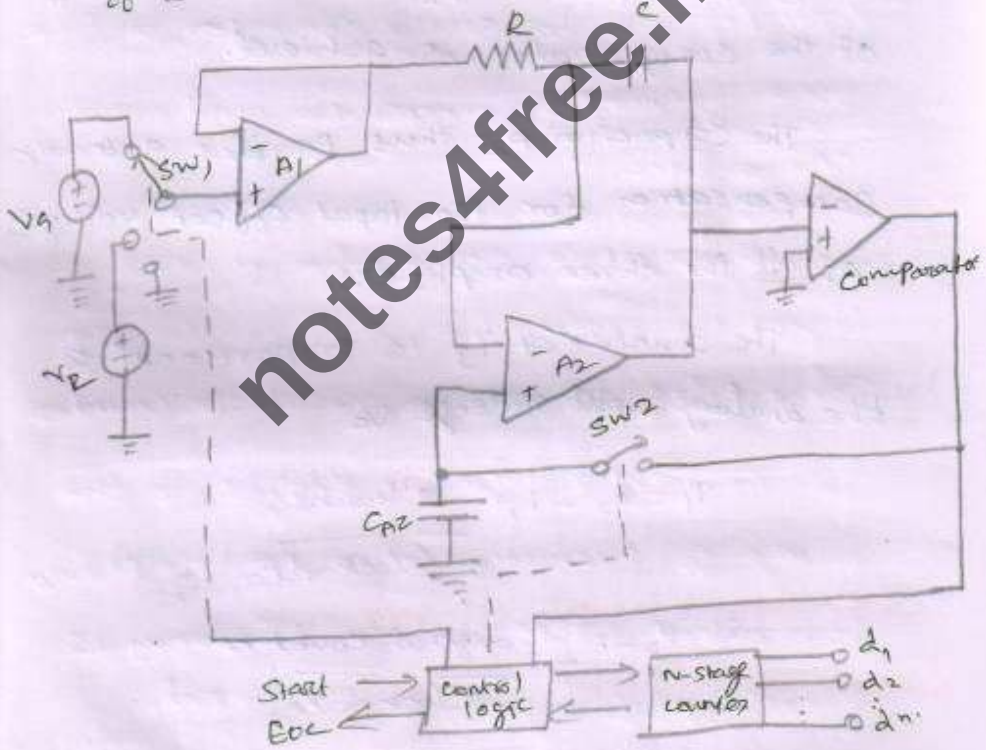


Fig. Dual Slop ADC.

N represents desired O/p Code

operation of the circuit Before the Command arrives, the switch SW_1 is co to ground and SW_2 is closed.

Any offset voltage present in the A Comparator loop after integration, appe across the capacitor C_{AZ} till the thresh of the comparator is achieved.

The capacitor C_2 thus provides auto Compensation for the input offset Vol of all the three amplifiers.

The counter at t_3 is proportional the analog input voltage Va

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{Clock rate.}}$$

& $$t_3 - t_2 = \frac{\text{digital count N}}{\text{Clock rate.}}$$

For an integrator

$$\Delta V_0 = (-1/RC)\, V(\Delta t)$$

The voltage V_1 is given by

4.31

$$V_1 = (-1/RC)(-V_R)(t_2 - t_3)$$

$$(-1/RC)\, V_a (t_2 - t_1) = (-1/RC)(-V_R)(t_2 - t_3)$$

$$V_a (t_2 - t_1) = (-V_R)(-)(t_3 - t_2)$$

$$V_a (t_2 - t_1) = V_R (t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$.

$$V_a (2^n) = V_R N$$

$$\boxed{V_a = V_R (N/2^n)}$$

Advantage:-

* It is highly accurate.
* Cost is low.
* It is immune to temperature. Caused variations in R_1 & C_1

Applications:-

* It is used in digital panel meters.
* Microprocessor based display versions.
* Direct LED displays.

A/D converter using voltage to Time Conver

The voltage to time conversion can be easily obtained by using voltage to frequ converter.

Time is reciprocal of the freque the frequency o/p of voltage to frequen converter can be easily converted to ti using a counter, monostable multivibrator and a latch.

A negative going pulse is used to trigger the monostable multivibrator. The same pulse is used to reset the counter

The input voltage is applied to the voltage to frequency converter. It produces the output pulses whose frequency is linearly proportional to the input.

When the trigger is applied to the monostable multivibrator its output goes high for the particular time period

4.33

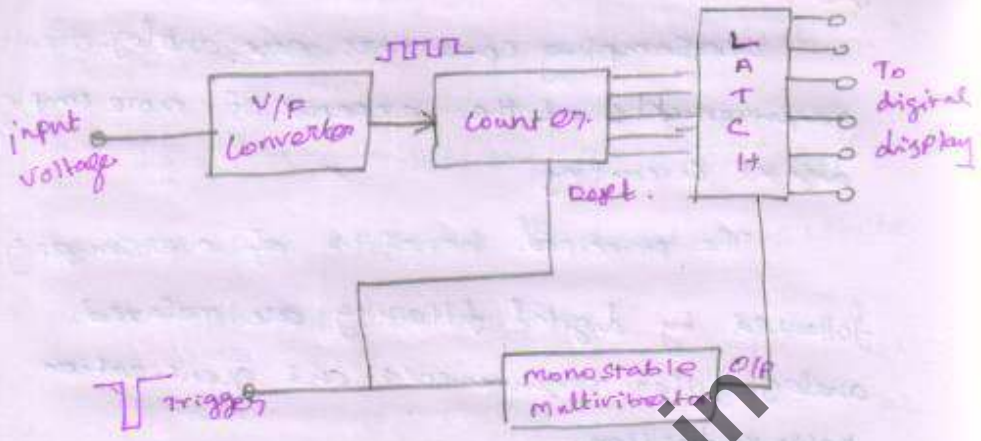


Fig. Voltage to Time Converter.

At the same time the Counter starts counting the pulses. After the time period of monostable multivibrator, its output goes low.

This output is applied to the latch which is negative edge triggered. Hence the Counter output gets latched.

The output is then displayed by the decade counting assemblies.

Over Sampling A/D Converters:-

Oversampling converters ease analog requirements at the expense of more digital circuitry

The principal benefits of oversam followed by digital filtering are relaxed analog-filter requirements and quantizat noise reduction.

It has addition benefits that is hig resolution (≥ 16 bits)

The digitization process of the input signal from dc to the sampling frequency

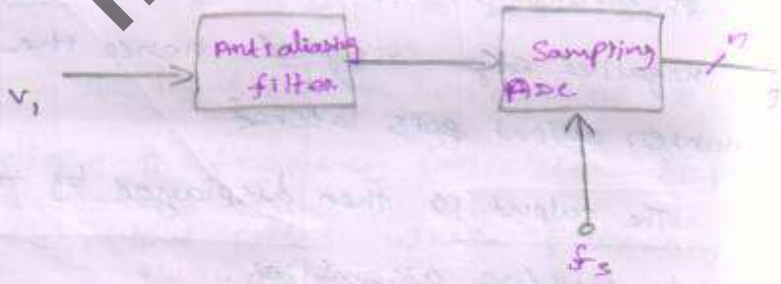


Fig. Nyquist sampling with analo filte

The range consists of two zones. Zone I extending from dc to $f_{s/2}$ and Zone II extending from f_{r2} to f_c.

4.35

Zone-I is also called the baseband. and

$f_{s/2}$ is called Nyquist bandwidth.

If v_i is a relatively active or busy signal its quantization noise can be treated as white noise with spectral density

$$e_q = \frac{q}{\sqrt{f_{s/2}}}$$

where $q = \frac{V_{FSR}}{2^n\sqrt{12}}$

The rms value

$$E_q = \frac{V_{FSR}}{2^n\sqrt{12}}$$

The result is

$$SNR_{max} = 6.02n + 1.76 dB.$$

Nyquist criterion states that if we want to recover or reconstruct a signal of a given bandwidth f_B from its digitized version, the sampling rate f_s must be

$$f_s > 2f_B$$

↳ Nyquist rate.

Consider the effect of speeding up the sampling rate by a factor of K, $K>>1$

The transition band of the analog filter preceding the digitizer is now much wide providing an opportunity for a drastic redu

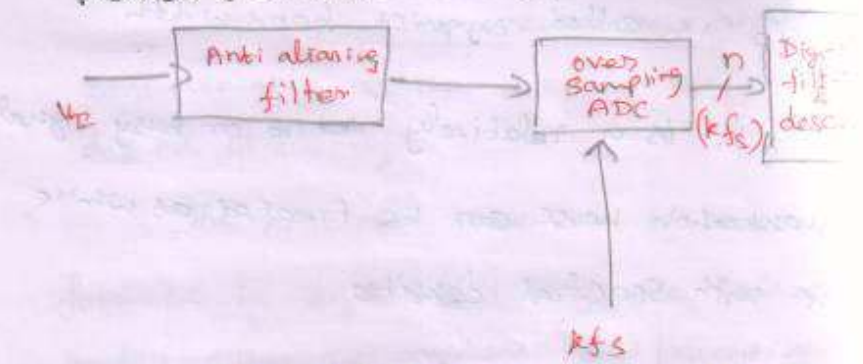


Fig:- over sampling with analog & digital filtering.

The quantization noise is now spread over a wider band

$$e_{qv} = \frac{q}{\sqrt{k f_s / 2}}$$

indicating a spectral - density reduction by

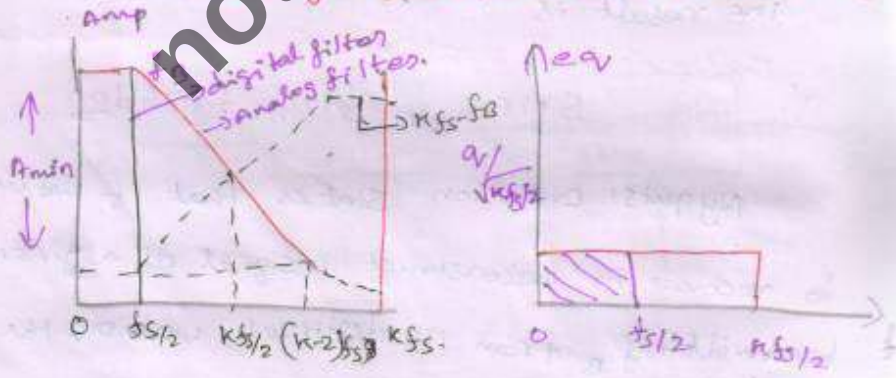


Fig:- Spectral density of oversampl

The rms noise at the o/p of the digitizer is $= \frac{V_{FSR}}{2^n \sqrt{12}}$

Eq. $\frac{V_{FS}}{2^n \sqrt{12k}}$ expressing km the form $k = 2^m$

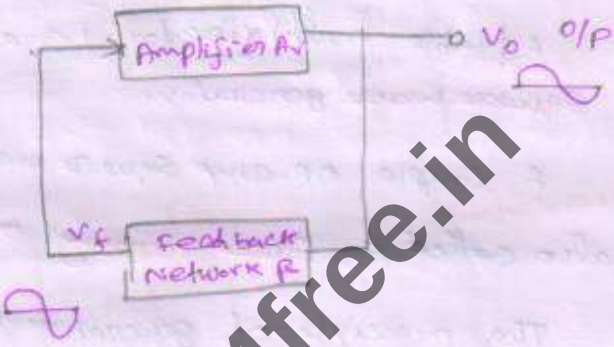
SNR = 6.02 (n+0.5m) + 1.76dB

5-1

UNIT – V

WAVEFORM GENERATORS & SPECIAL FUNCTION IC's.

Sine-wave generator :-

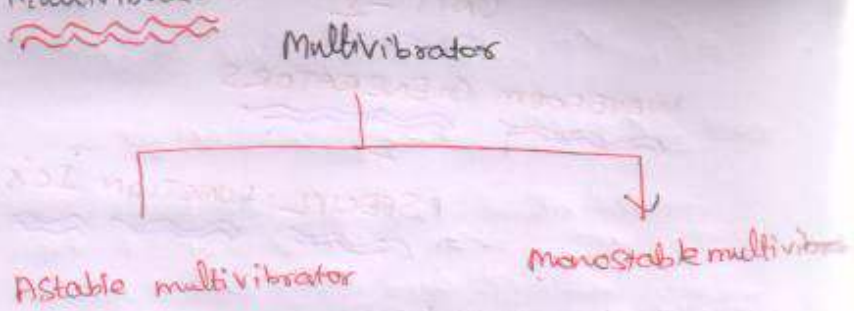


*) AS oscillator is basically a feed back circuit where a fraction V_f of the output voltage V_o of an amplifier is fedback to the input in the same phase.

*) For sustained oscillation $A_v\beta = 1$ that is magnitude condition $|A_v\beta| = 1$ and phase condition $A_v\beta = 0°$ or $360°$ must simultaneously satisfied in the circuit

*) There are different types of sine-wave oscillators available according to the range of frequency, namely RC oscillators for audio frequency and LC oscillators for radio frequency range.

Multivibrator:-



AStable Multivibrator:-

AStable multivibrator is also known as Square wave generator.

A single op-amp square wave generator is also called a Free running Oscillator.

The principle of generation of Square wave output is to force an op-amp to operate in the Saturation region.

The circuit conditions oscillate b/w these two quasi-Stable State.

Fraction $\beta = R_2/(R_1+R_2)$ of the output is fedback to the (+) input terminal.

Thus the reference voltage V_{ref} is βV_o and may take values as $+\beta V_{sat}$ or $-\beta V_{sat}$

The output is also fedback to the (-) input terminal after integrating by means of a low – pass RC

5.3

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to βV_{sat} & vice versa.

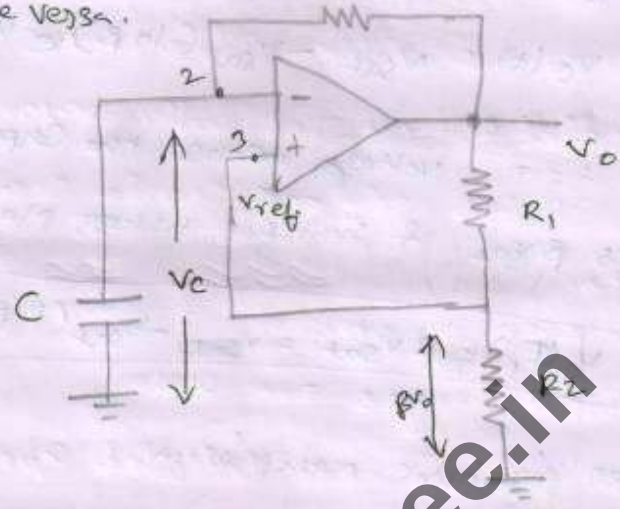


Fig:- Op-amp Square wave generator

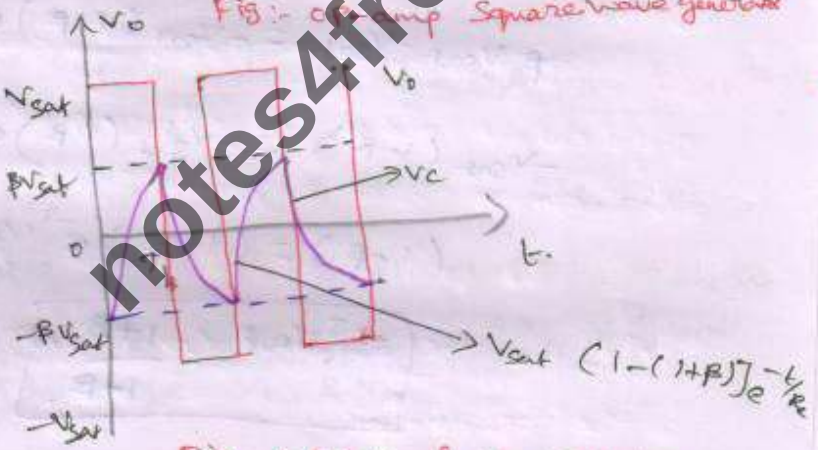


Fig. output & V_c waveform.

the voltage across the capacitor as a function of time is given by

$$V_i(t) = V_f + (V_i - V_f)\, e^{-t/RC}$$

$V_f = +V_{sat}$ → final value.

$V_i = -\beta V_{sat}$ → initial value

Therefore

$$v_C(t) = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-t/RC}$$

$$v_C(t) = V_{sat} - V_{sat}(1+\beta) e^{-t/RC}$$

At $t = T_1$, voltage across the capacitor reaches βV_{sat} & switches takes place

$$v_C(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta) e^{-T_1/RC}$$

After algebraic manipulation.

$$\beta V_{sat} - V_{sat} = -V_{sat}(1+\beta) e^{-T_1/RC}$$

$$-V_{sat}(1-\beta) = -V_{sat}(1+\beta) e^{-T_1/RC}$$

$$(1-\beta) = (1+\beta) e^{-T_1/RC}$$

$$e^{T_1/RC} = \frac{1+\beta}{1-\beta}$$

Taking natural log.

$$T_1 = RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

This gives only one half of the period

Total time period

$$T = 2T_1$$

$$T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

5.5

The output waveform is Symmetrical.

If $R_1 = R_2$ then $\beta = 0.5$

$$T = 2RC \ln\left(\frac{1+0.5}{1-0.5}\right)$$

$$= 2RC \ln\left(\frac{1.5}{0.5}\right)$$

$$= 2RC \ln(3)$$

For $T = 2RC$

$$f_0 = \frac{1}{T} = \frac{1}{2RC}.$$

The output voltage swings from $+V_{sat}$ to $-V_{sat}$

V_o Peak to peak $= 2V_{sat}$.

If an Asymmetric Square wave is desired the zener diods with different breakdown vge V_{z1} & V_{z2}

The output is either V_{o1} (or) V_{o2}

$$V_{o1} = V_{z1} + V_D$$

$$V_{o2} = V_{z2} + V_D$$

The positive section

$$T_1 = RC \ln\left(\frac{1+\beta(V_{o2}/V_{o1})}{1-\beta}\right)$$

The duration of -ive section T_2 will be the T_1 eqn with V_{o1} & V_{o2}

Monostable multivibrator:-

The monostable multivibrator is also called as one-shot multivibrator

It has only one stable state exists.

When an external trigger is appli the output changes its state.

The new state is called quasi-stable state.

The circuit is useful for generating single output pulse of adjustable time dura is response to a triggering signal.

The width of the output pulse depend only the one external components connected to the op-amp.

To analyse the circuit Assume that in the stable state. Output V_o is at $+V_{sat}$.

The +ive trigger of magnitude V_i is applied to the +ive input terminal.

(ie) $([\beta V_{sat} + (-V_i)] < 0.7V)$.

5.7

The output of the op-amp will switch from $+V_{sat}$ to $-V_{sat}$.

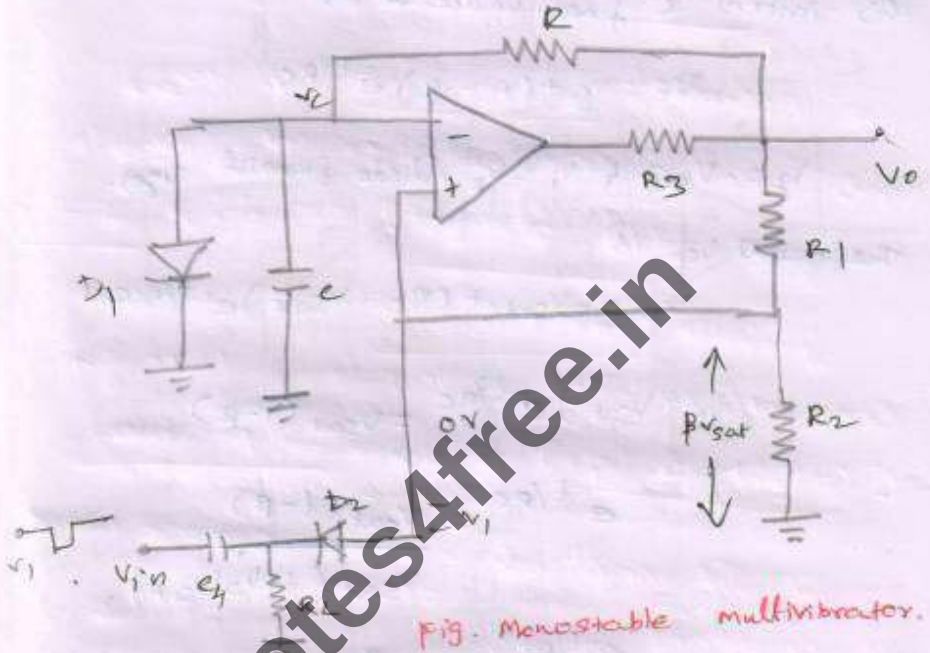
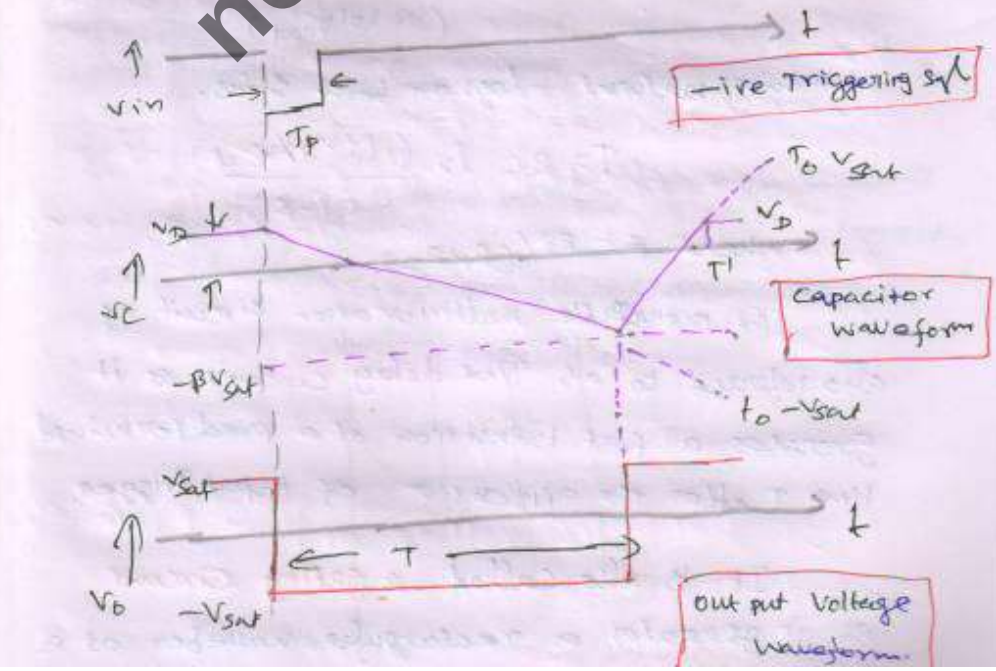


Fig. Monostable multivibrator.



The general Solution for a single time constant low pass RC circuit with v_i & V_2 as initial & final values is

$$V_o = V_f + (V_i - V_f) e^{-t/RC}.$$

$V_f = -V_{sat}$ & $V_i = V_D$ (diode forward V_{fe}).

The output V_c is

$$V_c = -V_{sat} + (V_D + V_{sat}) e^{-t/RC}$$

$$(V_D + V_{sat}) e^{-t/RC} = V_{sat}(1-\beta)$$

$$e^{-t/RC} = \frac{V_{sat}(1-\beta)}{V_{sat}(1+V_D/V_{sat})}.$$

$$e^{-t/RC} = \frac{1-\beta}{(1+V_D/V_{sat})}$$

Taking natural log on both sides.

$$T = RC \ln \frac{(1+V_D/V_{sat})}{(1-\beta)}$$

where $\beta = R_2/(R_1+R_2)$.

The monostable multivibration circuit is also referred to as Time delay circuit as it generates a fast transition at a predetermined time T after the application of input Trigger.

It is also called a gating circuit as it generates a rectangular waveform at a

Triangular wave generator :-

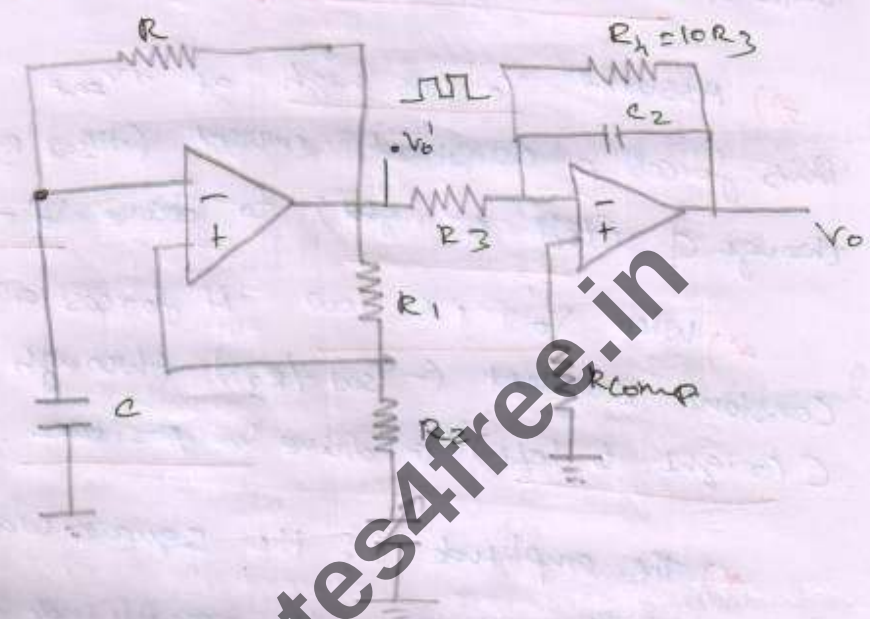


Fig :- Triangular wave generator

*) A triangular wave can be obtained by integrating a square wave.

*) A triangular wave generator can be formed by simply connecting an integrator to the square wave generator.

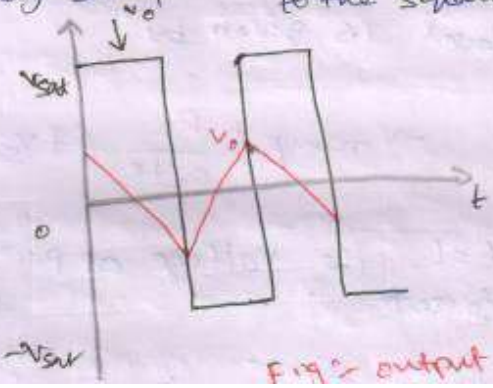


Fig :- output waveform.

*) Triangular wave is generated by alternatively charging & discharging a cap with a constant current.

*) Assume V_o' is high at $+V_{sat}$ This forces a constant current ($+V_{sat}/R$) through C (left to right) to drive V_o

*) When V_o' is low it forces a constant current ($-V_{sat}/R_3$) through C (right to left) to drive V_o positive.

*) The amplitude of the square wave is constant at $\pm V_{sat}$ the amplitude of the triangular wave will decrease as the frequency increases.

*) The effective voltage at point P during the time when o/p of A_1 is at $+V_{sat}$ level is given by

$$-V_{ramp} + \frac{R_2}{R_2+R_3}(+V_{sat} - (-V_{ramp}))$$

At $t=t_1$, the voltage at point P becomes equal to zero.

III^{rly} at $t = t_2$ when the output of A_1 switches from $-V_{sat}$ to $+V_{sat}$ (5.11)

$$V_{ramp} = -\frac{R_2}{R_3}(-V_{sat})$$

$$V_{ramp} = \frac{R_2}{R_3}(V_{sat})$$

*) Peak to peak amplitude of the triangular wave is

$$V_o(PP) = +V_{ramp} - (-V_{ramp})$$

$$= 2 \frac{R_2}{R_3} V_{sat}.$$

*) Putting the value in the basic integral equation

$$V_o = -\frac{1}{RC}\int v_i\,dt.$$

$$V_o(PP) = -\frac{1}{R_1C_1}\int_0^{T/2} (-V_{sat})\,dt$$

$$= \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right)$$

$$T = \frac{2R_1C_1V_o(PP)}{V_{sat}}$$

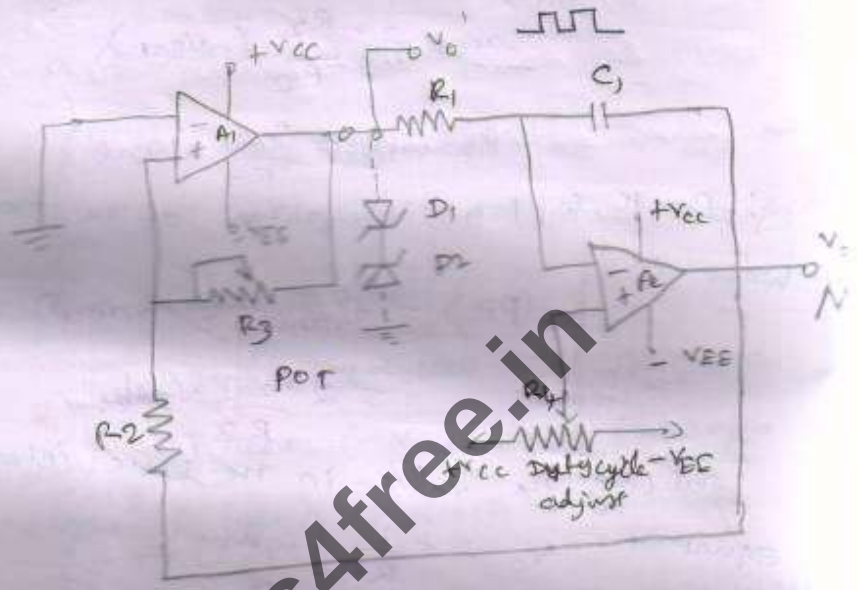
*) Sub the value of $V_o(PP)$ from eqn $2\frac{R_2}{R_3}V_{sat}$

$$T = \frac{2R_1C_1(2R_2/R_3)V_{sat}}{V_{sat}}$$

$$T = \frac{4R_1C_1R_2}{R_3}$$

Hence the frequency of oscillation f_o is

Saw-tooth wave generator:-



* The difference between the triangular and Sawtooth waveform is that the rise time of the triangular wave is always equal to its fall time.

* The same amount of time is required for the triangular wave to swing from $-V_{ramp}$ to $+V_{ramp}$ as for $+V_{ramp}$ to $-V_{ramp}$

* The Sawtooth wavefor has unequal rise and fall times. It may rise +ively many times faster than it falls -ively

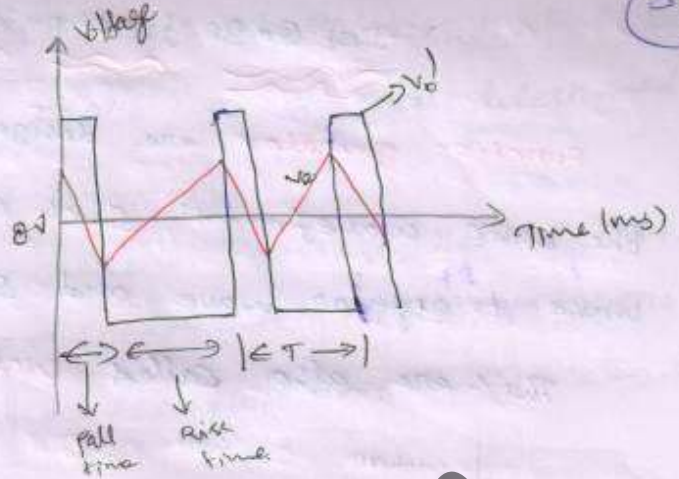


Fig. output waveform

* This can be accomplished by using the potentiometer and connecting it to $+V_{CC}$ and $-V_{EE}$
* Depending on the R_4 value fixing a certain dc level is inserted in the output of A_2.
* The output A_2 will be a triangular wave riding on some dc level that is a function of the R_4 setting.
* The duty cycle of the square wave will be determined by the polarity & amplitude of this dc level.
* If duty cycle less the 50% will then cause the output of A_2 to be a sawtooth.
* The amplitude of the sawtooth wave is independent of the R_4 setting.

ICL 8038 function generator.

Function generator are designed to provide the basic waveforms such as square wave triangular wave and sine wave. This are also called waveform generator

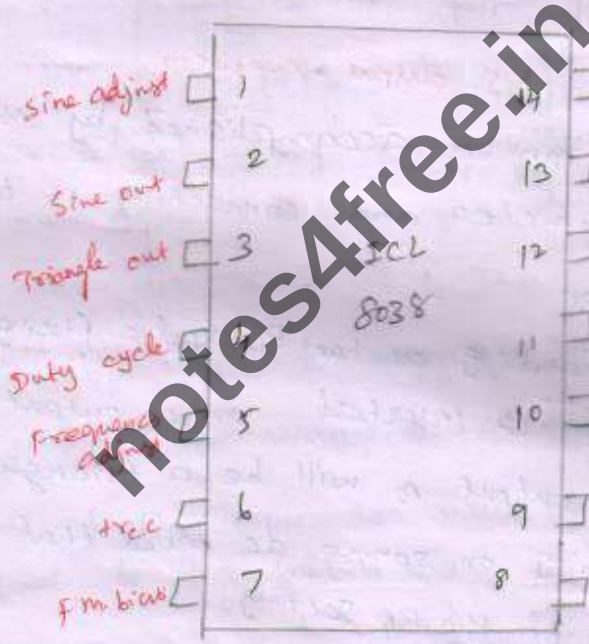


Fig. Pin diagram of ICL 8038.

The operation of ICL 8038 is based on charging & discharging of a grounded capacitor C, whose charging & discharging rates are controlled by programmable current generators I_1 & I_2

S.15

When switch is at position A, the capacitor charges at a rate determined by current source I_A.

Once capacitor voltage reaches V_{TH}, the upper comparator (CMP1) triggers & resets the flip-flop output.

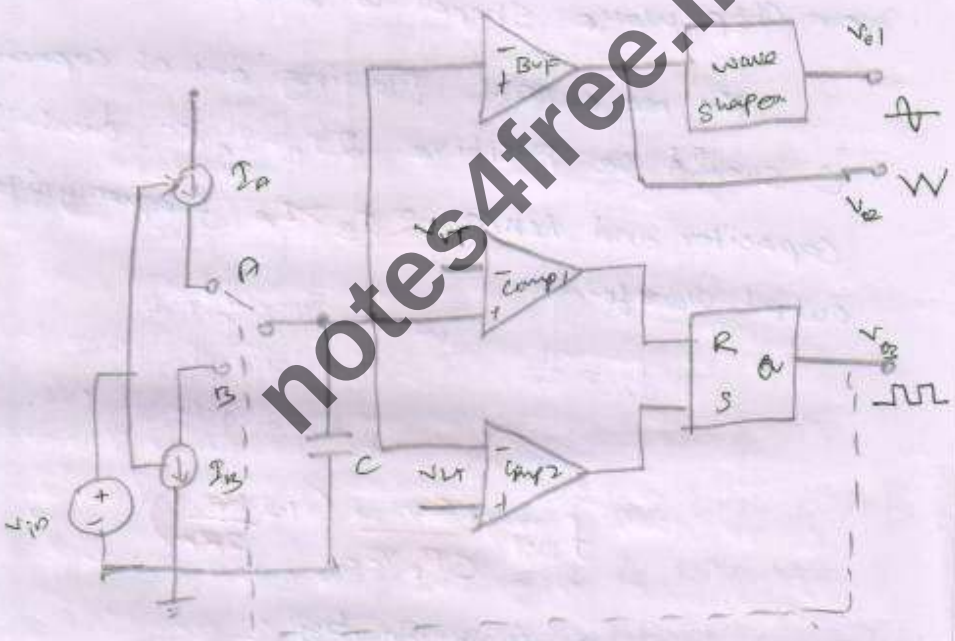


Fig. Block diagram of ICC 8038 function generator.

This causes the switch position to change from position A to B. Now capacitor starts discharging at the rate determined by the current sink

once the capacitor reaches V_{LT}, the lower comparator (comp 2) triggers and sets the flip-flop output. This causes the switch position to change from position B to A and this cycle repeats.

We get square wave at the o/p of the and triangular is then passed through the on chip wave shaper to generate sine wave.

The net current flowing out of capacitor C should be positive. $2I_B - I_A > 0$. discharges capacitor and hence $2I_B > I_A$ frequency of output waveform

$f_0 = \frac{1}{T}$ where $T = T_c + T_d$

T_c – charging time.

T_d – discharging time.

$$f_{out} = \frac{3V_1}{CR_n V_{CC}}\left(1 - \frac{R_B}{2R_n}\right)$$

Duty cycle is given by

$$\% d = \frac{T_c}{T_c + T_d} \times 100 = \left(1 - \frac{R_B}{2R_n}\right)$$

Application :-

→ communication

→ telemetry

→ Electronic music

→ Testing & calibration.

5.19

TIMER IC 555

The 555 timer is a highly stable device for generating accurate time delay or oscillation.

Signetic corporation first introduced the SE 555/NE 555 and two package styles

1) 8-pin circular style
2) TO-99 can or 8-pin mini DIP or 14 pin DIP.

Fig. Pin diagram of 555 Timer.

The 555 timer can be used with supply voltage in the range of +5V to +18V and can drive load upto 200mA. It is compatible with both TTL & CMOS logic circuits.

Because of the wide range of supply voltage the 555 timer is versatile and easy to use in various applications. such as oscillator, burglar alarm,

operation mode of 555 → Monostable operation
→ Astable operation

Monostable operation:

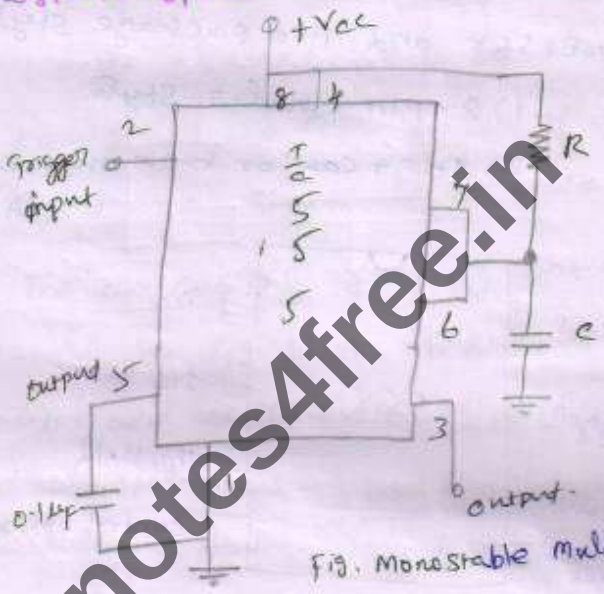


Fig. Monostable multivibrator.

In the standby state, FF holds transistor Q_1 on, thus clamping the external timing capacitor C to ground. The output remains at ground potential (low)

The trigger passes through Vcc/3, the FF is set ($\bar{Q}=0$). This make the transistor Q_1 off and the short circuit across the timing capacitor C is released.

5.19

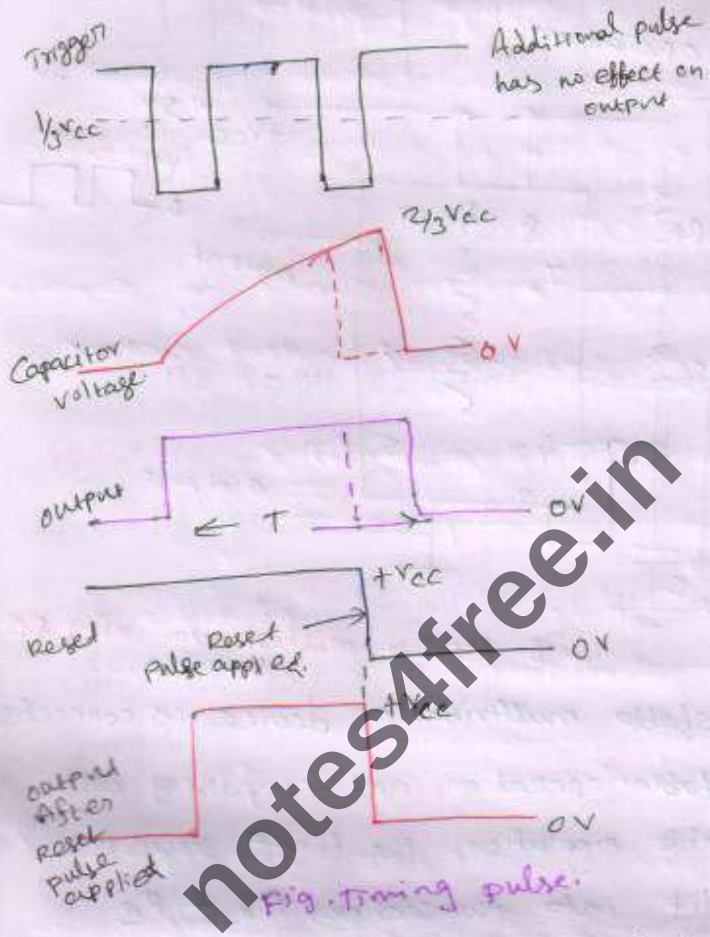


Fig. Timing pulse.

The timing interval is independent of the supply voltage. once trigger the output remains in the HIGH state until time T elapses. which depends only upon R and C.

Any additional trigger pulse coming during this time will not change the output state.

Astable operation.

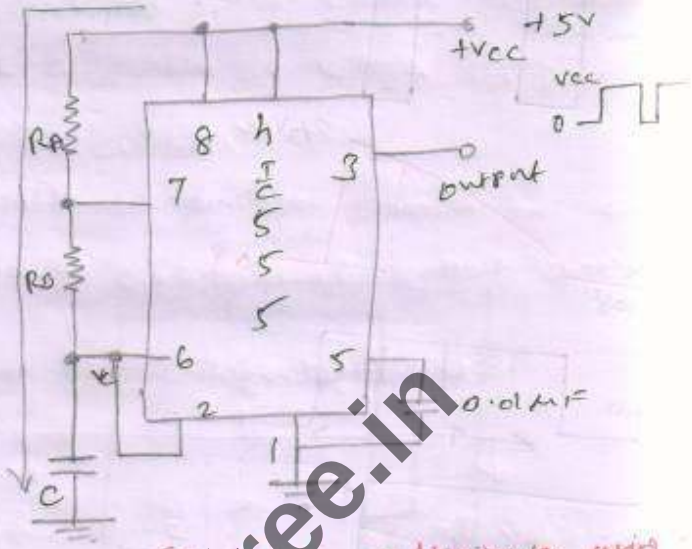


Fig. Astable Multivibrator using

Astable multivibrator device is connected for astable operation and comparing with monostable operation, the timing resistor now split into two sections R_A & R_B

PIN 7 of discharging transistor is connected to the junction of R_A and R_B

When the power supply V_{cc} is connected, the external timing capacitor C charges towards V_{cc} with at time constant $(R_A + R_B)C$.

If the output pin 3 is high state level is equal to V_{cc}.

5.21

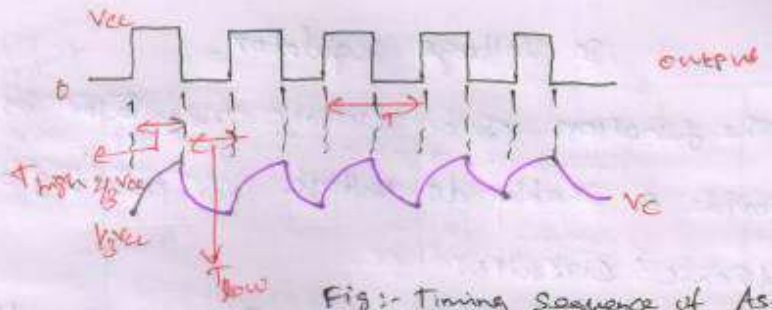


Fig:- Timing sequence of Astable multivibrator.

The length of time, the output remains HIGH is the time for the capacitor to charge from $(\frac{1}{3})V_{cc}$ to $(\frac{2}{3})V_{cc}$

The capacitor voltage for low pass RC circuit subjected to a step input of V_{cc} Volts is given by

$$V_c = V_{cc}(1-e^{-t/RC})$$

Applications:

* Missing pulse detector.
* Linear ramp generator
* Frequency divider
* pulse width modulation.

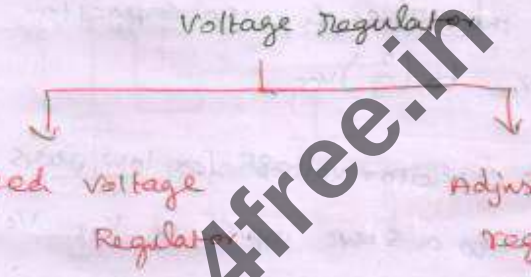
Features:

* Two operating mode i) monostable ii) Astable
* 8-pin metalcan package
* 8-pin mini DIP package
* output is capatible with TTL, CMOS & op-amp ckts
* Very high temperature stability

IC Voltage Regulator -

The function of a voltage regulator is to provide a stable dc voltage for powering electronic circuits.

A voltage regulator should be capable of providing substantial output current.



Three terminal fixed voltage regulator:-

78xx series are three terminal positive fixed voltage regulators with seven output voltage options available such as 5, 6, 8, 12, 15, 18 & 24 V.

In 78xx the last two numbers (xx) indicate the output voltage.

79 xx series of fixed output -ive voltage regulators which are complement to the 78 xx series devices.

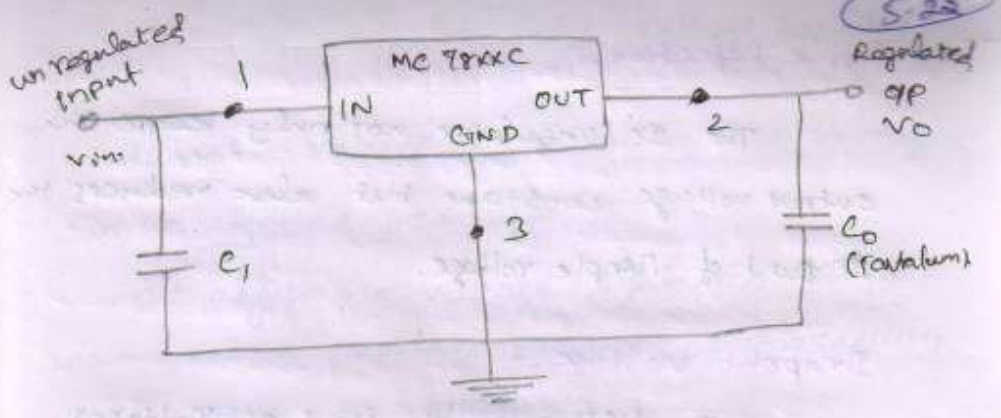


Fig:- Three terminal positive monolithic Regulator.

Three terminal voltage regulators have 3 terminals namely input which is unregulated (V_{in}), regulated output (V_o) and common or a ground terminal.

These regulators do not require any feedback connections.

The output capacitor C_o may not be needed but if used, it improves the transient response of the regulator.

Line / Input regulation:-

It is defined as the % change in the output voltage for a change in the input voltage.

Load regulation:-

The change in output voltage for change in load current and of V_o.

Ripple Rejection:-

The IC regulator not only keeps the output voltage constant but also reduces amount of ripple voltage.

Dropout voltage:-

The difference b/w i/p & o/p voltage ($V_{in}-V_o$) called dropout voltage.

Output resistance:-

It is the rate of change of output voltage with respect to the output current. It should be small.

Fig. metal can package

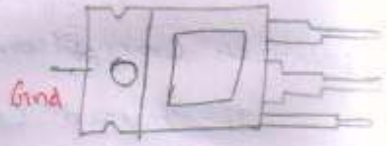


Fig plastic package

The minimum output voltage is the value of the fixed voltage available from the regulator.

The Lm117, 217, 317 positive regulators and Lm 137, 237, 337 negative regulators have been speacially designed to be used for obtaining adjustable output voltage

5.25

Three terminal Adjustable Voltage regulator (LM317)

Adjustable voltage Regulator, output voltage can be adjusted 1.2V upto 57V.

The adjustable voltage regulators have become more popular because of versatility performance & reliability.

The LM317 series is the most commonly used general-purpose adjustable voltage regulator

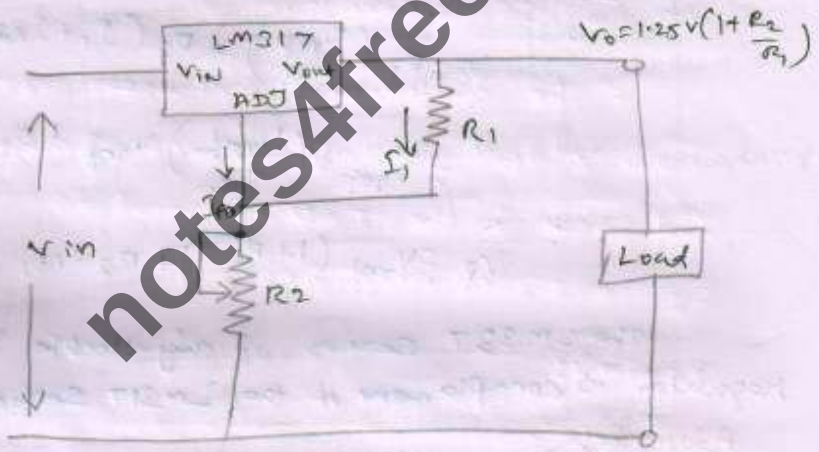


Fig:- Connection diagram of LM317 Regulator.

The LM317 requires only two external resistors to set the output voltage.

Reference voltage is impressed across resistor R_1 and since the voltage is constant. the current I_1 is also constant for a given value of R_1. Because resistor R_1 sets current I_1. This current Set or Program Resistor.

The output voltage V_o is

$$V_o = R_1 I_1 + R_2 (I_1 + I_{Adj})$$

where $I_1 = \frac{V_{Ref}}{R_1}$

R_1 - current (I_1) Set resistor

R_2 - output (V_o) set resistor

I_{Adj} - Adjustment pin current

I_1 value sub in V_o output voltage.

$$V_o = R_1 \left(\frac{V_{ref}}{R_1}\right) + R_2 (I_1 + I_{Adj})$$

$$V_{ref} + \left(\frac{V_{ref}}{R_1}\right) V_{ref} + R_2 I_{Adj}$$

$$V_o = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + R_2 I_{ADJ}.$$

The Lm337 series of adjustable voltage regulator is complement of the Lm317 series de

Advantage:-

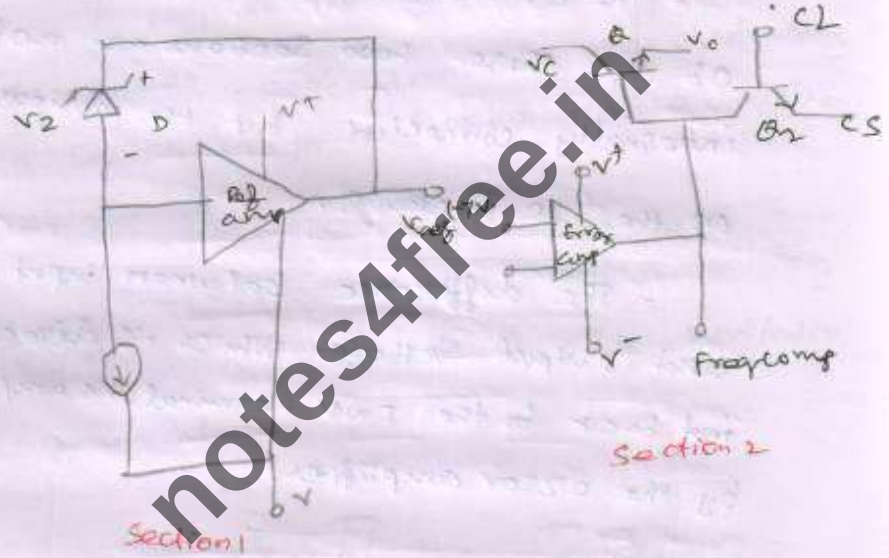
* Easy to use.
* It greatly simplifies power supply de
* Due to mass production.
* Low in cost.
* Ic voltage regulators are versatile.

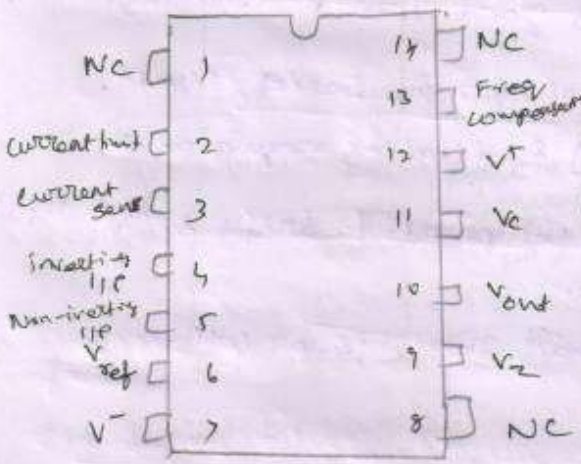
5.27

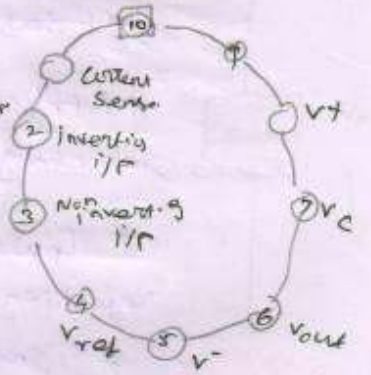
IC 723 general purpose regulator

Three terminal regulator have the following limitation.

* No short circuit protection.
* output voltage is fixed.







Metal can package

current limit

* The error amplifier compares a sample of the output voltage applied at the input terminal to the reference voltage V_{ref} applied at the NI input terminal.

* The error signal controls the conduction of Q_1. These two sections are not internally connected but the various pins on the IC package.

* The difference between input voltage and output voltage which is directly fed back to the INV terminal is amplified by the error amplifier.

Features:

* It has good line & load regulation.
* Application like Series, Shunt, switching & floating regulator.
* Low temperature drift & high ripple rejection.
* Small size, lower cost.

S.29

Monolithic Switching Regulator

The switching regulator, also called switched mode regulator operate in different way from a conventional series regulator.

To improve the efficiency of a regulator the series-pass transistor is used as a switch (turn ON & OFF) than a variable resistor in the linear mode.

The efficiency of a series switching regulator is independent of the input/output different relations.

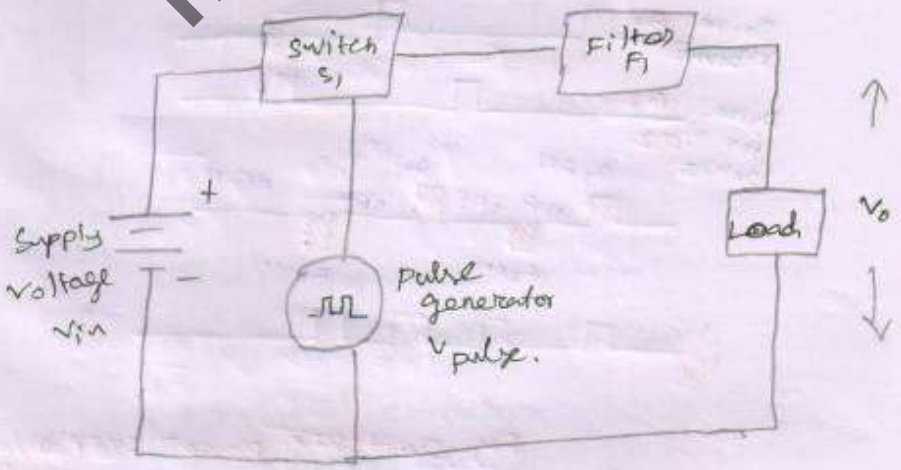


Fig. Basic switching regulator.

*) The duty cycle of the pulse waveform determines the relationship between the input and output voltages.

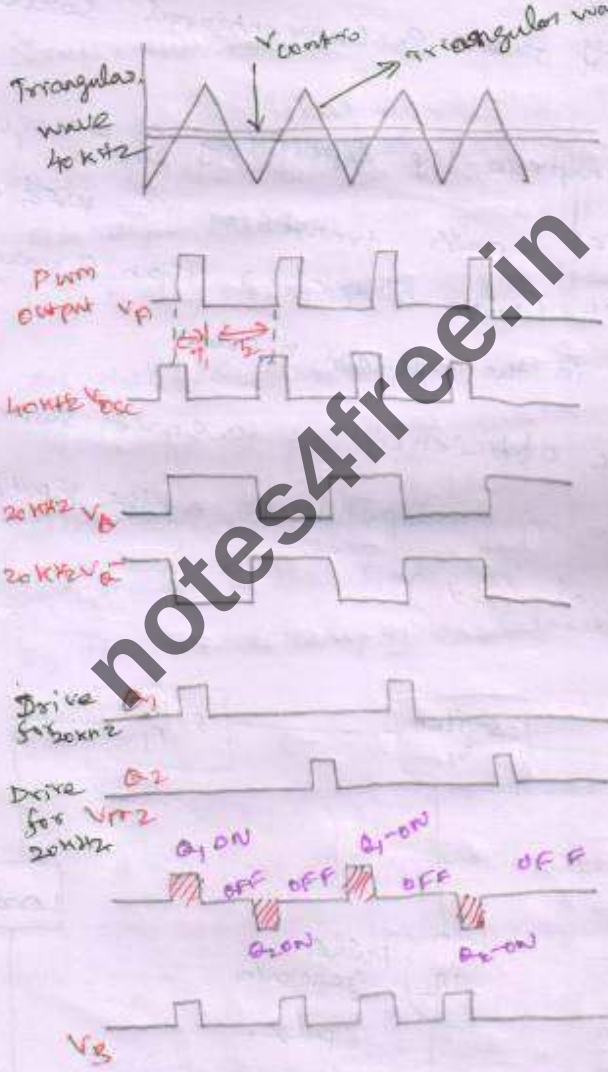


Fig switching power supply waveform

*) A high frequency triangular waveform is here used to reduce the ripple.

5.31

*) The duty cycle is the ratio of the on time the period of the pulse waveform.

$$\text{duty cycle} = \frac{t_{on}}{t_{on} + t_{off}}$$

$$= \frac{t_{on}}{T} = t_{on} f \quad \text{where } f = \frac{1}{T}$$

t_{on} - on-time of the pulse waveform

t_{off} - off time of the pulse waveform

T = time period = $t_{on} + t_{off}$ = $\frac{1}{\text{frequency}}$

*) Filter, converts the pulse waveform the output of the switch into a dc voltage

$$\frac{t_{on}}{T} \times V_{in}$$

t_{on} - on-time of the pulse.

T - Time period.

V_{in} - input voltage

Application:-

* Battery powered system
* Telecommunication circuits
* Personal computer
* printers.
* video games.

Switched Capacitor filter IC MF

The MF10 is a 20 pin Switched cap State variable filter IC from Nati Semiconductor.

The critical frequency is adjusta from 0.1Hz to 30 kHz with the exter generated clock.

The maximum clock frequency is

It contains two second order State variable filters one on the top a the other at the bottom with the control existing in the center.

The following relations are.

$$Q = \sqrt{\frac{R_2}{R_1} \times \frac{R_3}{R_4}}$$

$$f_o = \frac{f_{clk}}{100} \times \sqrt{\frac{R_2}{R_4}}$$

(or)

$$f_o = \frac{f_{clk}}{50} \times \sqrt{\frac{R_2}{R_4}}$$

The external resistors can be carefully Chosen to obtain flexibility.

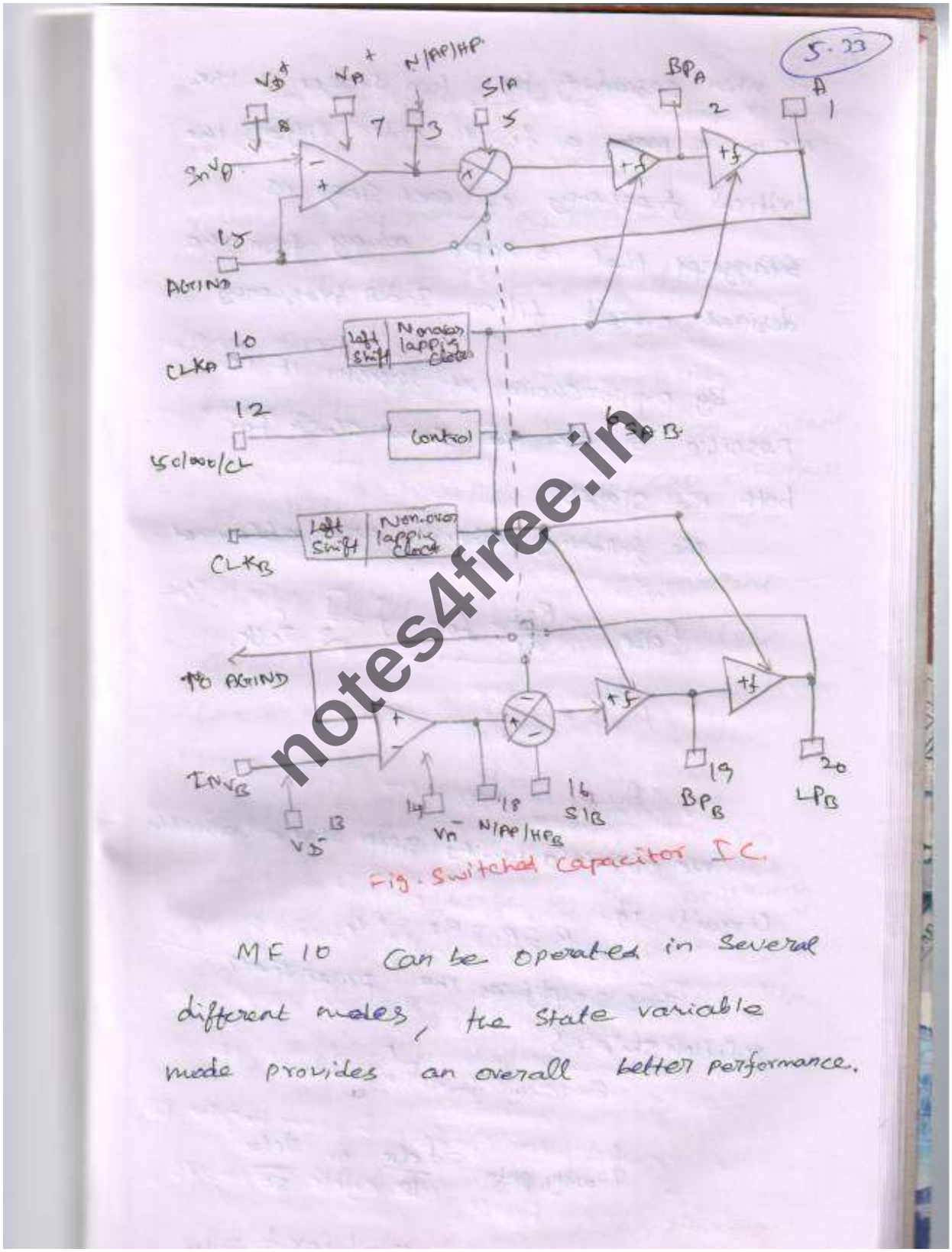


Fig. Switched capacitor IC

MF 10 Can be operated in several different modes, the state variable mode provides an overall better performance.

When cascading the two stages of the MF10 to make a fourth order filter, the critical frequency of each stage is staggered that is kept away from the desired overall filter 3-dB frequency

By proper choice of resistor it is possible to use the same device for both the stages.

The following relations are obtained

$$A_{OBP} = -\frac{R_2}{R_1} \text{ for } f = \frac{1}{2} f_{clk}.$$

$$A_{OHP} = -\frac{R_3}{R_1}$$

$$A_{OLP} = -\frac{R_4}{R_1}$$

we obtain a unity gain state variable

Circuit if $R = R_1 = R_2 = R_4$

This simplifies the parameter relationship as

$$\text{@ unity gain} = \frac{R_3}{R_6}$$

$$f_{o\,\text{unity gain}} = \frac{f_{clk}}{10} \text{ or } \frac{f_{clk}}{50}$$

$= -1$ for $\frac{1}{2} f_{clk}$

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Frequency to voltage & voltage to Frequency converter :-

voltage to Frequency converter :-

The 9400 is designed for pulse and square wave outputs having a frequency range 1Hz to 100KHz.

The Input can be either current or voltage and the output can interface with most form of logic.

A V/F converter equivalent circuit consists of an integrator, Comparators, a stable by network, a divide by 2 - Network and open collector output transistors.

The input current $I_{in} = \frac{V_{in}}{R_{in}}$ is converted to a charge by the integrating capacitor C_{int} and shows up as a linearly decreasing voltage V_A at the o/p of the OP-amp integrator.

$$V_A = -\left(\frac{I_{in}}{C_{int}}\right)t$$

I_{in} - input current (amperes).

t - time (Seconds)

V_A - o/p V_A of the integrator.

Pin diagram 9400.

The integrating capacitor Cint again begins converting the input current Iin to a charge and the output of the op-amp starts decreasing linearly.

When the output of the op-amp goes slightly below 0V, the output of the comparator goes from high to low. and hence the cycle repeats.

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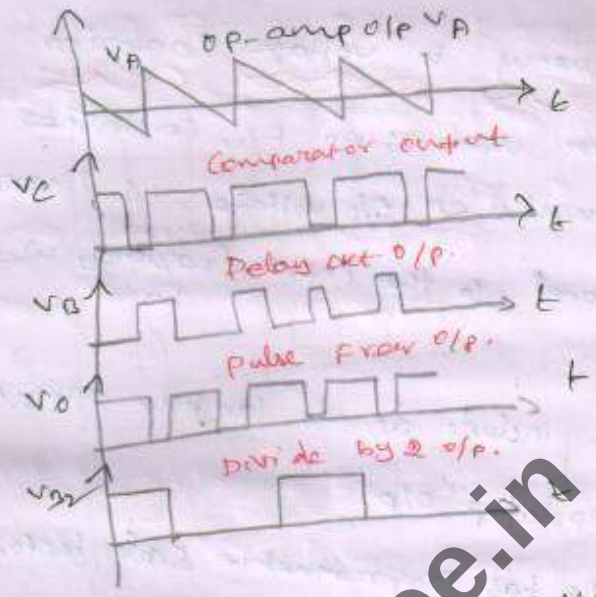

Fig :- output waveform of V/F converter.

Applications:

* Instrumentation & control
* Digital & communication sys.
* Temperature sensing & control
* Transducer Encoding.
* A/D converter.
* microprocessor data Acquisition.
* Digital panel meters.
* phase locked loop.

Frequency to voltage Converter

When used as an F/V converter the 9400 generates an O/P voltage is linearly proportional to the input frequency waveform

Features:-

* it include dc to 100 kHz operation
* op_amp O/P.
* It has programmable scale factor
* high input impedance (>10MΩ)
* its capacitors to accept any voltage shape.

When 9400 is used as a F/V Converter the input frequency is applied to the +ive input of the comparator.

The comparator hysteresis voltage is ± 200mV. The input signal amplitude must be greater than ± 200 mV in order to trip the comparator.

If only a unipolar input signal is available, it can be converted into a bipolar waveform by using the offset.

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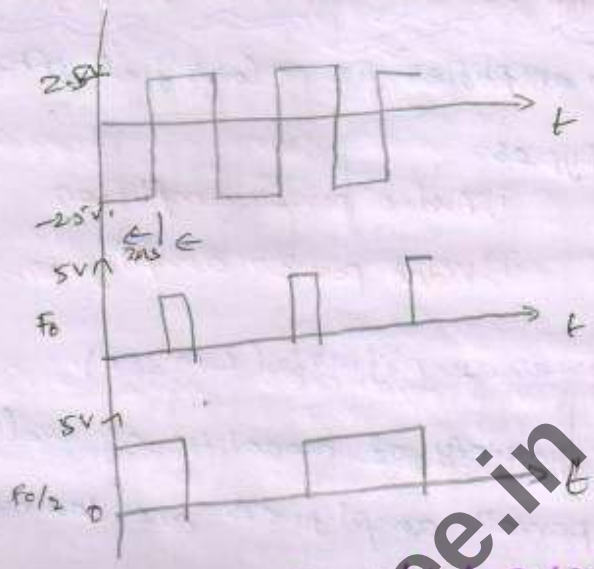

Fig. F/V digital outputs.

Each time the input signal crosses zero in the -ve direction, the output of the Comparator goes low.

On the other hand, each time the input waveform crosses zero in the +ve direction, the output of the comparator switches high.

Application:

* Frequency meter.
* tachometer.
* spectrometer.
* RPM indicators.
* motor control.

AUDIO & VIDEO POWER Amplifier.

Power amplifier is classified into the two types.

i) Audio power amplifier.

ii) Video power amplifier.

Audio power amplifier:- (LM380)

A variety of monolitic as well as hybrid power amplifiers are commercially available.

The power amplifiers differ from signal general-purpose op amps in delivering various amounts of power are nearly compact.

Features:

* Internally fixed gain of 50 (34dB)
* Wide supply voltage range (5 to 22V)
* Output is short-circuit proof with internal thermal limiting.
* High peak current capability
* High impedance.
* Standard dual-in-line-package.

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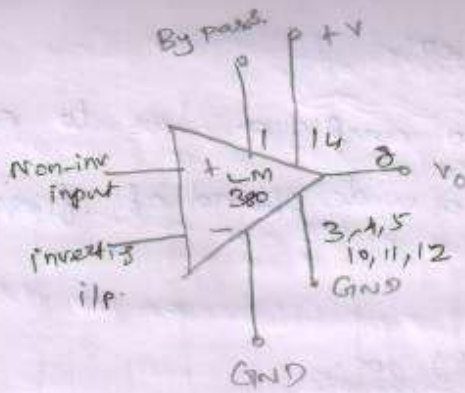

Fig:- symbolic repreprepresentation of LM380 Audio Amplifier.

Application:-

The number of external components LM380 is very less, it is mostly used for consumer applications

a) LM380 Audio Power amplifier.

b) Bridge power Audio amplifier

c) Intercom System.

The overall internal, voltage gain of the amplifier fixed at 50, gain can be increased by using positive feed back.

Video amplifier:-

A video amplifier has to amplify signals over a wide band of frequencies (20 MHz)

It is necessary for:-

i) All the frequencies must be amplified equally to maintain the same relative amplitudes.

ii) The relative phase of all the frequency components in the output must be the same as at the input.

Video amplifier is a wideband amplifier with bandwidth from dc to high frequency up to few MHz.

At low frequencies the problem may be eliminated by direct coupling which is readily possible for one or two limited number of stages.

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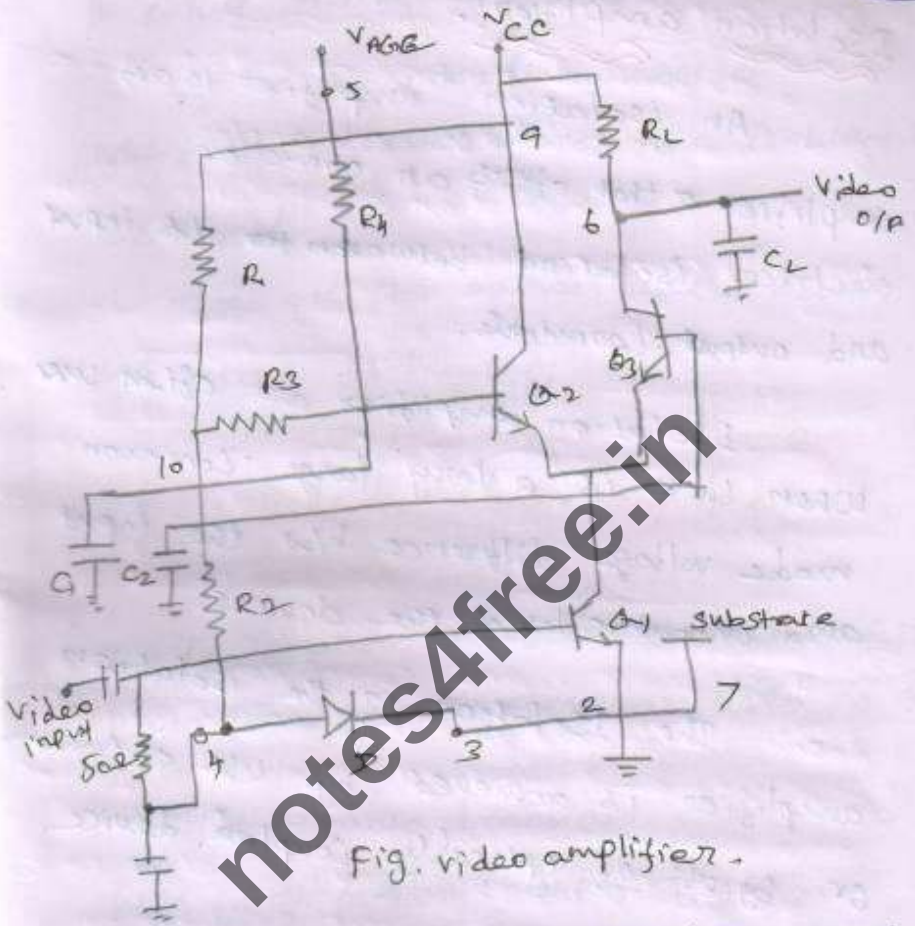


Fig. video amplifier.

Circuits with capacitor coupling, suitable compensation for low frequency response is possible. The dc being restored by dc restorer diode clamping circuits.

High frequency compensation can be achieved by shunt - series peaking coils in the load circuits.

Isolation amplifier:-

An isolation amplifier is an amplifier that offers an ohmic or electrical isolation between its input and output terminals.

Isolation amplifier are often used when there is a very large common mode voltage difference b/w the input and output sides of the devices.

The isolation in the isolation amplifier is achieved by use of transformer or by use of optically coupled device.

Fig. Different Symbols used for isolation amplifiers.

An important characteristics of an isolation amplifier is the linearity of the input

5.45

to output transfer Characteristics.

But the non-linear input current to light output characteristics is a problem in this regards.

There are two methods used to obtain high degree of linearity.

a) LED-photo transistor couples.

b) Isolated current amplifiers with feedback linearization.

An isolation amplifiers in which a LED. photo transistor couplers are used as an opto isolators.

LED-photo transistor coupler is used in the feedback loop amplifiers.

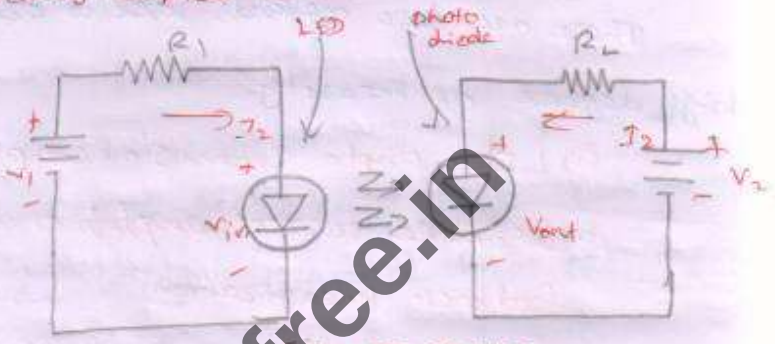
The second LED photo transistor coupler is used at the input of amplifiers.

Both LED-photo transistor Couplers used with matched characteristics, are driven by the same amplifiers.

Due to the matched characteristics of the two LED-photo transistor pairs the non-linear characteristics & temperature dependence get compensated

Opto Coupler and fiber optic Ics

* The combined package of a LED and a photodiode is called an opto coupler.
* It is also called an opto isolator or an optically coupled isolator



(a) opto coupler

* The source V_1 and series resistance R_1 decide the forward current I_1 through the LED. Thus LED emits the light. This light is incident on a photodiode.
* A reverse bias current is set up in the output circuit this current produces a drop across the output resistance R_2

$$V_{out} = V_2 - I_2 R_2$$

Characteristics:-

* Current transfer ratio.
* Isolation voltage b/w i/p & o/p
* Response time
* Common mode Rejection.
* Bandwidth.

Features:-

* The isolation voltage ±2500V

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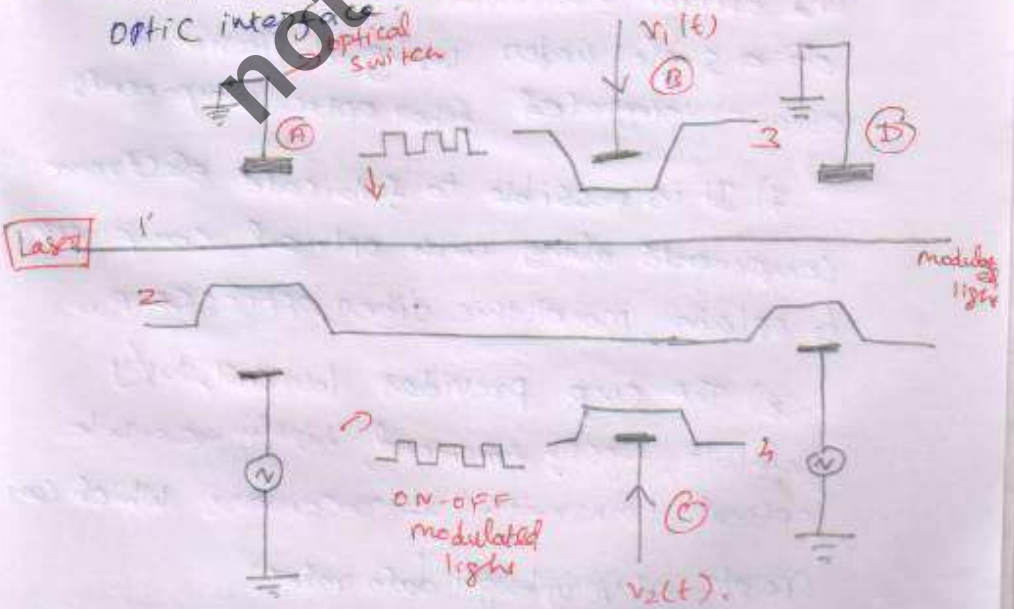
* Total power dissipation is 250mw
* Low cost dual in line package.

Advantage:-

* Electrical isolation b/w i/p & o/p circuit
* The response times of optocoupler is small
* Capable of wideband signal transmission
* Easy interfacing with logic devices.
* Compact & light weight.

Fiber optic IC

* A fiber optic technology is well suited for such applications, fastest growing segments in the electronics market.
* Number of fiber optic product can be used to implement a range of different fiber optic interfaces.



*) Two most important Advantages of fibes optic system over copper wire conventional systems are.

*) The low level of at attenuation on high frequency signals. This is what is required for long distance telephone lines and computer networks

*) The lack of RFI radiation and a low sensitivity of EMI noise which increases the accuracy and the security of the data transmission

*) All the devices such as optical modulators opto couplers, wavelength multiplexers, and optical switches can be fabricated on a single wafer using diffusion to obtain integrated fiber optic components

*) It is possible to fabricate electronic components along with optical components to obtain monolithic fiber optic chip.

*) The chip provides low cost, highly reliable, highly functional, highly accurate optical transmitters & receivers which can operate at very high data rates.